SIGNETICS ANALOG

APPLICATIONS MANUAL

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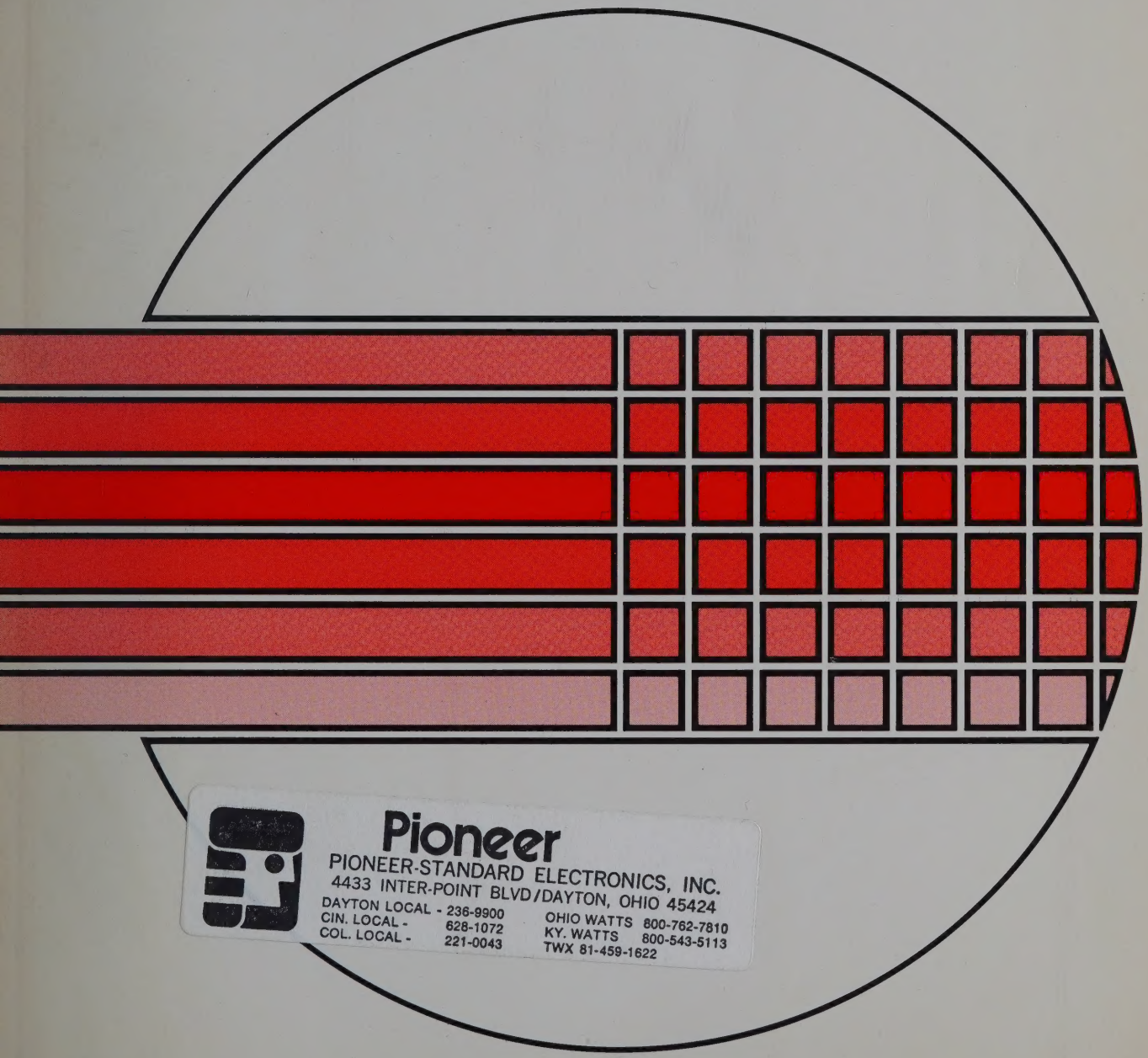

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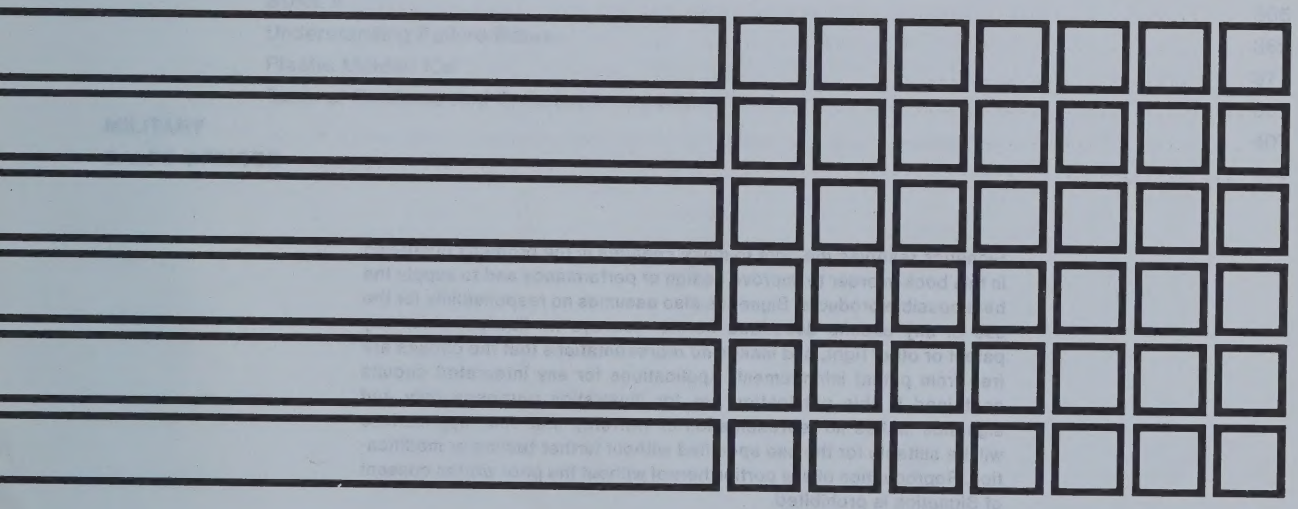

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SECTION I
ANALOG IC PROCESSING

As one of the world's largest manufacturers of integrated circuits, Signetics designs, develops, manufactures and sells over 1600 different types of integrated circuits. Signetics produces linear circuits, utilizing both bipolar and metal-oxide-semiconductor (MOS) manufacturing processes.

The Analog division is a major broad line supplier of both Signetics' original designs and industry standard devices. The NE535 High Performance Operational Amplifier, the NE554 Dual Tracking Regulator and the ST100 Codec (Telecommunications) are among Signetics' original products. The breadth of the Analog product line offers the designer, the component engineer, and the purchasing agent a varied approach to linear circuits.

This broad analog circuit product line is backed by Signetics' industry image as a quality manufacturer to whom the servicing of the customer's needs is paramount.

The 1979 Analog Application Manual is intended to serve as a single technical reference for designing with linear circuits by presenting applications information necessary to implement properly Signetics' analog products. The Applications portion is updated and rewritten to reflect data on new products issued.

Additions and erratta will be generated at periodic intervals.

Your inputs to improve our publications will be greatly appreciated.

Ira Zingmond,
Manager, Linear
Applications

SECTION I
ANALOG IC PROCESSING

SECTION I
PROCEDURE TO FOLLOW

INTRODUCTION

Integrated circuits are divided into three general categories: (1) linear, (2) digital, and (3) MOS. Distinctly different design and process techniques are used for each type. The main difference between linear processes and other IC processes is their diversity. While digital circuits are commonly restricted to low voltage switching, linear circuits may be fabricated with anything from switching to linear characteristics, high or low voltages, high or low frequency, or any combination of these properties. To cope with this range of applications, the following processes are frequently used:

Epitaxial— 0.25 ohm-cm gold doped and non-gold doped
0.5 ohm-cm gold doped
1.0 ohm-cm Schottky and non-Schottky
2.5 ohm-cm
5.0 ohm-cm

Dielectric— 2 to 15 ohm-cm

All epitaxial processes are similar. The main difference is the resistivity of the deposited epitaxial layer in which the components are formed. This provides the means of selecting higher breakdown voltages or lower saturations by merely selecting an epitaxial resistivity.

For instance, the 5 ohm-cm process is used for operational amplifiers and regulators because it gives the 50V LV_{ceo} transistor breakdowns required. Since the phase lock loops need only 20V, and lower saturation voltages are desirable, the 2.5 ohm-cm process is used for their fabrication.

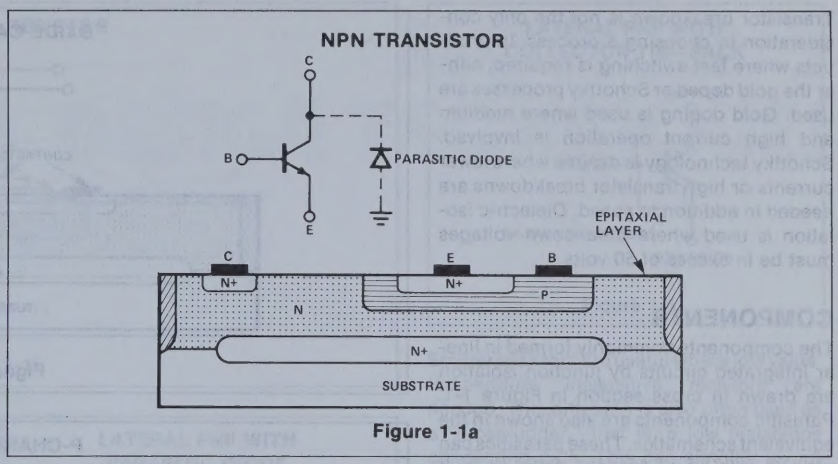


Figure 1-1a

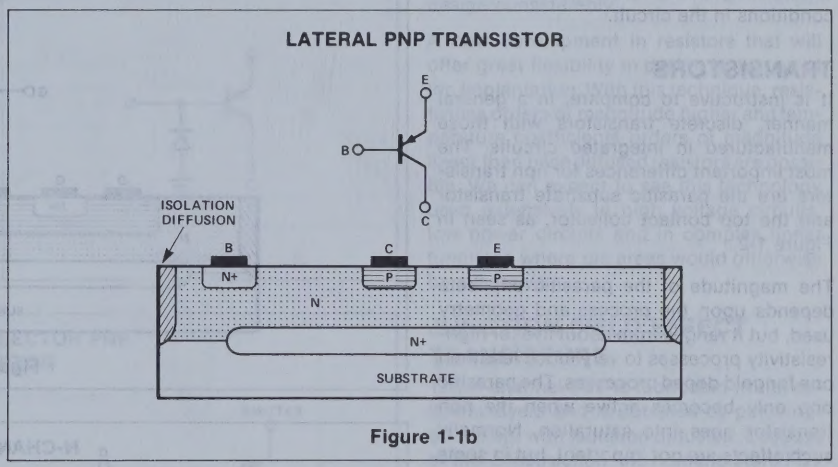


Figure 1-1b

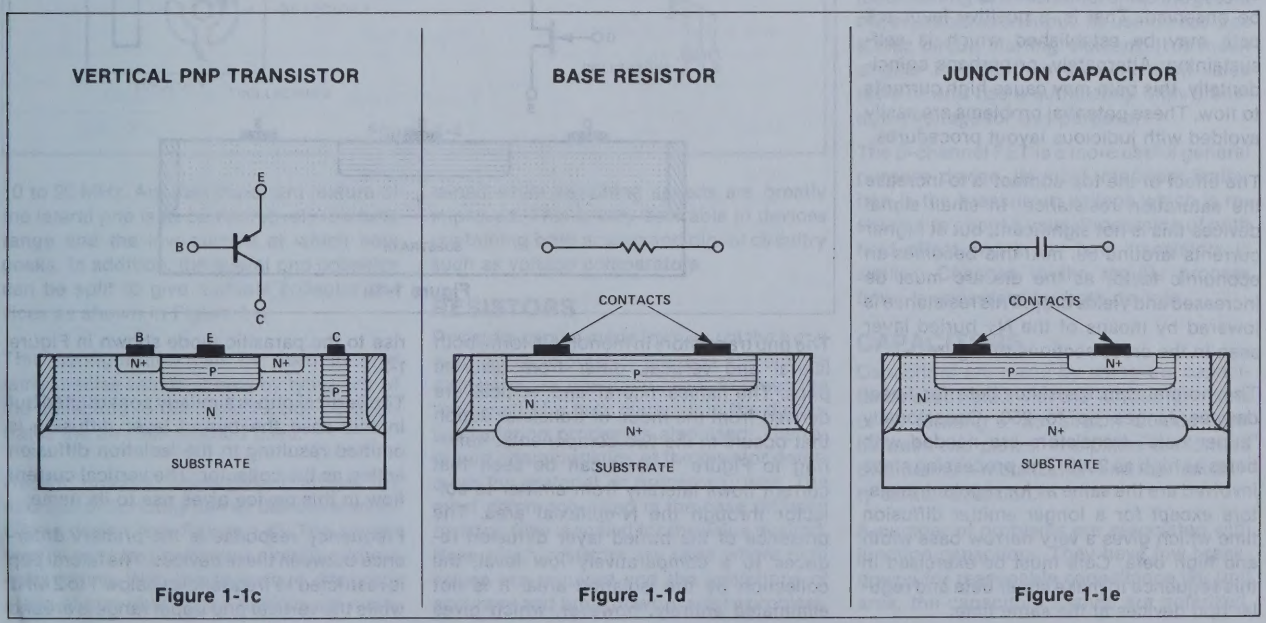


Figure 1-1c

Figure 1-1d

Figure 1-1e

Transistor breakdown is not the only consideration in choosing a process. In products where fast switching is required, either the gold doped or Schottky processes are used. Gold doping is used where medium and high current operation is involved. Schottky technology is desired where lower currents or high transistor breakdowns are needed in addition to speed. Dielectric isolation is used where breakdown voltages must be in excess of 50 volts.

COMPONENTS

The components commonly formed in linear integrated circuits by junction isolation are drawn in cross section in Figure 1-1. Parasitic components are also shown in the equivalent schematics. These parasitics can occasionally cause "sneak" paths or fault conditions in the circuit.

TRANSISTORS

It is instructive to compare, in a general manner, discrete transistors with those manufactured in integrated circuits. The most important differences for npn transistors are the parasitic substrate transistor and the top contact collector, as seen in Figure 1-2.

The magnitude of the parasitic pnp beta depends upon the process and geometry used, but it ranges from about five for high-resistivity processes to very much less than one for gold doped processes. The parasitic pnp only becomes active when the npn transistor goes into saturation. Normally such effects are not important, but in some circuit configurations latching effects may be observed. That is, a positive feedback path may be established which is self-sustaining. Alternately, or perhaps coincidentally, this path may cause high currents to flow. These potential problems are easily avoided with judicious layout procedures.

The effect of the top contact is to increase the saturation resistance. In small signal devices this is not significant, but at higher currents (around 50. mA) this becomes an economic factor as the die arc must be increased and yields drop. This resistance is lowered by means of the N+ buried layer seen in the cross sections of Figure 1-1.

The normal npn transistor beta for linear devices ranges up to 250. Occasionally "super beta" transistors are needed with betas as high as 2000. The processing steps involved are the same as for regular transistors except for a longer emitter diffusion time which gives a very narrow base width and high beta. Care must be exercised in this sequence to make super beta and regular npn devices at the same time.

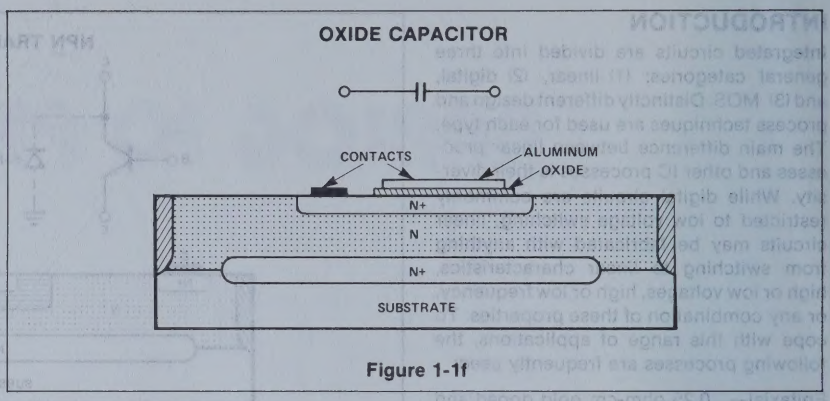


Figure 1-1f

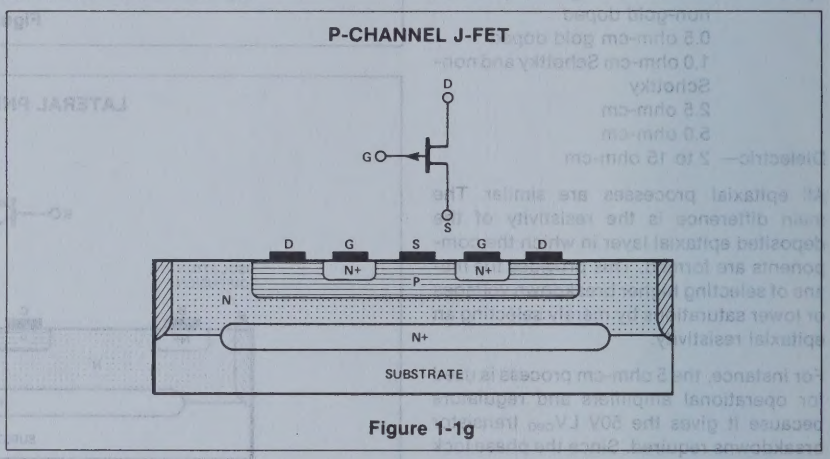


Figure 1-1g

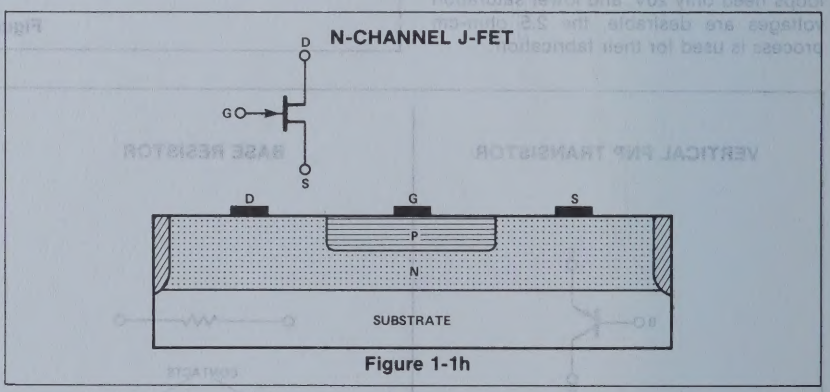


Figure 1-1h

The pnp transistors in monolithic form, both lateral and vertical, differ from discrete pnps. The names 'lateral' and 'vertical' are derived from the mode of transistor action that occurs in the two components. Referring to Figure 1-1B it can be seen that current flows laterally from emitter to collector through the N-epitaxial area. The presence of the buried layer diffusion reduces to a comparatively low level, the collection by the isolation area. It is not eliminated entirely, however, which gives rise to the parasitic diode shown in Figure 1-3.

The vertical pnp is similarly constructed but in this case the buried layer diffusion is omitted resulting in the isolation diffusion acting as the collector. The vertical current flow in this device gives rise to its name.

Frequency response is the primary difference between these devices. The lateral pnp is restricted to frequencies below 1 to 2 MHz while the vertical pnp upper range is around

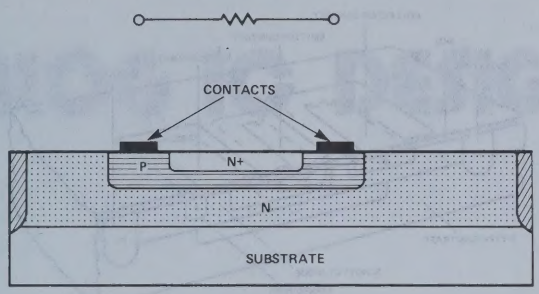


Figure 1-1i

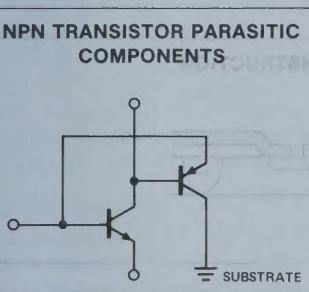


Figure 1-2

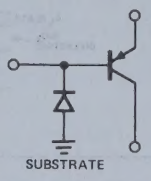


Figure 1-3

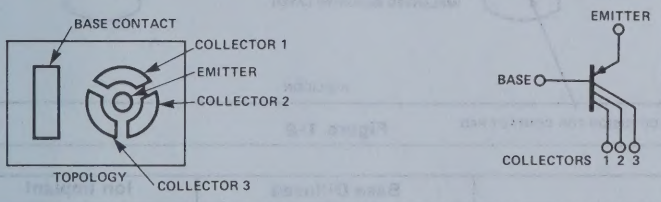


Figure 1-4

10 to 20 MHz. Another important feature of the lateral pnp is its comparatively low beta range and the low current at which beta peaks. In addition, the lateral pnp collector can be split to give multiple collector devices as shown in Figure 1-4.

This configuration can be used to give fairly precise values of beta by tying one of the collectors to the base. Figure 1-5 illustrates the tie back method used.

Recent process development allows the addition of Schottky barrier devices to monolithic design (see Figure 1-6). The advantage is very fast switching circuits without gold doping. With this technique, the properties of non-gold doped devices are maintained while switching speeds are greatly improved. This is very desirable in devices containing both analog and digital circuitry such as voltage comparators.

RESISTORS

Resistors can be made from any of the n or p type layers. In practice the base and emitter diffusions are generally used. At times the "epilayer" (the bulk material) in the dielectric isolation process is also used. The required characteristics of the resistor determine the material or processes used. The most commonly used is the base diffused resistor. Size is scaled for the value desired. Base pinch resistors are used where high values are required and the limitations of accuracy and breakdown are not a problem.

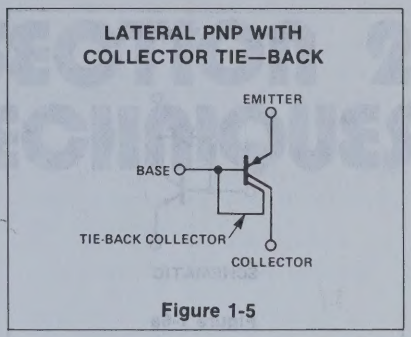


Figure 1-5

Emitter resistors are useful where low value, temperature insensitive resistors are needed. This diffusion is also often used as a "cross-under," that is, a low resistance connecting path. This can simplify layout design considerably.

A new development in resistors that will offer great flexibility in design is the use of ion implantation. With this technique, resistivities orders of magnitude higher and temperature coefficients orders of magnitude lower than base diffused resistors are possible. We can expect to see this technology used extensively in high voltage circuits, low power circuits and in complex linear functions where die areas would otherwise be excessive.

JUNCTION FIELD EFFECT TRANSISTORS

The n-channel FET is fabricated in the epitaxial layers and is obtained by pinching-off the epi with isolation diffusion. Because of this construction, the nomenclature FET is something of a misnomer since the gate is not available as an input. Its usefulness is as a bias circuit starting element. It is much smaller in area than an equivalent value resistor and has a sufficiently high breakdown voltage for this purpose.

The p-channel FET is a more useful general purpose device. Its most important limitation is the breakdown voltage which is restricted to about 5 volts. Processing of both field effect and super beta transistors is similar. Changes in the regular process flows is necessary for both devices.

CAPACITORS

Capacitors are made by using the capacitance associated with the various junctions or by forming a thin silicon dioxide layer between two plates. The plates are formed by aluminum metalization and low resistivity emitter diffusion.

A number of problems are associated with junction capacitors. They have low breakdowns for reasonable capacitance per unit area, the capacitors formed are polarized,

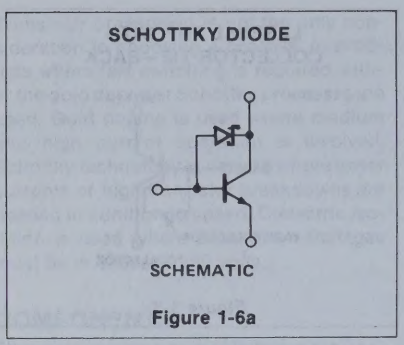


Figure 1-6a

and they have high leakage currents. Oxide capacitors are free from these problems but the capacitance per unit area is comparatively low. Junction capacitors are used primarily where decoupling capacitors are needed, while oxide capacitors are used where high quality is needed.

OTHER DEVICES

There are a number of other components such as SCR, SCS and Zener diodes that are available coincidentally with the components discussed above. The Zener diodes available are the emitter base junction and the emitter-isolation junction. Other junctions have breakdowns that are high and variable so they are seldom used.

ION IMPLANTATION

The ion implantation process is a room temperature process.This process permits the fabrication of very large value resistors, otherwise economically unobtainable with the standard diffusion process. The cost of using implantation to fabricate resistors is essentially that of one additional masking step in the conventional monolithic process. The masking is done following the last high-temperature diffusion—the emitter diffusion. This is necessary since exposure of the implanted wafers to high diffusion temperatures will result in changes to the implanted characteristics.

Figure 1-8 illustrates the compatible ion implantation resistor process as applied to otherwise conventional monolithic devices. The implantation is done into the "N" type epitaxial material which is normally covered by about 8 to 10kÅ of silicon dioxide. Through the use of standard photomasking techniques, this field oxide is opened to permit the penetration of the charged ions into the semiconductor material. The base diffused regions serve to provide low-resistance contact terminations for the implanted resistors. The resistivity of the implanted region is precisely controlled by varying the dose of ions which is accurately known by measurement of the beam current.

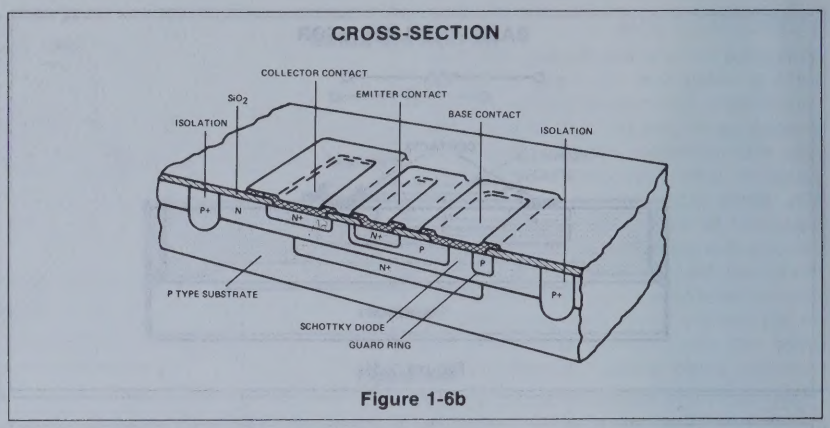


Figure 1-6b

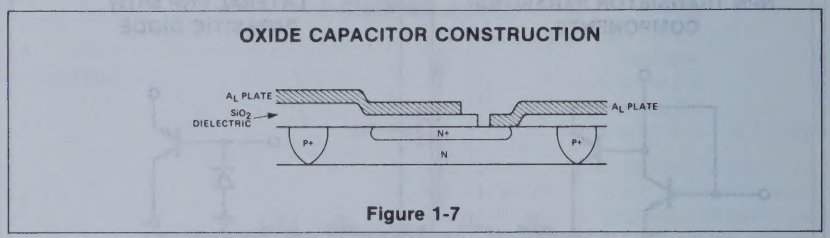


Figure 1-7

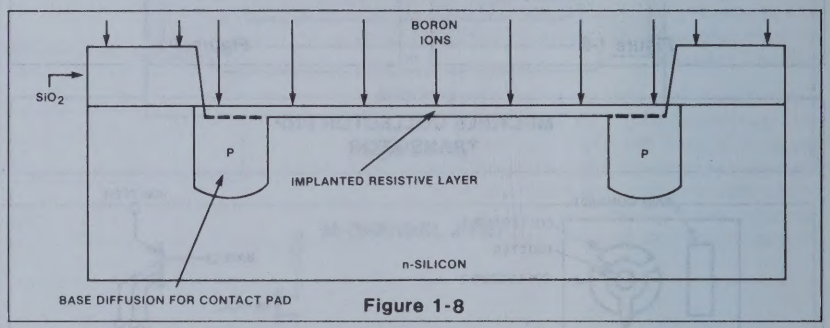


Figure 1-8

	Base Diffused	Ion Implant
Sheet Resistivity	150Ω/□[2]	200 - 10KΩ/□[2]
Maximum Resistance	50KΩ	5MΩ
TCR	2000 ppm/°C	Note 1
Initial Accuracy	20 - 30%	5 - 10%
Matching	< 3%	< 1%

TABLE 1-1

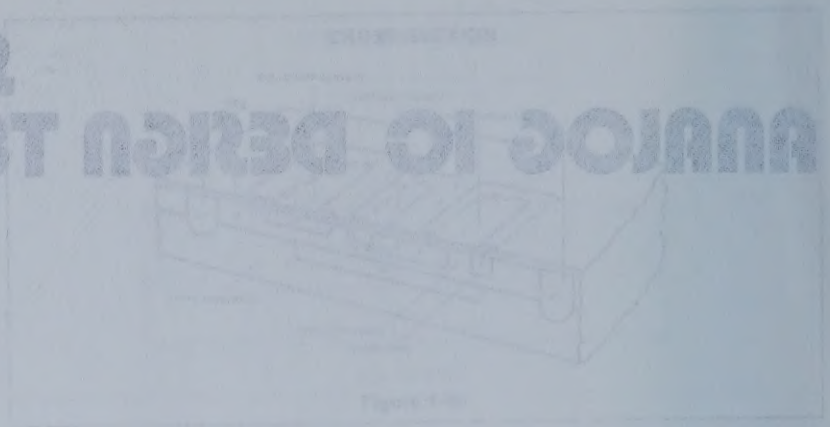
NOTE
1. Dependent upon sheet resistivity & processing 2. Ω/□ = ohms per square

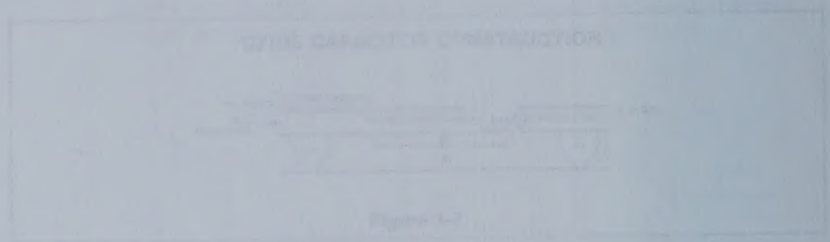
It is also interesting to note that the lateral component of conventional diffused resistors, known as out-diffusion or side diffusion, is essentially zero with implantation due to its inherent low temperature processing. Hence, the accuracy and matching of the resistors is primarily determined by photomasking tolerances. Table 1-1 summarizes a comparison of ion-implanted vs diffused resistor components.

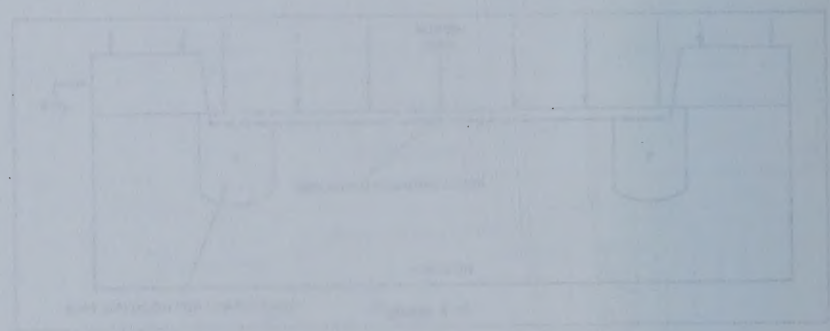
The use of ion implanted resistors can act to improve designs in several ways.

First, in a conventional integrated circuit design with a significant amount of resistance, the use of ion implantation can significantly reduce chip area, improve yields, and hence significantly lower the cost of manufacturing the device. This is true particularly in the newer more complex circuits where chip area exceeds 5000 sq. mils. Chip size can be reduced by savings amounting to 20 to 30%. This is done at the modest cost of one additional masking and subsequent room temperature processing.

SECTION 2
ANALOG IC DESIGN TECHNIQUES







INTRODUCTION

The components available for linear ICs were reviewed in the previous section. From that discussion it was clear that many differences exist between IC components and those available to discrete circuit design. These differences may be conveniently summarized as follows:

A. Limited resistor accuracy and values
B. Lack of integrated inductance
C. Small integrated capacitance values
D. Poor PNP transistor performance
E. Limited power dissipation

On the other hand, linear IC designs have the advantages of excellent component matching, both active and passive; and the accessibility of a great number of active components.

To cope with the limitations of monolithic circuitry, designers have evolved special techniques and practices, a number of which are detailed in this section.

BIAS CIRCUITRY

In discrete designs the bias circuitry is accomplished by high value resistor networks. In linear designs this is impractical because of the die area required. The alternative is to use an n-channel FET as shown in Figure 2-1.

SIMPLE BIAS CIRCUIT

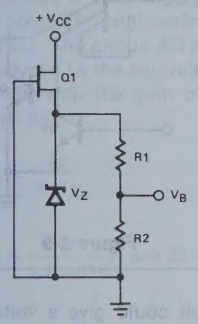


Figure 2-1

Zener V_Z is fed current by FET Q1. The required bias voltage is then developed by the resistor divider R1 and R2. This simple technique can be elaborated upon if temperature compensation is required. By adding transistor Q2 shown in Figure 2-2, the positive temperature coefficient of the zener diode is offset by the negative one of the forward biased emitter-base diode.

More elaborate schemes, which include the maintenance of constant currents in the

TEMPERATURE COMPENSATED BIAS NETWORK

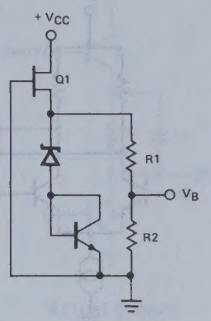


Figure 2-2

diodes, buffering the load from the source, and adjusting the composite temperature coefficient to zero, are commonly found where accurate references are required.

Current sources as well as voltage sources can be easily obtained using similar circuitry. Both npn and pnp type current sources are depicted by Figure 2-3.

NPN AND PNP CURRENT SOURCES

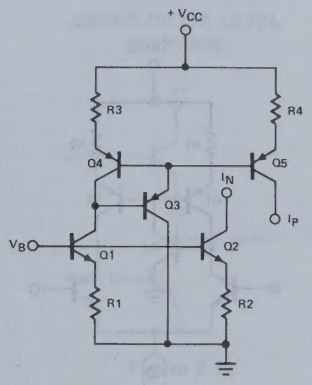


Figure 2-3

Assuming Q1-Q2 and Q4-Q5 are well matched and of the same geometries it can be shown that :
Equations

$$I_{NPN} = \frac{V_B - V_{BE}}{R2} \text{ and} \qquad (2\text{-}1)$$

$$I_{PNP} = \left[\frac{V_B - V_{BE}}{R1}\right]\frac{R3}{R4} \qquad (2\text{-}2)$$

These equations demonstrate that the circuit currents can be made independent of external supply voltages and temperature fluctuations. Circuits such as these are used extensively in modern operational amplifiers such as the NE531 and NE536, where their presence assures that such parameters as coltage gain and offset voltage remain constant with temperature supply voltage variations.

The preceding circuits are valuable for high and medium values of current. Low current values are better developed by the popular circuit of Figure 2-4.

LOW VALUE CURRENT SOURCE

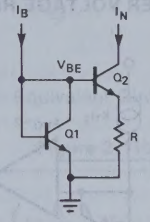


Figure 2-4

If the geometries of Q1 and Q2 are identical, the following equations hold:

$$V_{BE1} = V_{BE2} + I_N R \qquad (2\text{-}2a)$$

$$V_{BE1} = \frac{kT}{q} \ln\left(\frac{I_B}{I_S}\right) \qquad (2\text{-}2b)$$

$$V_{BE2} = \frac{kT}{q} \ln\left(\frac{I_N}{I_S}\right) \qquad (2\text{-}2c)$$

$$I_N R = \frac{kT}{q} \ln\left(\frac{I_B}{I_N}\right) \qquad (2\text{-}2d)$$

Where the subscripts refer to their respective transistors, beta is high, and other symbols have their standard meaning.

This is a transcendental equation which is represented graphically by Figure 2-5.

CURRENT SOURCE FAMILY CURVES

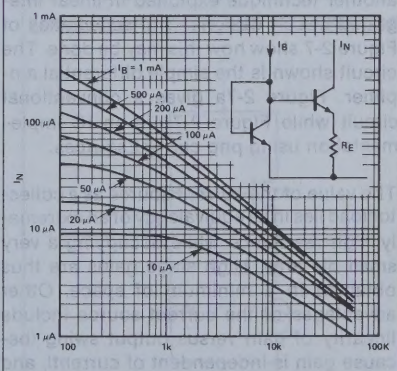


Figure 2-5

As can be seen, it becomes possible to obtain very low currents with reasonable values of resistance. This circuit is used in the NE592 where I_{bias} is set by a single resistor and the value of theoperating power supplies.

This principle may be extended to provide a particularly useful voltage reference. The circuit of Figure 2-6 illustrates how this is done.

NON ZENER VOLTAGE REFERENCE

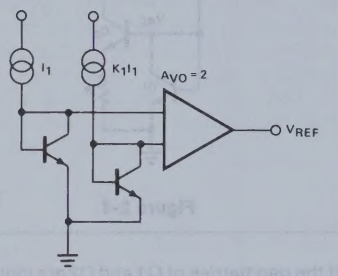


Figure 2-6

From the same considerations as before, the reference voltage can be shown to be:

$$V_{Ref} = K_2 \frac{kT}{q} I_n K_1 \qquad (2\text{-}3)$$

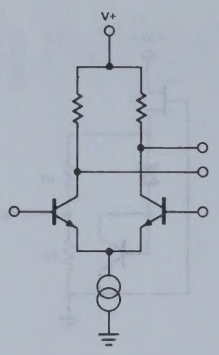
There are a number of interesting and useful properties of this circuit. Compared with a zener reference, it is much less noisy and can be used at lower supply voltages. With judicious circuit implementation, the voltage can be controlled to about ±10% and low temperature coefficients can be achieved.

CURRENT SOURCE LOADS

Using current sources for load resistors is another technique exploited in linear integrated circuit designs. The schematics of Figure 2-7 show how this may be done. The circuit shown is the simple differential amplifier. Figure 2-7a gives a conventional circuit while Figure 2-7b is an IC implementation using pnp current sources.

The value of the current source as a collector load lies in its equivalency of an extremely high resistance while occupying a very small die area. High stage gains are thus obtained in a minimum of space. Other advantages of the current source include linearity of gain versus output swing (because gain is independent of current), and large output swing capabilities. The active load circuit also has the feature of summing the gain from both output sides. The disadvantages of the circuit in Figure 2-7b are that the noise in the pnps is summed into the npn input noise, and the self-biasing scheme used in Figure 2-7b can introduce some added offset current if the pnp betas are low because pnps run at different current levels. A change in the circuit which avoids this problem is shown in Figure 2-8.

DIFFERENTIAL AMPLIFIER



Conventional Design Current Source Loads

Figure 2-7a

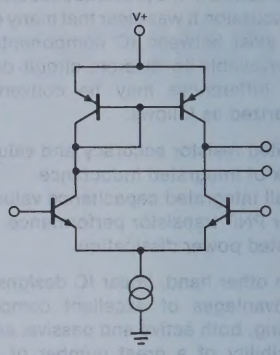


Figure 2-7b

IMPROVED DIFFERENTIAL AMPLIFIER

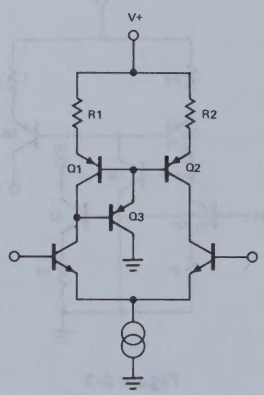


Figure 2-8

The current imbalance between Q1 and Q2 is now only:

$$I_{B_3} = \frac{2I_{C_1}}{\beta_1\beta_3} \qquad (2\text{-}4)$$

Where I_{B3} is Q3 base current I_{C1} is Q1 collector current and β_1 and β_3 are betas of Q1 and Q3 respectively. This imbalance is now negligible. Resistors have also been added to the pnp emitters to increase the output impedance and, therefore, the gain.

Use of the pnp as a collector load can be extended by using multiple collector pnps as indicated in Figure 2-9.

MULTIPLE COLLECTOR TRANSISTOR LOADS

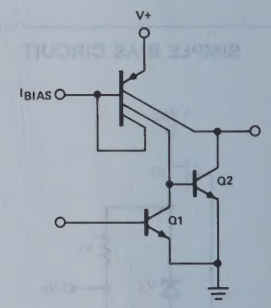


Figure 2-9

This circuit could give a voltage gain of many millions, which for linear amplification would be generally impractical due to clipping. A practical realization would incorporate feedback to define gain, as shown in Figure 2-10, where the voltage gain is given by the ratio:

$$A_V = \frac{R_F}{R_E} \qquad (2\text{-}5)$$

LEVEL SHIFTING

The necessity for level shifting arises from two general requirements:

A. Level interfacing from input to output
B. Maintaining voltages across transistor collector-base junctions to avoid clipping.

The latter situation can be seen in the circuit of Figure 2-10, where the voltage across Q1 is limited to a V_{BE} minus an IR drop which limits the voltage swing at the output. Discrete designers overcome this problem with a liberal use of coupling and decoupling capacitators which are not available to linear IC designers, unless incorporated externally.

AMPLIFIER STAGE WITH FIXED GAIN

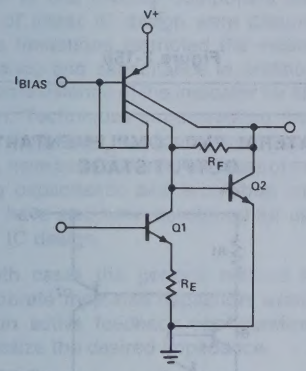


Figure 2-10

Resistive level shifting is one method used in integrated circuitry. Figure 2-11 illustrates the actual and equivalent networks.

The DC voltage is level shifted down from point A to point B through resistor R1 by the current of Q2. The circuit AC performance can be analyzed by the equivalent circuit of Figure 2-11b with the gain of the circuit being given by:

$$A_1 = \frac{Z_2}{Z_1 Z_2} \qquad (2\text{-}6)$$

Where

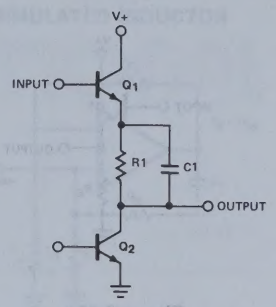
$$Z_1 = \frac{R1}{1 + j\omega R1C1} \text{ and } Z2 = \frac{R2}{1 + j\omega R2C2}$$

Maximum gain and broad bandwidth are dependent upon the following relationships:

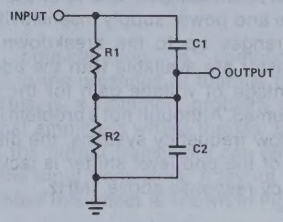
R2 >> R1 and C1 >>C2

These conditions can generally be met since the output can be fed into an emitter follower with high input resistance and low input capacitance. R2 and C2 values would be in the 5M and 0.5pF range respectively. These values place workable values of R1 and C1 at 10-20K ohms and 15-30pF respectively. Lower values of R1 consume excessive current while lower values of C1 degrade the 50MHz frequency performance.

RESISTIVE LEVEL SHIFTING



Actual Circuit



Equivalent Circuit

Figure 2-11a **Figure 2-11b**

The disadvantages of this circuit include:

A. Large die area for R1 and C1
B. Limited voltage range
C. Power consumption without gain

A level shifter which overcomes these problems is the zener diode. A reverse biased transistor emitter base junction, giving a voltage drop of 6 to 7 volts, is commonly used for the zener since the voltage is in the range generally required.

ZENER DIODE LEVEL SHIFTING

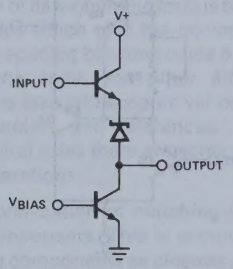


Figure 2-12

Multiples of this value can be gained by cascading more diodes. The benefits of this method are speed and small die area, while disadvantages include inflexibility to power supplies and high noise. These drawbacks restrict the use of this method to switching circuits such as comparators and sense amplifiers.

A combination of these two methods provides a circuit which provides a variable level shift. The zener of Figure 2-13 produces a constant voltage drop which is modified by resistors R1 and R2. Input to output voltage is given by:

$$V = \left(1 + \frac{R1}{R2}\right)(V_2 - V_{BE}) \qquad (2\text{-}7)$$

VARIABLE LEVEL SHIFT

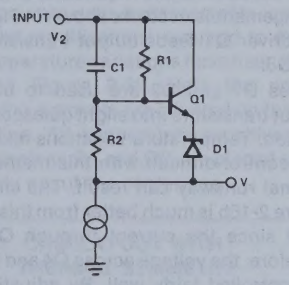


Figure 2-13

The most universally used level shifting technique, however, uses the pnp transistor. The circuit of Figure 2-10 has been redrawn to include pnp level shifters in Figure 2-14.

LEVEL SHIFT WITH PNP TRANSISTORS

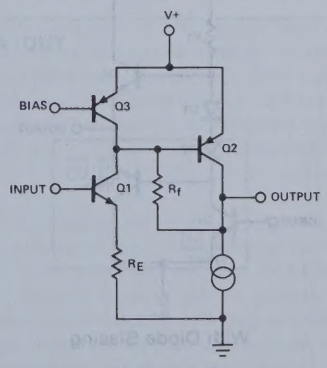


Figure 2-14

Transistors Q3 and Q4 are current source loads as described earlier. With the addition of Q2 the level shifting has been accomplished across the gain stage itself. The primary advantages are a large voltage range and power supply insensitivity. Voltage ranges up to the breakdown of the transistor are available with the additional advantage of voltage gain for the current consumed. Although not a problem in audio and low frequency systems, the disadvantage of the pnp level shifter is lack of frequency response above 1MHz.

OUTPUT STAGES

The design techniques for driven stages used in linear integrated circuits differ little from those of conventional designs. In cases where the power required is small, the conventional class A emitter follower is generally used as shown in Figure 2-15a.

The integrated form may vary in that R_E is generally replaced by a current source in the interest of smaller die size, as shown in Figure 2-15b. Where both sink and source drive capabilities are required, the npn-pnp arrangement is used. As shown in Figure 2-16a driver Q1 feeds output transistors Q2 and Q3.

Diodes D1 and D2 are used to bias the output transistors into slight quiescent conduction. Temperature variations make current control difficult with this method and thermal runaway can result. The circuit of Figure 2-16b is much better from this standpoint since the current through Q4 and, therefore, the voltage across Q4 and Q5 can be controlled fairly well. By adjusting the value of R2, the current flowing through Q2 and Q3 is likewise controlled. A further advantage of this scheme is that Q4, Q5 and R2 can be placed in the same isolation tub.

An alternative to the use of the vertical pnp is the compound npn-pnp circuit of Figure 2-17. Keeping in mind the poor frequency and phase response of the lateral pnp, the loop formed from Q3 and Q6 has the potential danger of instability, however.

CLASS A EMITTER FOLLOWER

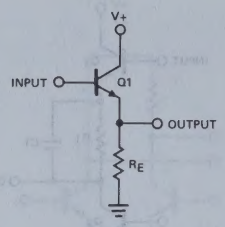


Figure 2-15a

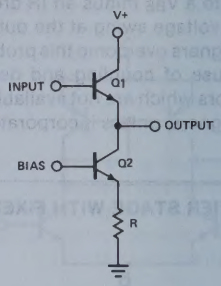
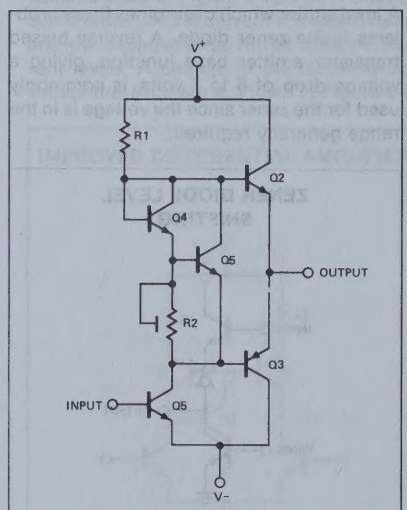


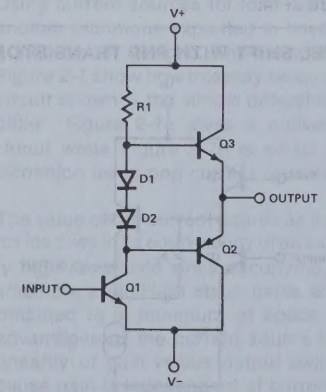
Figure 2-15b



Transistor Biasing

Figure 2-16b

COMPLEMENTARY OUTPUT STRUCTURE



With Diode Biasing

Figure 2-16a

OUTPUT PROTECTION

Output stages are commonly protected so that the maximum current available does not damage the device. A circuit achieving this is shown in Figure 2-18.

As the output current increases, the voltage drop across R1 rises sufficiently to turn on Q1, which in turn removes some base drive from Q3. The output current is thus limited to the value specified by the IR drop of R1. Currents in the negative direction are likewise limited by R2 and Q2 acting upon Q4.

LATERAL PNP COMPLEMENTARY OUTPUT STAGE

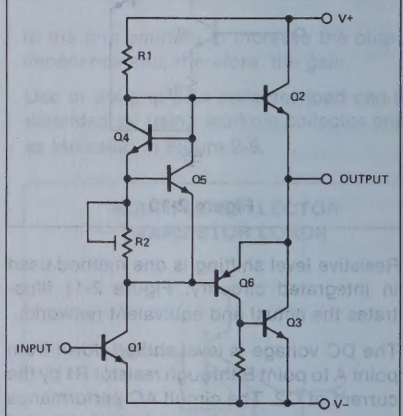


Figure 2-17

COMPLEMENTARY OUTPUT STAGE WITH SHORT CIRCUIT PROTECTION

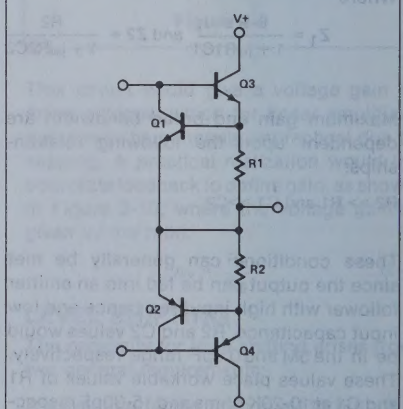


Figure 2-18

Often times the current handled by Q4 is large. If this is the case, the base drive at Q4 must be large to overcome low beta in the pnp. Hence Q2 must handle large currents to effect output protection. For this reason negative current limiting is often installed at earlier stages of a design so that smaller Q2 collector currents are required to control the output.

REACTIVE COMPONENT SIMULATION

Earlier in this chapter component limitations of linear IC design were discussed. These limitations restricted the values of resistance and capacitance in addition to the non-existence of the indicator for linear design. Techniques circumventing the resistor limitations, such as current source loads, have been covered. Methods of multiplying capacitance and simulating inductance have also been developed for use in linear IC design.

In both cases the general method is to incorporate the oxide capacitors available into an active feedback configuration to synthesize the desired impedance.

Capacitive multiplication is done using the circuit of Figure 2-19. The effective capacitance is given by the relationship:

$$C_{eff} = C_1\left(\frac{R1}{R3}\right) \qquad (2\text{-}8)$$

Values of resistance for R1 should be as high as possible since the impedance appears in series with the effective capacitance.

CAPACITANCE MULTIPLIER

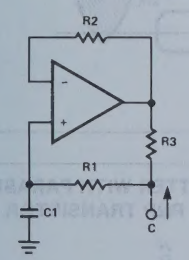


Figure 2-19

Virtual inductors can be synthesized from active devices as well. With a constant current excitation, the voltage dropped across an inductance increases with frequency. Thus an active device whose output increases with frequency can be characterized as an inductance. The circuit of Figure 2-20 yields such a response with the effective inductance being equal to:

$$L = R_1R_2C_1 \qquad (2\text{-}9)$$

SIMULATED INDUCTOR

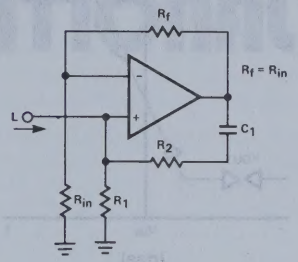


Figure 2-20

The Q of this inductance depends upon R1 being equal to R2. At this point the Q of the inductor is maximum. At the same time, however, the positive and negative feedback paths of the amplifier are equal leading to the distinct possibility of oscillation at high frequencies. R1 should therefore always be slightly smaller than R2 to assure stable operation.

LAYOUT CONSIDERATIONS

Of paramount importance to the layout of a linear circuit is the chip size. Every possible effort is made to reduce chip size for economic reasons.

In general, the transition of a circuit design to a layout of its monolithic form is by way of design rules which give the minimum and maximum spacing between oxide openings of both the same and other diffusions. These rules take into account various process parameters and tolerances. Besides these general rules there are some particular considerations.

First is optimization of matching between similar components. This is accomplished by placing components as close as possible so that the differences due to micro-variations are minimized. In the case of transistors this means placing them in adjacent isolation tubs. For resistors this means running them parallel with identical numbers of corners and with identical end-contacts.

Another consideration is component matching in the presence of thermal transients. This is a common problem with operational amplifiers where thermal transients of the output transistors can reflect back to the input transistors. A layout that could exhibit this effect is shown in Figure 2-21.

As the output drives the load, the power dissipation from output transistors Q3 and Q4 cause thermal gradients across the die. Transistors Q1 and Q2 receive a thermally generated voltage difference of 2mV per degree centigrade. Since operational amplifiers such as the NE531 have voltage gains in excess of 100dB, the voltage need only be 20-200 μV to produce output saturation.

The layout example of Figure 2-21 would generate large offset voltages as well as make accurate gain measurements impossible. The modifications required to eliminate temperature variations have been illustrated in Figure 2-22. Here the power dissipating elements are situated on the die center line. All temperature sensitive elements, such as Q1 and Q2, are placed symmetrically about the center line.

CHIP LAYOUT WITH THERMAL SYMMETRY

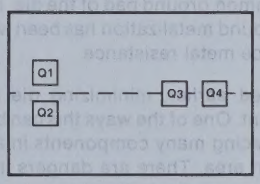
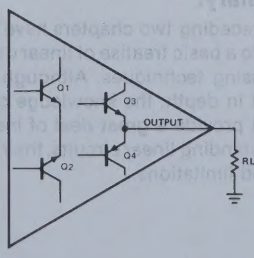


Figure 2-22

POOR THERMAL LAYOUT



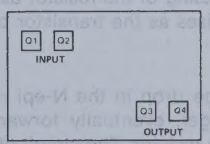


Figure 2-21

Die layout is also important with respect to ground current feedback. A good example occurs when both digital and linear circuitry appear on the same chip, as with sense amplifiers.

A functional block diagram of the sense amplifier with parasitic resistances R1 and R2 is shown in Figure 2-23. Resistors R1 and R2 represent the impedance of the die metalization.

PARASITIC RESISTANCE IN GROUND LINES

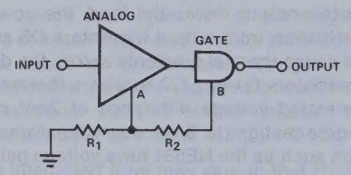


Figure 2-23

When the TTL gate output switches large ground currents occur on the gate ground leads. This transient current flows through R1 and R2, raising the voltage at points A and B. These potentials can cause positive (or negative) feedback which can alter the ideal transfer curve of Figure 2-24a to that of Figure 2-24b. Both discontinuities and hysteresis are evident.

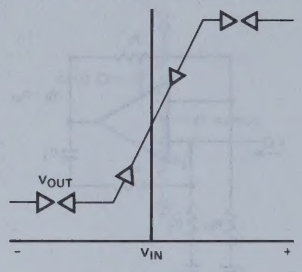
The improved method of grounding is illustrated in Figure 2-25. Ground paths have been arranged so that currents sum only at the common ground pad of the die. In addition, ground metalization has been widened to reduce metal resistance.

As stated earlier, minimizing die area is important. One of the ways this can be done is by placing many components in a single isolation area. There are dangers in doing this, however, due to the presence of parasitic components. To illustrate, the emitter follower circuit of Figure 2-26 will be used.

To save space both components are diffused in the same isolation tub as shown by Figure 2-27. The transistor collector contact serves the dual role of collector contact and reverse biasing of the resistor as required. Danger arises as the transistor current increases.

The voltage drop in the N-epi region becomes larger, eventually forward biasing part of the resistor. The circuit of Figure 2-28 applies should forward biasing occur, adding a parasitic pnp transistor between the resistor and the npn transistor base. If the beta is high enough a regenerative loop occurs causing latch up. The solution lies in locating the resistor out of the transistor current path.

SENSE AMPLIFIER TRANSFER CURVE



Ideal

Figure 2-24a

HYSTERESIS DUE TO GROUND CURRENTS

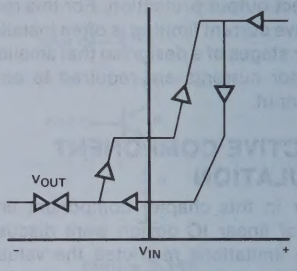


Figure 2-24b

IMPROVED SENSE AMPLIFIER LAYOUT

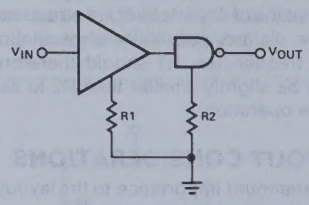


Figure 2-25

EMITTER FOLLOWER CIRCUIT

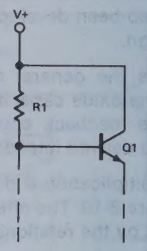


Figure 2-26

CROSS SECTIONAL OF EMITTER FOLLOWER CIRCUIT

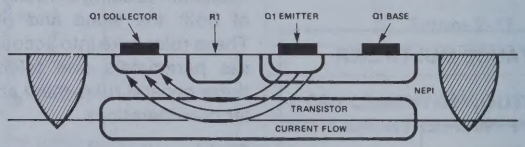


Figure 2-27

Summary:

The preceding two chapters have been devoted to a basic treatise of linear design and processing techniques. Although severely limited in depth, the knowledge presented should provide a great deal of insight into understanding linear circuits, their capabilities and limitations.

EMITTER WITH PARASITIC PNP TRANSISTOR

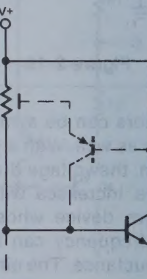
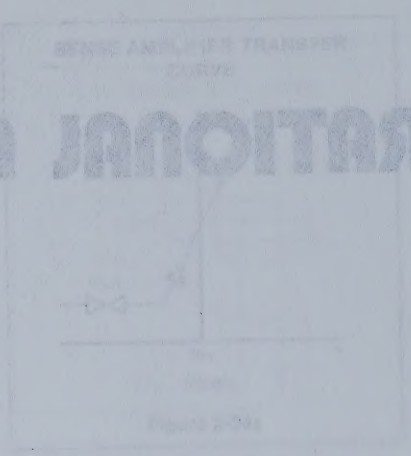
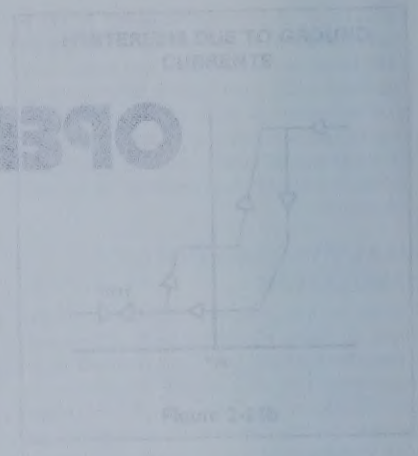
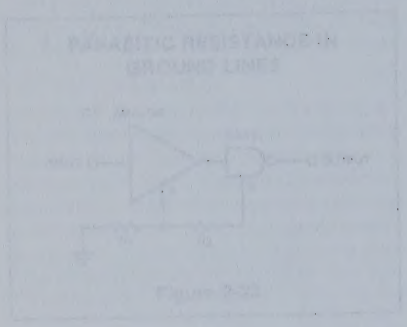


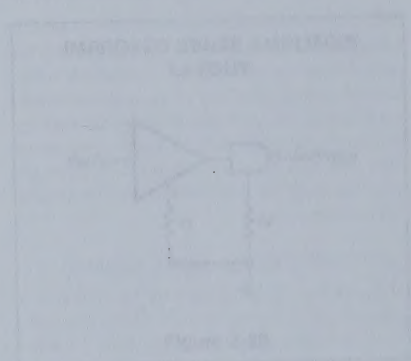
Figure 2-28

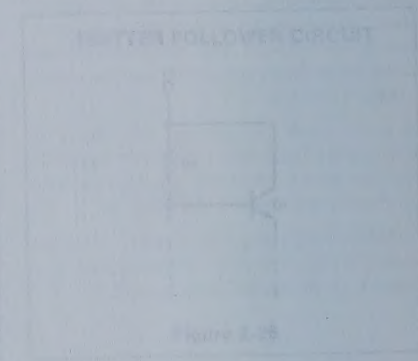
SECTION 3
OPERATIONAL AMPLIFIERS

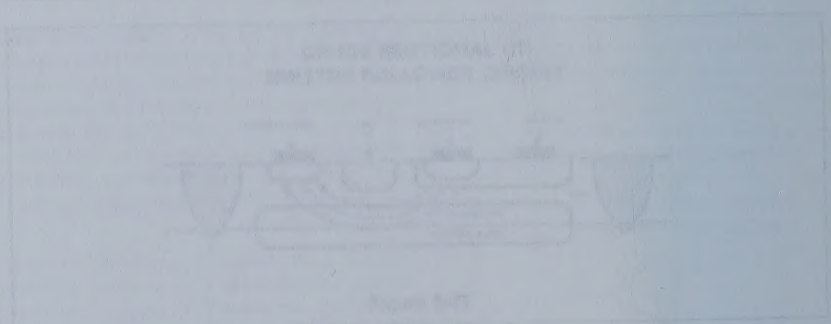

SENSE AMPLIFIER TRANSFER CURVE


INTERFERENCE DUE TO GROUND CURRENTS


PARASITIC RESISTANCE IN GROUND LINES


IMPROPER GROUND ARRANGEMENT


EMITTER FOLLOWER CIRCUIT


CROSS SECTIONAL VIEW EMITTER FOLLOWER CIRCUIT

EMITTER WITH PARASITIC PNP TRANSISTOR

INTRODUCTION

The operational amplifier was first introduced in the early 1940's. Primary usage of these vacuum tube forerunners of the ideal gain block was in computational circuits. They were fed back in such a way as to accomplish addition, subtraction, and other mathematical functions.

Expensive and extremely bulky, the operational amplifier found limited use until new technology brought about the integrated version, solving both size and cost drawbacks.

Volumes upon volumes have been and could be written on the subject of op amps. In the interest of brevity this chapter will cover the basic op amp as it is defined along with test methods and suggestive applications. Also, included is a basic coverage of the feedback theory from which all configurations can be analyzed.

THE PERFECT AMPLIFIER

The ideal operational amplifier possesses several unique characteristics. Since the device will be used as a gain block, the ideal amplifier should have infinite gain. By definition also, the gain block should have an infinite input impedance in order not to draw any power from the driving source. Additionally, the output impedance would be zero in order to supply infinite current to the load being driven. These ideal definitions are illustrated by the ideal amplifier model of Figure 3-1.

IDEAL OPERATIONAL AMPLIFIER

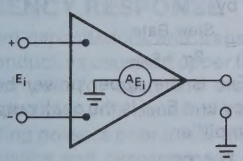


Figure 3-1

Further desirable attributes would include infinite bandwidth, zero offset voltage, and complete insensitivity to temperature, power supply variations, and common mode input signals.

Keeping these parameters in mind, further contemplation produces two very powerful analysis tools. Since the input impedance is infinite, there will be no current flowing at the amplifier input nodes. In addition, when feedback is employed the differential input voltage reduces to zero. These two statements are used universally as beginning points for any network analysis and will be explored in detail later on.

THE PRACTICAL AMPLIFIER

Tremendous strides have been made by modern technology with respect to the ideal amplifier. Integrated circuits are coming closer and closer to the ideal gain block. Input bias currents for instance are in the pA range for FET input amplifiers while offset voltages have been reduced to less than 1mV in many cases, in Bipolar devices.

Any device has limitations however, and the integrated circuit is no exception. Modern op amps have both voltage and current limitations. Peak to peak output voltage, for instance, is generally limited to one or two base-emitter voltage drops below the supply voltage while output current is internally limited to approximately 25mA. Other limitations such as bandwidth and slew rates are also present, although each generation of devices improves over the previous one.

DEFINITION OF TERMS

Earlier the ideal operational amplifier was defined. No circuit is ideal of course so practical realizations contain some sources of error. Most sources of error are very small and therefore can usually be ignored. It should be noted that some applications require special attention to specific sources of error.

Before the internal circuitry of the op amp is further explored it would be beneficial to define those parameters commonly referenced.

INPUT OFFSET VOLTAGE

Ideal amplifiers produce 0 volts out for 0 volts input. But, since the practical case is not perfect, there will appear a small dc voltage at the output even though no differential voltage is applied. This dc voltage is called the input offset voltage, with the majority of its magnitude being generated by the differential input stage pictured in Figure 3-2.

An operational amplifier's performance is in large part dependent upon the first stage. It is the very high gain of the first stage that amplifies small signal levels to drive remaining circuitry. Coincidentally, the input current, a function of beta, must be as small as possible. Collector current levels are thus made very low in the input stage in order to gain low bias currents. It is this input stage also which determines dc parameters such as offset voltage since the amplified output of this stage is of sufficient voltage levels to eclipse most subsequent error terms added by the remaining circuitry. Under balanced conditions the collector currents of Q1 and Q2 are perfectly matched, hence we may say:

DIFFERENTIAL INPUT STAGE

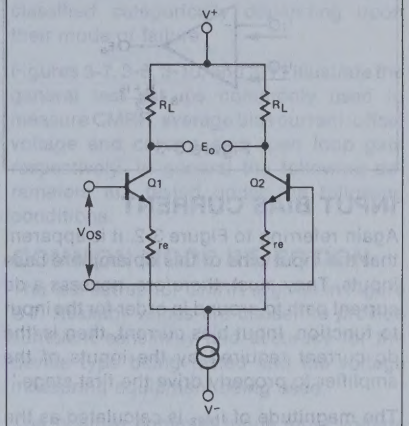


Figure 3-2

$$E_{OS} = I_{C2}R_L - I_{C1}R_L = 0 \quad (3\text{-}1)$$

In practice small differences in geometries of the base emitter regions of Q1 and Q2 will cause E_{OS} not to equal 0. Thus, for balance to be restored a small dc voltage must be added to one V_{BE} or

$$V_{OS} = V_{BE}1 - V_{BE}2 \quad (3\text{-}2)$$

where the V_{BE} of the transistor is found by

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_E}{I_s}\right) \quad (3\text{-}3)$$

Reference is made to the input when talking of offset voltage. Thus, the classic definition of input offset voltage is 'that differential dc voltage required between inputs of an amplifier to force its output to zero volts.'

Offset voltage becomes a very useful quantity for the designer because many other sources of error can be expressed in terms of V_{OS}. For instance, the error contribution of input bias current can be expressed as offset voltages appearing across the input resistors.

INPUT OFFSET VOLTAGE DRIFT

Another related parameter to offset voltage is V_{OS} drift with temperature. Present day amplifiers usually possess V_{OS} drift levels in the range of 5μV to 40μV per degree C. The magnitude of V_{OS} drift is directly related to the initial offset voltage at room temperature. Amplifiers exhibiting larger initial offset voltages will also possess higher drift rates with temperature. A rule of thumb often applied is that the drift per degree C will be 3.3μV for each millivolt of initial offset. Thus, for tighter control of thermal drift, a low offset amplifier would be selected.

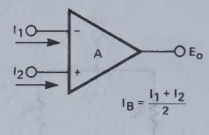


Figure 3-3

INPUT BIAS CURRENT

Again referring to Figure 3-2, it is apparent that the input pins of this op amp are base inputs. They must, therefore, possess a dc current path to ground in order for the input to function. Input bias current, then is 'the dc current required by the inputs of the amplifier to properly drive the first stage.'

The magnitude of I_{bias} is calculated as the average of both currents flowing into the inputs and is calculated from

$$I_B = \frac{I_1 + I_2}{2} \qquad (3\text{-}4)$$

Bias current requirements are made as small as possible by using high beta input transistors and very low collector currents in the first stage. The trade-off for bias current is lower stage gain due to low collector current levels and lower slew rates. The effect upon slew rate is covered in detail under the compensation section.

INPUT OFFSET CURRENT

The ideal case of the differential amplifier and its associated bias current does not possess an input offset current. Circuit realizations always have a small difference in bias currents from one input to the other, however. This difference is called the input offset current. Actual magnitudes of offset current are usually at least an order of magnitude below the bias current. For many applications this offset may be ignored but very high gain, high input impedance amplifiers should possess as little I_{os} as possible because the difference in currents flowing across large impedances develops substantial offset voltages. Output voltage offset due to I_{os} can be calculated by

$$V_{out} = A_{cl}(I_{os}R_s) \qquad (3\text{-}5)$$

Hence, high gain and high input impedances magnify directly to the output, the error created by offset current. Circuits capable of nulling the input voltage and current errors are available and will be covered later in this chapter.

INPUT OFFSET CURRENT DRIFT

Of considerable importance is the temperature coefficient of input offset current. Even though the effects of offset are nulled at room temperature, the output will drift due to changes in offset current over temperature. Many popular models now include a typical specification for I_{os} drift with values ranging in the .5nA per degree C area. Obviously those applications requiring low input offset currents also require low drift with temperature.

INPUT IMPEDANCE

Differential and common mode impedances looking into the input are often specified for integrated op amps. The differential impedance is the total resistance looking from one input to the other while common mode is the common impedance as measured to ground. Differential impedances are calculated by measuring the change of bias current caused by a change in the input voltage.

COMMON MODE RANGE

All input structures have limitations as to the range of voltages over which they will operate properly. This range of voltages impressed upon *both inputs* which will not cause the output to misbehave is called the common mode range. Most amplifiers possess common mode ranges of ±12 volts with supplies of ±15 volts.

COMMON MODE REJECTION RATIO

The ideal operational amplifier should have no gain for an input signal common to both inputs. Practical amplifiers do have some gain to common mode signals. The classic definition for common mode rejection ratio of an amplifier is the ratio the differential signal gain to the common mode signal gain expressed in dB as shown in equation 3-6a.

$$CMRR(dB) = 20 \log \frac{e_o/e_i}{e_o/e_{cm}} \qquad (3\text{-}6a)$$

The measurement CMRR as in 3-6a requires 2 sets of measurements. However, note that if e_o in equation 3-6a is held constant, CMRR becomes:

$$CMRR(dB) = 20 \log \frac{e_{cm}}{e_i} \qquad (3\text{-}6b)$$

A new alternate definition of CMRR based on 3-6b is the ratio of the change of input offset voltage to the input common mode voltage change producing it.

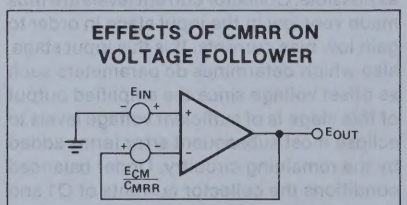


Figure 3-4

Figure 3-4 illustrates the application of the equivalent common mode error generator to the voltage follower circuit. The gain of the voltage follower with error contributions caused by both finite gain and finite common mode rejection ratio is shown in equation 3-7

$$\frac{e_o}{e_{in}} = \frac{1 \pm 1/CMRR}{1+1/A} \qquad (3\text{-}7)$$

where A equals open loop gain and is frequency dependent.

AC PARAMETERS

Parameter definition has up to this point, been dealing primarily with dc quantities of voltages, currents, etc. Several important ac or frequency dependent parameters will now be discussed.

An ideal gain block was defined earlier as one which would provide infinite gain and bandwidth. Real circuits approximate infinite open loop gain with low frequency gains in excess of 100dB. The very high gains achieved with present designs are possible only by cascading stages. Although providing very high open loop gain the cascading of stages results in the need for frequency compensation in closed loop configurations and reduces the open loop.

LARGE SIGNAL BANDWIDTH

The large signal or power bandwidth of an amplifier refers to its ability to provide its maximum output voltage swing with increasing frequency. At some frequency the output will become slew rate limited and the output will begin to degrade. This point is defined by

$$F_{PL} = \frac{\text{Slew Rate}}{2\pi \bullet E_{out}} \qquad (3\text{-}8)$$

where F_{PL} is the upper power bandwidth frequency and E_{out} is the peak output swing of the amplifier.

SLEW RATE

The maximum rate of change of the output in response to a step input signal is termed slew rate. Deviation from the ideal is caused by the limitation in frequency response of the amplifier stages and the phase compensation technique used. Summing node and amplifier output capacitances must be kept to a minimum to guarantee getting the maximum slew rate of the operational amplifier. Circuit board layout must also be of high frequency quality. Power supplies should be adequately bypassed at the pins, with both low and high frequency components to avoid possible ringing. A selection of a proper capacitor in parallel with the feedback resistor may be necessary. Too small a value could result in excessive ringing and too large a value will decrease

frequency response. In general, the worst case slew rate is in the unity gain non-inverting mode (see Figure 3-5a). Specifications of slew rate should always reflect this worst case condition with the maximum required compensation network.

AMPLIFIER SLEW RATE LIMITATIONS

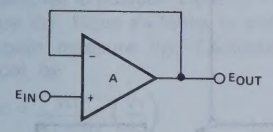


Figure 3-5a

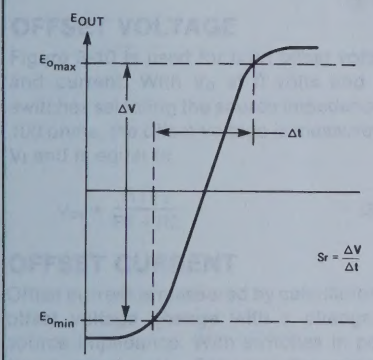


Figure 3-5b

FREQUENCY RESPONSE

Distributed capacitances and transit times in semiconductors cause an upper frequency limit or pole for each and every gain stage. Monolithic pnp transistors used for level shifting possess poor upper frequency characteristics and cascaded gain stages, used to approach the highest gain, subtract from the maximum frequency response. As shown in Figure 3-6 the open loop frequency response of the op amps shown crosses unity gain at approximately 10MHz. Closed loop response is unstable without compensation, however, so typical unity gain frequencies are readjusted by the effects of phase compensation, in this case 1MHz.

From Figure 3-6 it is also apparent that an amplifier has a trade off between gain and bandwidth. Higher gains are achieved at the expense of bandwidth. This trade off is a constant figure called the gain bandwidth product.

TEST METHODS

Product testing of integrated circuits uses automatic test equipment. Large computer controlled test decks test all data sheet limits in a matter of milliseconds. Each parameter is tested in a specific circuit configuration defined by the test hardware.

A typical simplified op amp test configuration is depicted by Figure 3-9. Units may be classed in several categories according to selected parameters. Even failures may be classified categorically depending upon their mode of failure.

Figures 3-7, 3-8, 3-10, and 3-11 illustrate the general test set ups commonly used to measure CMRR, average bias current, offset voltage and current and open loop gain respectively. In general the following parameters are tested under the following conditions.

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

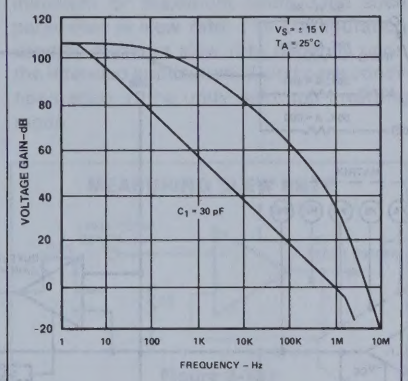


Figure 3-6

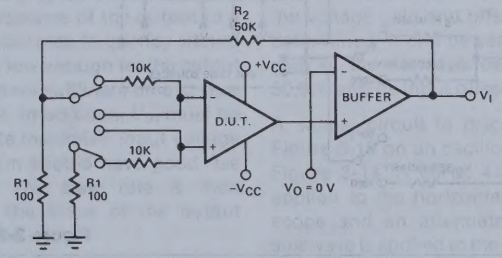
COMMON MODE REJECTION

The test set-up for CMRR is given in Figure 3-7. Resistor values are chosen to provide sufficient sensitivity and accuracy for the device type being tested and the voltage measuring equipment being used.

The positive common mode input voltage within the range V_{CM1} is algebraically subtracted from all supply voltages and from V_O. Then V_1 is measured (V_{11}). The most negative common mode voltage within the range, V_{CM2}, is then subtracted from all the supply voltages and V_O, and V_1 is again measured (V_{12}).
Then

$$CMRR = (R1 + R2)/R1\,|(V_{CM1} - V_{CM2})/V_{11} - V_{12} \quad (3\text{-}9)$$

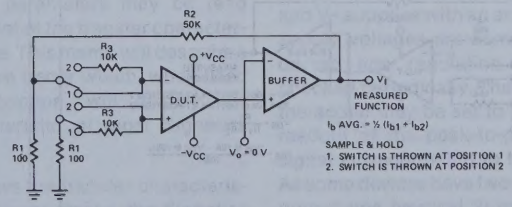
CIRCUIT DIAGRAM USED FOR CMRR MEASUREMENT



All resistor values are in ohms.

Figure 3-7

CIRCUIT DIAGRAM USED FOR AVERAGE BIAS CURRENT MEASUREMENT



All resistor values are in ohms.

Figure 3-8

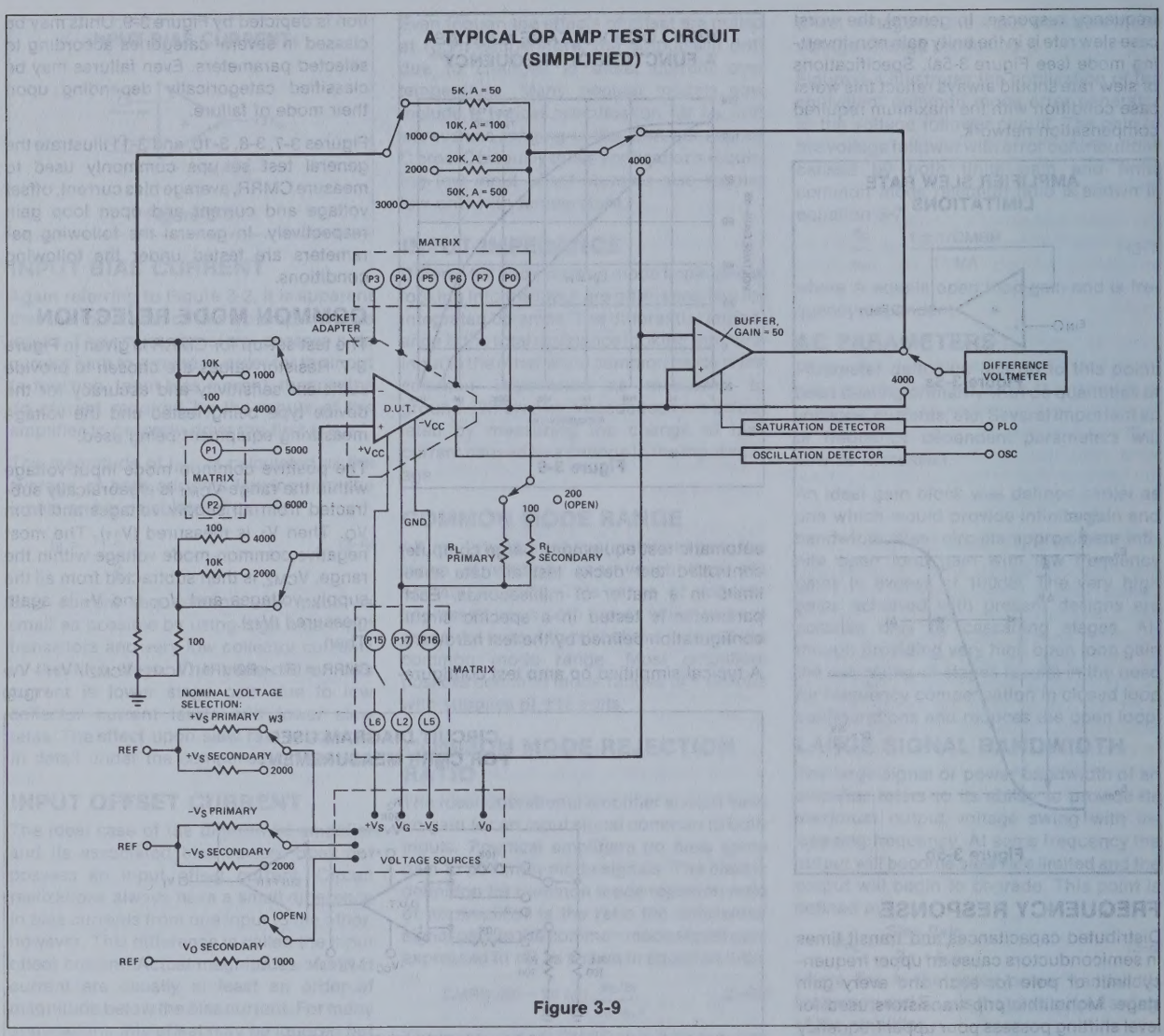
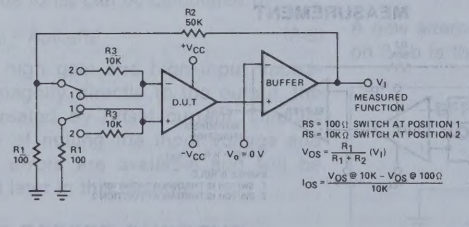


Figure 3-9

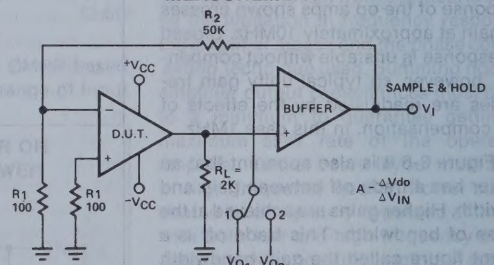
CIRCUIT DIAGRAM USED FOR OFFSET VOLTAGE AND OFFSET CURRENT



All resistor values are in ohms.

Figure 3-10

CIRCUIT DIAGRAM USED FOR LARGE-SIGNAL OPEN LOOP GAIN MEASUREMENT



All resistor values are in ohms.

Figure 3-11

This operation is equivalent to swinging both inputs over the full common mode range, and holding the output voltage constant, but it makes the V_I measurement much simpler.

BIAS CURRENT

Bias current is measured in the configuration of Figure 3-8.

With switches at position 1 and $V_O = 0$ volts, measure V_I1. Move switches to position 2 and again measure V_{I2}. Calculate I_{BIAS} (average), by

$$I_{B1} = \frac{R1}{R1 + R2}\left(\frac{V_1}{R3}\right) \quad (3\text{-}10a)$$

$$I_{B2} = \frac{R1}{R1 + R2}\left(\frac{V_1}{R3}\right) \quad (3\text{-}10b)$$

$$I_{BIAS}\ (avg) = \frac{I_{B1} + I_{B2}}{2} = \frac{R1}{R1 + R2}\,\frac{V_I1 - V_I2}{2R3} \quad (3\text{-}10c)$$

OFFSET VOLTAGE

Figure 3-10 is used for both offset voltage and current. With V_O at 0 volts and the switches selecting the source impedance of 100 ohms, the offset voltage is measured at V_I and is equal to

$$V_{os} = \frac{R1V_1}{R1 + R2} \quad (3\text{-}11)$$

OFFSET CURRENT

Offset current is measured by calculation of offset voltage change with a change in source impedance. With switches in position 1, measure V_{I2}. Calculate the contribution of I_{os} by

$$I_{os} = \frac{V_{I2} - V_1}{R3} \quad (3\text{-}12)$$

SIGNAL GAIN

The signal gain of operational amplifiers is most commonly specified for the full output swing.

This is referred to as large signal voltage gain and can be measured by the circuit of Figure 3-11. Usually specified under a specific load determined by R_L, a signal equal to the maximum swing of the output voltage is applied to V_O in both positive and negative directions. V_{I1} and V_{I2} are measured values of V_I and and V_O = maximum positive and maximum negative signals respectively. The gain of the device under test then becomes

$$A_{VO} = \left(\frac{R1 + R2}{R1}\right)\left(\frac{V_{O1} - V_{O2}}{V_{I1} - V_{I2}}\right) \quad (3\text{-}13)$$

SLEW RATE

Many other parameters are checked automatically by similar means. Only the most important ones have been covered here. Of great interest to the designer are other parameters which do not necessarily carry minimum or maximum limits. One such parameter is slew rate. The configuration used to measure slew rate depends upon the intended application. Worst case conditions arise in the unity gain non-inverting mode.

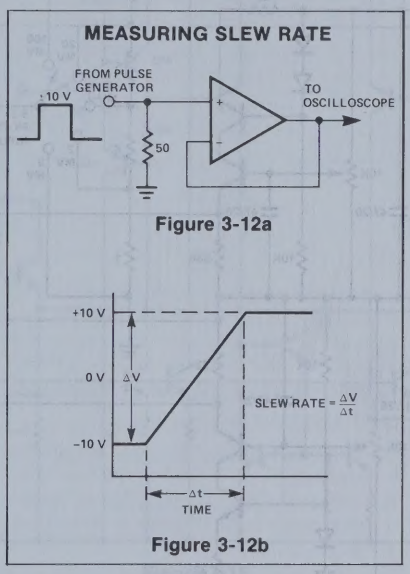


Figure 3-12a

Figure 3-12b

Figure 3-12 shows a typical bench set up for measuring the response of the output to a step input. The input step frequency should be of a frequency low enough for the output of the op amp to have sufficient time to slew from limit to limit. In addition, V_{in} must be less than absolute maximum input voltage and the wave form should have good rise and fall times. The slew rate is then calculated from the slope of the output voltage versus time or

$$SR = \frac{\Delta V_{out}}{\Delta T} \text{ in volts/}\mu s \quad (3\text{-}14)$$

OP AMP CURVE TRACER

Two of the most important parameters of linear integrated circuits having differential inputs are voltage gain and input offset voltage. These parameters may be read directly from a plot of the transfer characteristic of the device. This memo will describe a very simple curve tracer which, when used with an oscilloscope, will display the transfer characteristic of most Signetics linear devices.

Figure 3-13 shows the transfer characteristic of a typical linear device, the Signetics NE531. Note that the unit saturates at approximately +12 and -12 volts and exhibits a linear transfer characteristic between -10 and +10 volts.

From the slope of this linear portion of the transfer characteristic, and from the point

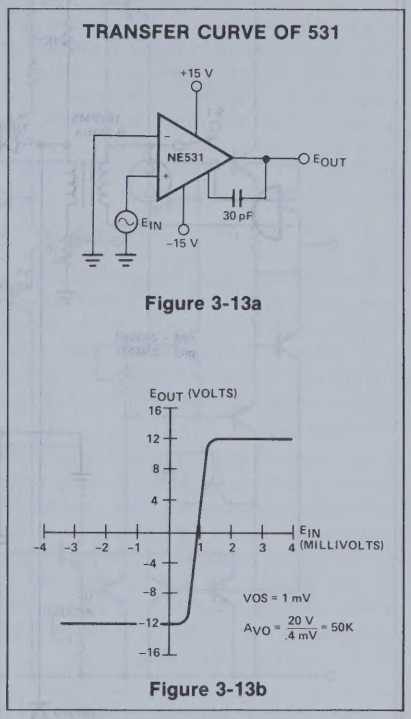


Figure 3-13a

Figure 3-13b

and +10 volts where it crosses the E_{in} axis, the voltage gain and offset voltage may be determined. It can be seen that the voltage gain of the device under test, (D.U.T.), is 50,000 and its input offset voltage is 1.0mV.

A simple circuit to display the curves of Figure 3-13 on an oscilloscope is shown in Figure 3-14. A 60Hz, 44Vp-p sinewave is applied to the horizontal input of oscilloscope and an attenuated version of the sinewave is applied to the input of the D.U.T.

The output of the D.U.T. drives the vertical input of the scope. For providing V+and V– to the D.U.T., the tester uses two simple adjustable regulators, both current limited at 25mA. Input drive to the D.U.T. may be selected by means of S-2 as shown.

To use the curve tracer, first preset the V+ and V– supplies with an accurate meter. The supply voltages are somewhat dependent on ac line regulation and should be checked periodically. The horizontal gain of the scope may be set to give a convenient readout of the peak-to-peak D.U.T. input signal corresponding to the setting of S-2. As some devices have two outputs, a second output line (vertical 2) has been provided for these devices. The transfer function of such devices will be inverted to that of Figure 3-13 of course.

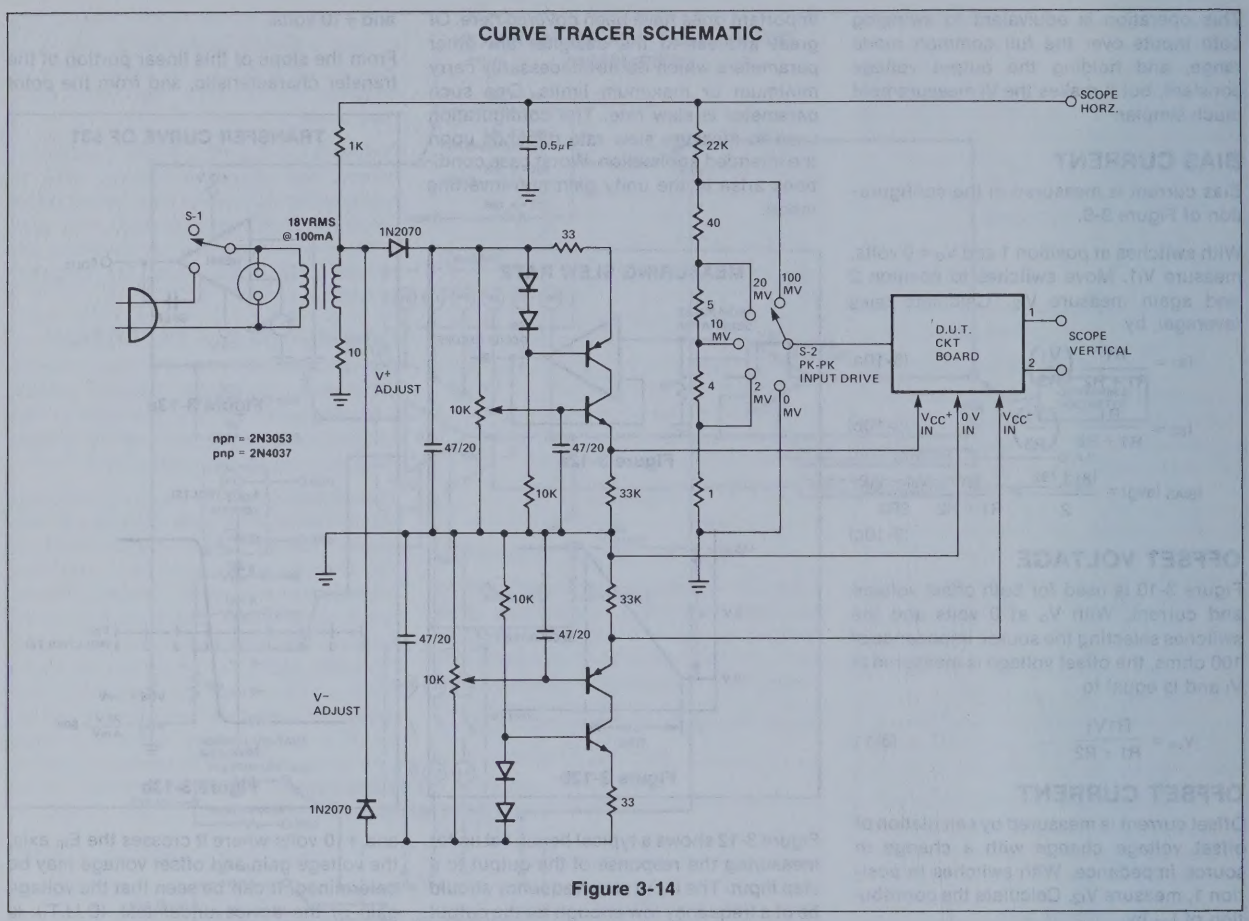


Figure 3-14

Simplicity and low cost are the two major attributes of this tester. It is not intended to perform highly rigorous tests for all devices. It is, however, a reasonably accurate means of determining the gains and offset voltages of most amplifiers. It will in addition, indicate the transfer curves of comparators and sense amplifiers with equivalent accuracies.

AMPLIFIER DESIGN

Linear operational amplifier IC's were introduced soon after the appearance of the first digital integrated circuits. The performance of these early devices, however, left much to be desired until the introduction of the 709 device. Even with its lack of short circuit protection and its complicated compensation requirements, the 709 gained real acceptance for the IC op amp. The 709 was designed using a three stage approach requiring both input and output stage compensation. In addition the output stage was not short circuit proof and the input stage latched up under certain conditions, requiring external protection.

Much better designs soon were introduced. Among the contenders were the 741, 748, 101, and 107 devices. All were general purpose devices with single capacitor compensation, (some were internally compensated), and all heralded input and output overstress protection. The basic design has two gain stages. By rolling off the frequency response of one of these, (the second stage), so that the overall gain is unity at a frequency below the point where excess phase becomes significant, the device can be stabilized for all feedback configurations. Further, by making the first stage a voltage to current converter, with a small g_m and the second stage a current to voltage converter with a high r_m, the second stage can be rolled off at 6dB octave with a small value capacitor in the order of 30pF, which can then be built into the device itself. This concept is shown in Figure 3-15.

The frequency and phase response of the pnp devices in the first stage dictate a roll off in the second stage to give a loop gain of unity at about 1.0MHz. For the unity gain feedback configuration, this implies an open loop gain of unity at this frequency. The capacitor C_c controls this parameter by looking much smaller than r_m at frequencies above a few cycles, giving a clean 6dB/octave roll off over 5 decades.

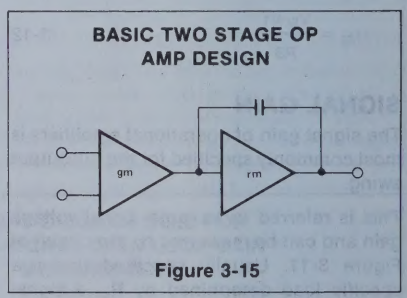


Figure 3-15

The overall gain at frequencies where the impedance of C_c dominates r_m is given by

$$A_v(\omega) = \frac{qI_{S1}}{4KT} \cdot \frac{1}{\omega Cc} \qquad (3\text{-}15)$$

Substituting the value given above, we find that a capacitance of $C_c = 30pF$ gives a unity

SCHEMATIC OF 536

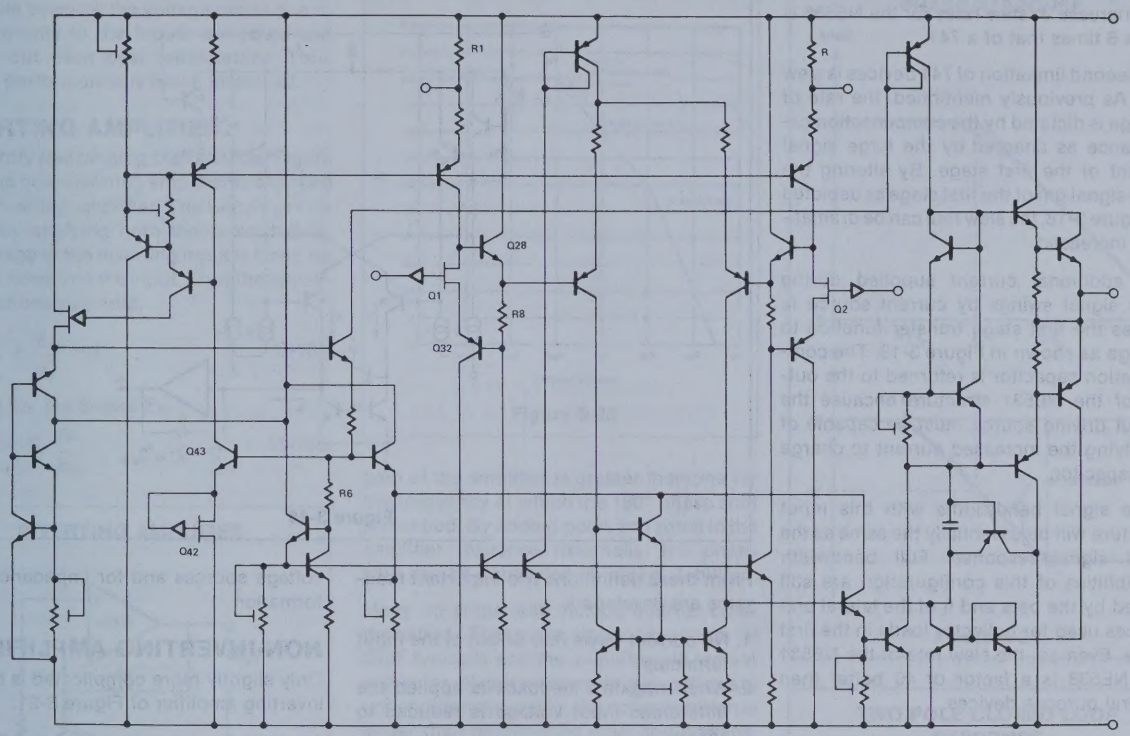


Figure 3-16

gain frequency of about 1.0MHz.

First stage large signal current also defines the slew rate for a specific compensation technique. It is this current which must charge and discharge the C_C by the expression

$$SR = \frac{dV}{dT} = \frac{I_{LS}}{C_C} \qquad (3\text{-}16)$$

where I_{LS} is the largest signal current of the input stage. Obviously, the slew rate can be improved by increasing the first stage collector current. This would, however, reflect directly upon the bias current by increasing it.

Two serious limitations, then, of these devices for diverse applications are input bias current and slew rate. Both may be overcome with small changes of the input structure to yield higher performance devices.

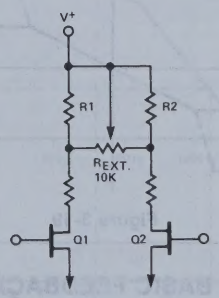
Reducing the input bias current becomes a matter of raising the transistor beta of the first stage. Several current designs boasting very low input currents use what is termed super beta input devices. These transistors have betas of 1,500 to 7,000. Bias currents under 2nA can be achieved in this way. Even though the B_{VCEO} of such transistors can be as low as 1 volt, the lower breakdowns are accounted for in the input stage by rearranging the bias technique. Bandwidths and slew rates suffer only slightly as a result of the lower current levels.

Further reduction in room temperature input bias current can be achieved by the use of FET input devices. A, (slightly simplified), schematic of the NE536 FET input op amp is given in Figure 3-16.

The majority of the 741 circuitry is preserved with the appropriate input and bias structural changes made to incorporate the junction FETs. The biasing of Q1 and Q2 is chosen to minimize offset voltage and drift. The voltage across Q1 is controlled by Q28, Q32, and R8 which is the same as that across R6 via Q42 and Q43. The operating points of Q1 and Q2 are closely controlled by the I_{DSS} of Q42 via their respective current sources. Offset adjustment is accomplished by trimming the values of R1 and R2 externally to equalize the currents through Q1 and Q2. Figure 3-17 illustrates the technique required.

FET input structures of this type can provide input bias, (gate leakage), currents on the order of 5pA at room temperature. However, unlike the input bias currents of bipolar devices, the input bias current changes rapidly with temperature, doubling in value for every 10° C rise in temperature. For high temperatures the bias current of FETs becomes only about 4 times lower than super beta structures.

OFFSET VOLTAGE ADJUSTMENT OF THE NE536



All resistor values are in ohms.

Figure 3-17

The NE536 offers the advantages of very high input impedance and higher slew rate. The increase in slew rates for the NE536 is about 6 times that of a 741.

The second limitation of 741 devices is slew rate. As previously mentioned, the rate of change is dictated by the compensation capacitance as charged by the large signal current of the first stage. By altering the large signal gm of the first stage as depicted by Figure 3-18, the slew rate can be dramatically increased.

The additional current supplied during large signal swings by current source I_4 causes the first stage transfer function to change as shown in Figure 3-19. The compensation capacitor is returned to the output of the NE531 structure because the output driving source must be capable of supplying the increased current to charge the capacitor.

Large signal bandwidths with this input structure will be essentially the same as the small signal response. Full bandwidth possibilities of this configuration are still limited by the beta and f_t of the lateral pnp devices used for collector loads in the first stage. Even so, the slew rate of the NE531 and NE538 is a factor of 40 better than general purpose devices.

INPUT STRUCTURE OF 531

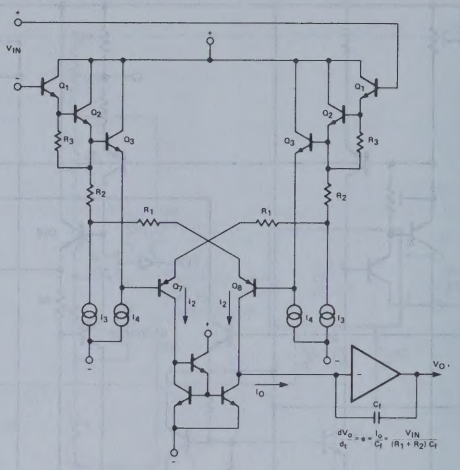


Figure 3-18

VOLTAGE/CURRENT CURVES OF FIRST STAGE

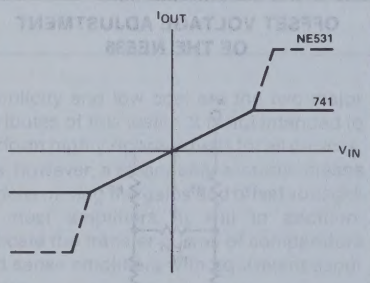


Figure 3-19

BASIC FEEDBACK THEORY

At the beginning of this chapter the ideal op amp was defined. The ideal parameters are never fully realized but they present a very convenient method for the preliminary analysis of circuitry. So important are these ideal definitions that they are repeated here. The ideal amplifier possesses:

1. Infinite gain
2. Infinite input impedance
3. Infinite bandwidth
4. Zero output impedance

From these definitions two important theorems are developed:

1. No current flows into or out of the input terminals.
2. When negative feedback is applied the differential input voltage is reduced to zero.

Keeping these rules in mind, the basic concept of feedback can be explored.

VOLTAGE FOLLOWER

Perhaps the most often used and simplest circuit is that of a voltage follower. The circuit of Figure 3-20 illustrates the simplicity.

VOLTAGE FOLLOWER

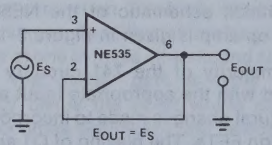


Figure 3-20

Applying the zero differential input theorem the voltages of pins 2 and 3 are equal and since pins 2 and 6 are tied together, their voltage is equal; hence, $E_{out} = E_{in}$. Trivial to analyze, the circuit nevertheless does illustrate the power of the zero differential voltage theorem. Because the input impedance is multiplied and the output impedance divided by the loop gain the voltage follower is extremely useful for buffering voltage sources and for impedance transformation.

NON-INVERTING AMPLIFIER

Only slightly more complicated is the non-inverting amplifier of Figure 3-21.

NON-INVERTING AMPLIFIER

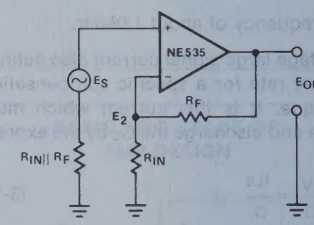


Figure 3-21

The voltage appearing at the inverting input is defined by

$$E_2 = \frac{E_{out} \bullet R_{in}}{R_F + R_{in}} \qquad (3\text{-}17a)$$

Since the differential voltage is zero, $E_2 = E_s$, and the output voltage becomes

$$E_{out} = E_s \left(1 + \frac{R_F}{R_{in}}\right) \qquad (3\text{-}17b)$$

It should be noted that as long as the gain of the closed loop is small compared to open loop gain, the output will be accurate, but as the closed loop gain approaches the open loop value more error will be introduced.

The signal source is shown in Figure 3-21 in

series with a resistor equal in size to the parallel combination of R_{in} and R_F. This is desirable because the voltage drops due to bias currents to the inputs are equal and cancel out even over temperature. Thus overall performance is much improved.

INVERTING AMPLIFIER

By slightly rearranging the circuit of Figure 3-21, the non-inverting amplifier is changed to an inverting amplifier. The circuit gain is found by applying both theorems; hence, the voltage at the inverting input is 0 and no current flows into the input. Thus the following relationships hold.

$$\frac{E_s}{R_{in}} + \frac{E_o}{R_F} = 0 \qquad (3\text{-}18a)$$

Solving for the output E_o

$$E_o \doteq -E_s \frac{R_F}{R_{in}} \qquad (3\text{-}18b)$$

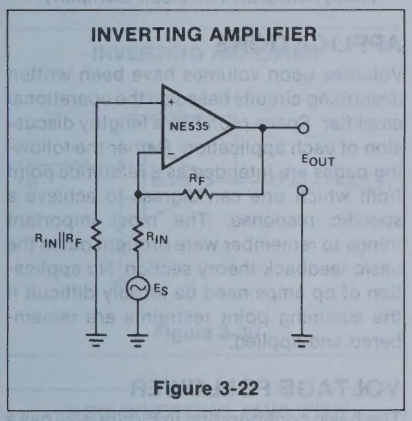


Figure 3-22

As opposed to the non-inverting circuits the input impedance of the inverting amplifier is not infinite but becomes essentially equal to R_{in}. This circuit has found widespread acceptance because of the ease with which input impedance and gain can be controlled to advantage, as in the case of the summing amplifier.

COMPENSATION

Present day operational amplifiers are comprised of multiple stages, each of which has a 3dB point or pole associated with it. Referring to Figure 3-23, the 3dB break points of a two stage amplifier are approximated by the Bode plot.

As with any feedback loop, the op amp must be protected from phase shifts in excess of 360°. A steady 180° phase shift is developed by the amplifier from output to inverting input. In addition the sum of all additional shifts due to amplifier poles or feedback component poles will cause the necessary additional 180° to sustain oscillation if the

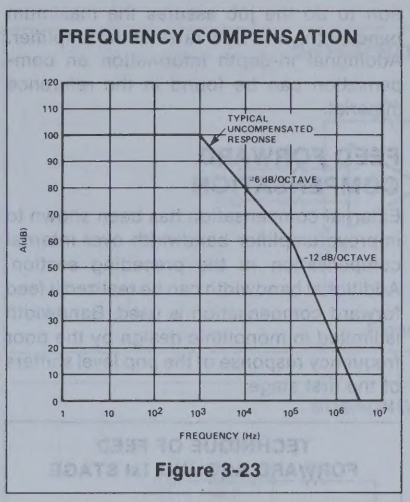


Figure 3-23

gain of the amplifier is greater than one for the frequency at which the 180° phase shift is reached. By adding poles and zeros to the amplifier response externally, the phase shift can be controlled to insure stability.

Many op amps now include internal compensation. These are single capacitors of 30pF typically and the amplifier will remain stable for all gains. However, since they are unconditionally stable, the compensation is larger than required for most applications. The resultant loss of bandwidth and slew rate may be acceptable in the general case but selection of an externally compensated device can add a great deal to the amplifier response if the compensation is handled properly.

In order to fully develop the point at which instability occurs a fuller understanding of phase response is necessary.

The diagram of Figure 3-24 depicts the phase shift of a single pole. Note that at the pole position the phase shift is 45° and that phase shift becomes 0° for a decade below the pole and -90° for a decade above the pole location. This is a Bode approximation which possesses a 5.7° error at 0° and 90° but this error is usually considered small enough to be ignored. The single pole produces a maximum of 90° phase shift and also produces a frequency roll off of 20dB per decade. The addition of the second pole of Figure 3-25 produces an additional 90° phase shift and increases the role off slope to -40dB per decade.

At this point phase shift could exceed 180° because unity gain is reached causing instability. For gain levels equal to A1 or $|1/\beta|$, the phase shift is only 90° and the amplifier is stable. However, the gain of A2 the phase shift is 180° and the loop is unstable. Gains in between A1 and A2 are

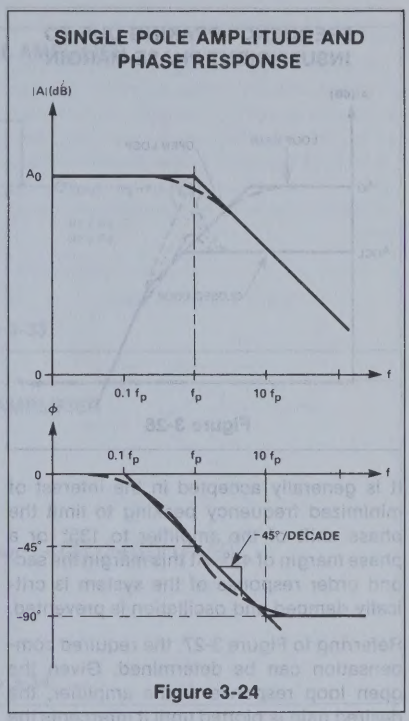


Figure 3-24

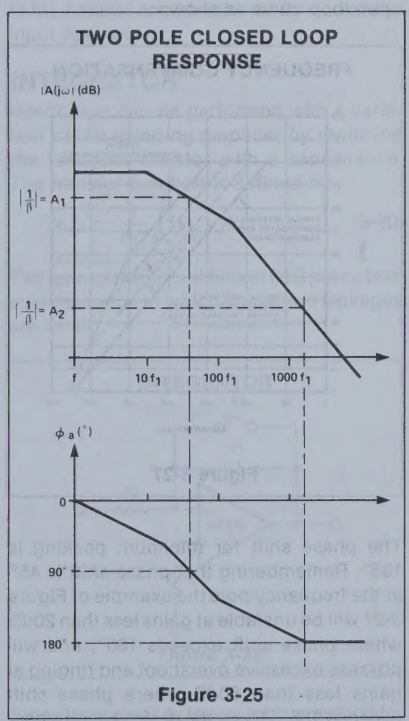


Figure 3-25

marginally stable. However, as shown in Figure 3-26 the phase shift as it approaches 180° causes increasing frequency peaking and overshoot until sustained oscillations occur.

FREQUENCY PEAKING DUE TO INSUFFICIENT PHASE MARGIN

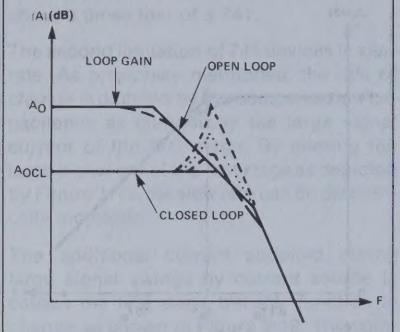


Figure 3-26

It is generally accepted in the interest of minimized frequency peaking to limit the phase shift of the amplifier to 135° or a phase margin of 45°. At this margin the second order response of the system is critically damped and oscillation is prevented.

Referring to Figure 3-27, the required compensation can be determined. Given the open loop response of the amplifier, the desired gain is plotted until it intercepts the open loop curve as shown.

FREQUENCY COMPENSATION

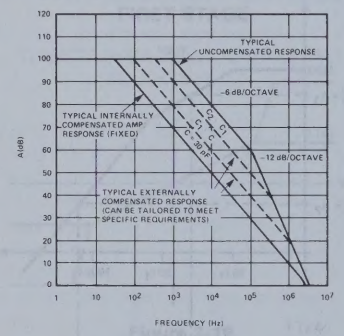


Figure 3-27

The phase shift for minimum peaking is 135°. Remembering that phase shift is 45° at the frequency pole the example of Figure 3-27 will be unstable at gains less than 20dB where phase shift exceeds 180°, and will possess excessive overshoot and ringing at gains less than 60dB where phase shift exceeds 135°. Thus, the desired compensation will move the second pole of the amplifier out in frequency until the closed loop gain intersects the open loop response before the second break of the amplifier occurs. Selecting only enough compensation to do the job assures the maximum bandwidths and slew rates of the amplifier. Additional in-depth information on compensation can be found in the reference material.

FEED FORWARD COMPENSATION

External compensation has been shown to improve amplifier bandwidth over internal compensation in the preceding section. Additional bandwidth can be realized if feed forward compensation is used. Bandwidth is limited in monolithic design by the poor frequency response of the pnp level shifters of the first stage.

TECHNIQUE OF FEED FORWARD AROUND 1st STAGE

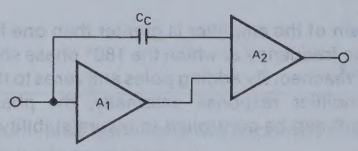


Figure 3-28a

FREQUENCY RESPONSE WITH FEED FORWARD COMPENSATION

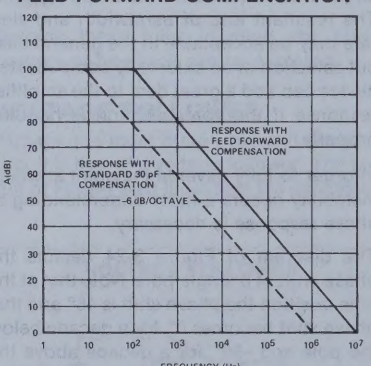
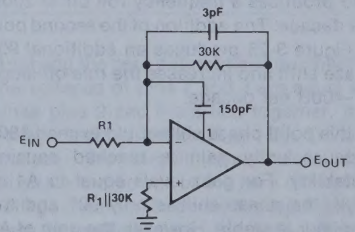


Figure 3-28b

FEED FORWARD COMPENSATION OF LM301



All resistor values are in ohms.

Figure 3-28c

The concept of feed forward compensation bypasses the input stage at high frequencies driving the higher frequency second stage directly as pictured by Figure 3-28a. The Bode plot of Figure 3-28b shows the additional response added by the feed forward technique used in Figure 3-28c. The response of the original amplifier requires less compensation at lower frequencies allowing an order of magnitude improvement in bandwidth. The typical feed forward network for the LM301 is shown in Figure 3-28c with its Bode plot in Figure 3-28b. Standard compensation and feed forward are both plotted to illustrate the bandwidth improvement. Unfortunately, the use of feed forward compensation is restricted to the inverting amplifier mode.

REFERENCES

1. *OPERATIONAL AMPLIFIERS-Design & Applications,* Jerald Graeme and Gene Tobey, McGraw Hill Book Company.

APPLICATIONS

Volumes upon volumes have been written describing circuits based on the operational amplifier. Space prohibits a lengthy discussion of each application. Rather the following pages are intended as a reference point from which one can digress to achieve a specific response. The most important things to remember were brought out in the basic feedback theory section. No application of op amps need be terribly difficult if the summing point restraints are remembered and applied.

VOLTAGE FOLLOWER

The basic configuration in Figure 3-29 has a gain of 1 with extremely high input impedance. Setting the feedback resistor equal to the source impedance will cancel the effects of bias current if desired.

VOLTAGE FOLLOWER

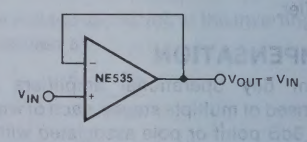


Figure 3-29

However, for most applications a direct connection from output to input will suffice. Errors arise from offset voltage, common mode rejection ratio and gain. The circuit can be used with any op amp with the required unity gain compensation, if it is required.

INVERTING AMPLIFIER

With the inverting amplifier of Figure 3-30 the gain can be set to any desired value defined by R2 divided by R1. Input impedance is defined by the value of R1, and R3 should equal the parallel combination of R1 and R2 to cancel the effect of bias current. Offset voltage, offset current, and gain contribute most of the errors. The ground may be set anywhere within the common mode range and any op amp will provide satisfactory response.

NON-INVERTING AMPLIFIER

Gain for the non-inverting amplifier is defined by the sum of R1 and R2 divided by R1.

The amplifier does not phase invert and possesses high input impedance. Again the impedances of the two inputs should be equal to reduce offsets due to bias currents.

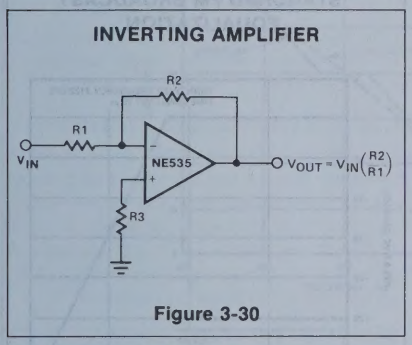


Figure 3-30

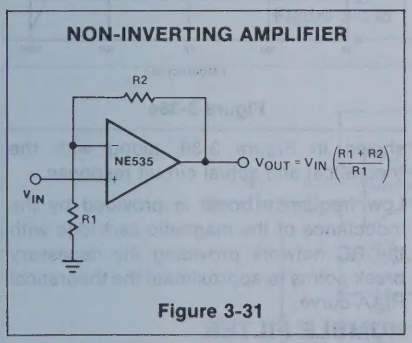


Figure 3-31

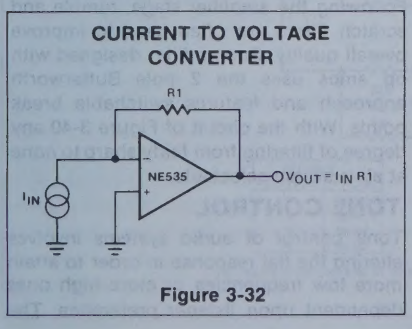


Figure 3-32

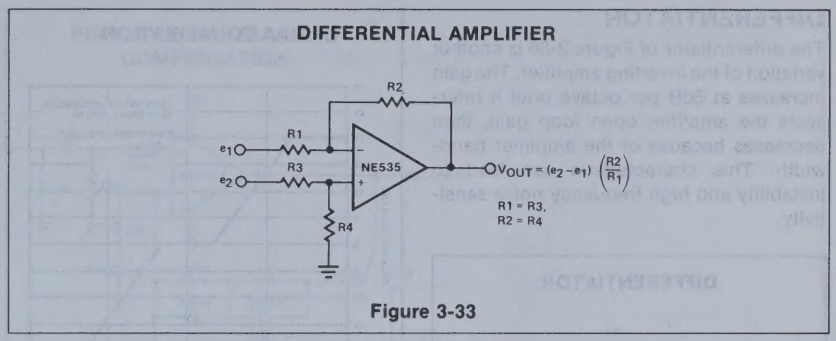


Figure 3-33

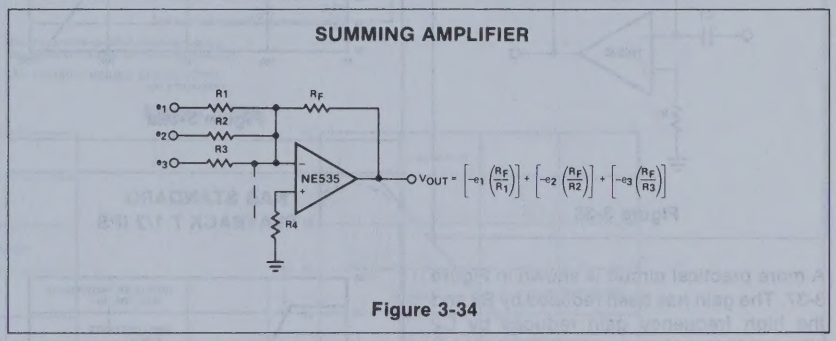


Figure 3-34

CURRENT TO VOLTAGE CONVERTER

The transfer function of the current to voltage converter is

$$V_{out} = I_n R1 \qquad (3\text{-}19)$$

Evaluation of the circuit depends upon the virtual ground theorem developed earlier. The current flowing into the input must be the same as that flowing across R1, hence, the output voltage is the IR drop of R1.

Limitations, of course, are output saturation voltage and output current capability. The inputs may be biased anywhere within the common mode range.

DIFFERENTIAL AMPLIFIER

This circuit of Figure 3-33 has a gain with respect to differential signals of R2/R1.

The common mode rejection is dominated by the accuracy of the resistors. Other errors arise from the offset voltage, input offset current, gain and common mode rejection. The circuit can be used with any op amp discussed in this chapter with the proper compensation.

SUMMING AMPLIFIER

The summing amplifier is a variation of the inverting amplifier. The output is the sum of the input voltages, each being weighed by—R_F/R_{in}.

The value of R4 may be chosen to cancel the effects of bias current and is selected equal to the parallel combination of R_F and all the input resistors.

INTEGRATOR

Integration can be performed with a variation of the inverting amplifier by replacing the feedback resistor with a capacitance. The transfer function is defined by

$$V_{out} = -\frac{1}{RC}\int_0^t V_{in} \bullet dt \qquad (3\text{-}20)$$

The gain of the circuit falls at 6dB per octave over the range in which strays and leakages are small.

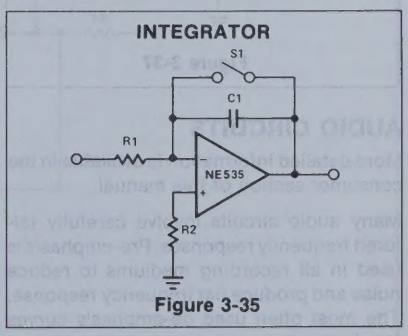


Figure 3-35

Since the gain at dc is very high a method for resetting initial conditions is necessary. Switch S1 removes the charge on the capacitor. A relay or FET may be used in the practical circuit. Bias and offset currents and offset voltage of the switch should be low in such an application.

DIFFERENTIATOR

The differentiator of Figure 3-36 is another variation of the inverting amplifier. The gain increases at 6dB per octave until it intersects the amplifier open loop gain, then decreases because of the amplifier bandwidth. This characteristic can lead to instability and high frequency noise sensitivity.

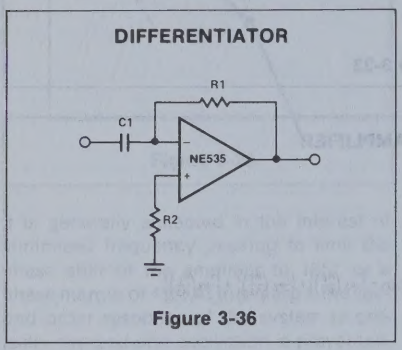


Figure 3-36

A more practical circuit is shown in Figure 3-37. The gain has been reduced by R3 and the high frequency gain reduced by C2 allowing better phase control and less high frequency noise. Compensation should be for unity gain.

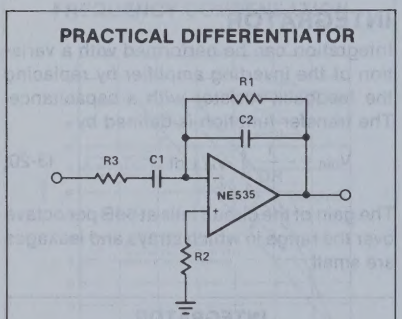


Figure 3-37

AUDIO CIRCUITS

More detailed information is available in the consumer section of this manual.

Many audio circuits involve carefully tailored frequency responses. Pre-emphasis is used in all recording mediums to reduce noise and produce flat frequency response. The most often used de-emphasis curves for broadcast and home entertainment systems are shown in Figure 3-38. Operational amplifiers are well suited to these applications because of their high gain and easily tailored frequency response.

RIAA PREAMP

The preamplifier for phono equalization is

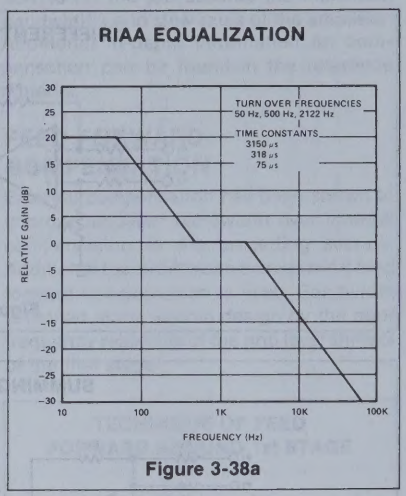


Figure 3-38a

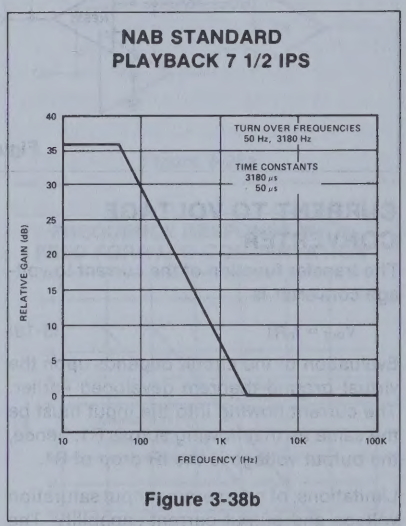


Figure 3-38b

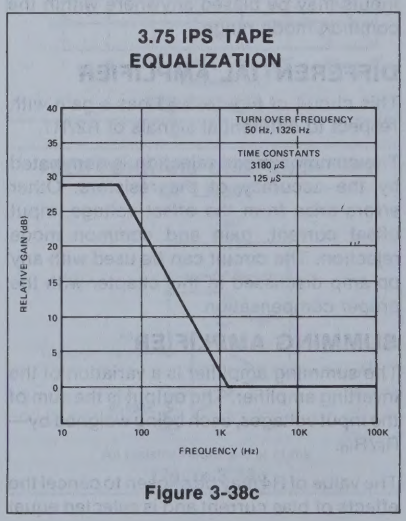


Figure 3-38c

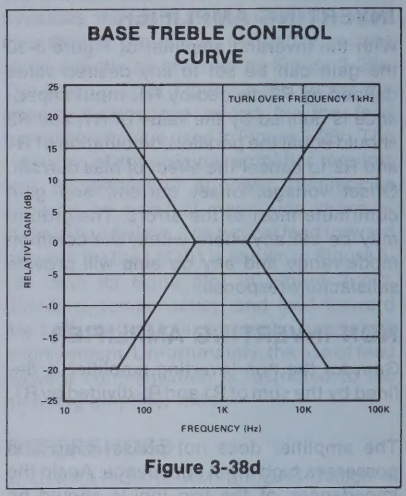


Figure 3-38d

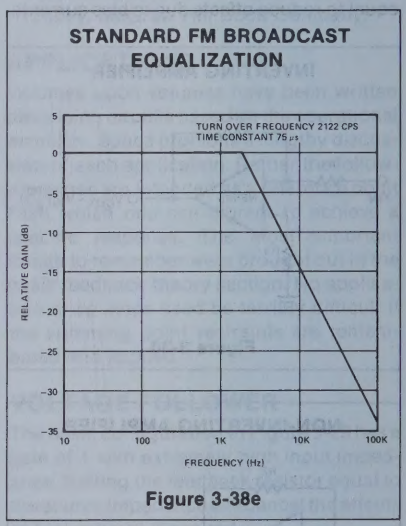


Figure 3-38e

shown in Figure 3-39, along with the theoretical and actual circuit response.

Low frequency boost is provided by the inductance of the magnetic cartridge with the RC network providing the necessary break points to approximate the theoretical RIAA curve.

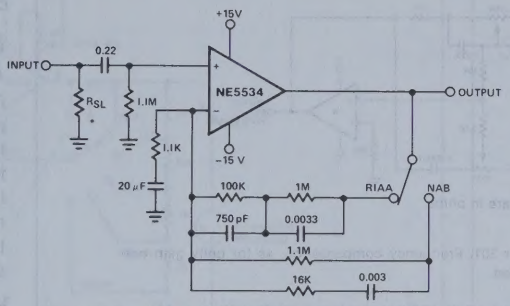
RUMBLE FILTER

Following the amplifier stage, rumble and scratch filters are often used to improve overall quality. Such a filter designed with op amps uses the 2 pole Butterworth approach and features switchable break points. With the circuit of Figure 3-40 any degree of filtering from fairly sharp to none at all is switch selectable.

TONE CONTROL

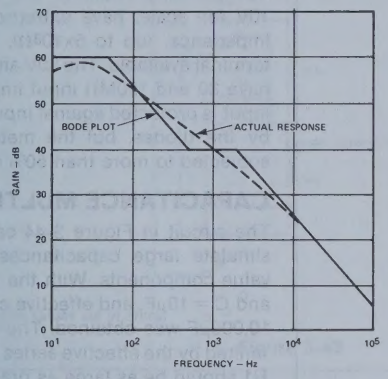
Tone control of audio systems involves altering the flat response in order to attain more low frequencies or more high ones dependent upon listener preference. The

PREAMPLIFIER—RIAA/NAB COMPENSATION



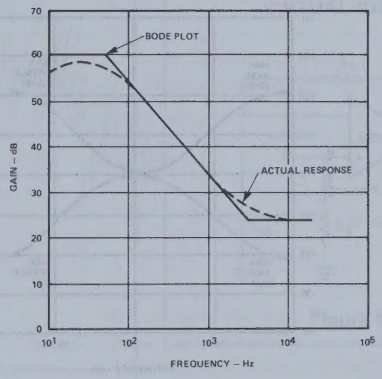
*Select to provide specified transducer loading.
Output Noise ≅ 0.8mV rms (with input shorted)
All resistor values are in ohms.

Figure 3-39a



Bode Plot of RIAA Equalization and the response realized in an actual circuit using the 531.

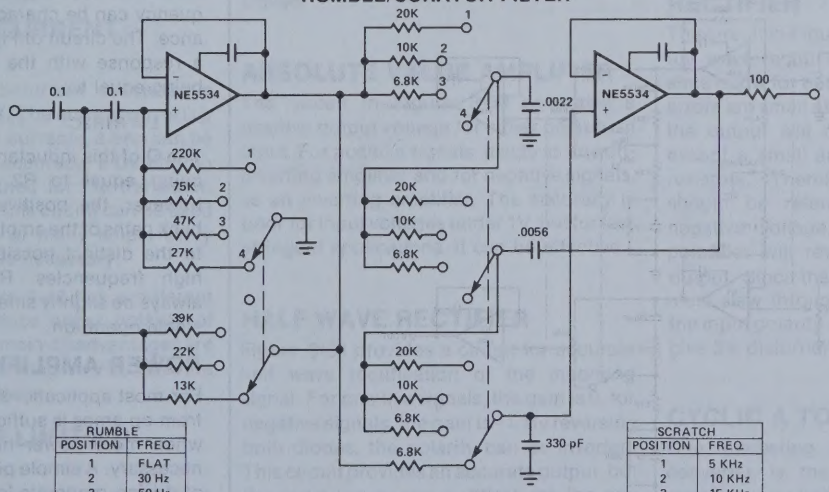
Figure 3-39b



Bode Plot of NAB Equalization and the response realized in the actual circuit using the 531.

Figure 3-39c

RUMBLE/SCRATCH FILTER



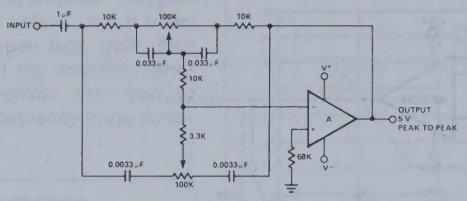
RUMBLE	
POSITION	FREQ.
1	FLAT
2	30 Hz
3	50 Hz
4	80 Hz

SCRATCH	
POSITION	FREQ.
1	5 KHz
2	10 KHz
3	15 KHz
4	FLAT

All resistor values are in ohms.

Figure 3-40

TONE CONTROL CIRCUIT FOR OPERATIONAL AMPLIFIERS



All resistor values are in ohms.

NOTES
1. Amplifier A may be a NE531 or 301. Frequency compensation, as for unity gain non-inverting amplifiers, must be used.
2. Turn-over frequency—1kHz.
3. Bass boost +20dB at 20Hz, bass cut -20dB at 20Hz, treble boost +19dB at 20kHz, treble cut -19dB at 20kHz.

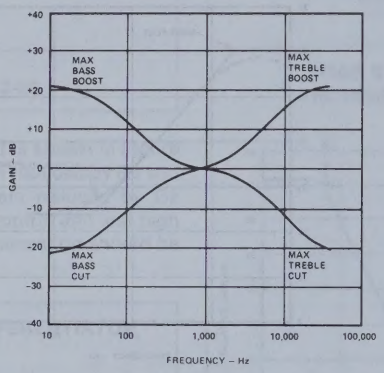
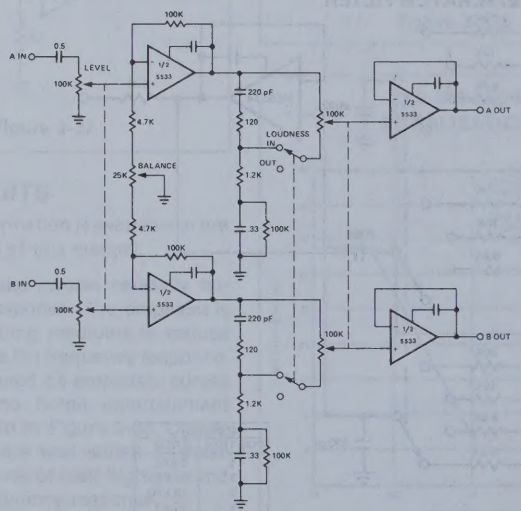


Figure 3-41

BALANCE AMPLIFIER WITH LOUDNESS CONTROL



All resistor values are in ohms.

Figure 3-42

circuit of Figure 3-41 provides 20dB of bass or treble boost or cut as set by the variable resistance. The actual response of the circuit is shown also.

BALANCE AND LOUDNESS AMPLIFIER

Figure 3-42 shows a combination of balance and loudness controls. Due to the non-linearity of the human hearing system the low frequencies must be boosted at low listening levels. Balance, level, and loudness controls provide all the listening controls to produce the desired music response.

VOLTMETER

Figure 3-43 shows a high impedance voltmeter, using the NE536 op amp as a non-inverting amplifier. The ranges, up to 10V full scale, have extremely high input impedance, (up to $5x10^8\Omega$), with a guard terminal available. The 30V and 100V scales have 30 and 100MΩ input impedance. The input is protected against input overvoltage by the diodes, but the meter cannot be subjected to more than 50% overload.

CAPACITANCE MULTIPLIER

The circuit in Figure 3-44 can be used to simulate large capacitances using small value components. With the values shown and C = 10μF, and effective capacitance of 10,000μF was obtained. The Q available is limited by the effective series resistance. So R1 should be as large as practical.

SIMULATED INDUCTOR

With a constant current exitation, the voltage dropped across an inductance increases with frequency. Thus, an active device whose output increases with frequency can be characterized as an inductance. The circuit of Figure 3-45 yields such a response with the effective inductance being equal to:

$$L = R1R2C \qquad (3\text{-}21)$$

The Q of this inductance depends upon R1 being equal to R2. At the same time, however, the positive and negative feedback paths of the amplifier are equal leading to the distinct possibility of instability at high frequencies. R1 should therefore always be slightly smaller than R2 to assure stable operation.

POWER AMPLIFIER

For most applications, the available power from op amps is sufficient. There are times when more power handling capability is necessary. A simple power booster capable of driving moderate loads is offered in Figure 3-46.

The circuit as shown uses a 741 device. Other amplifiers may be substituted only if

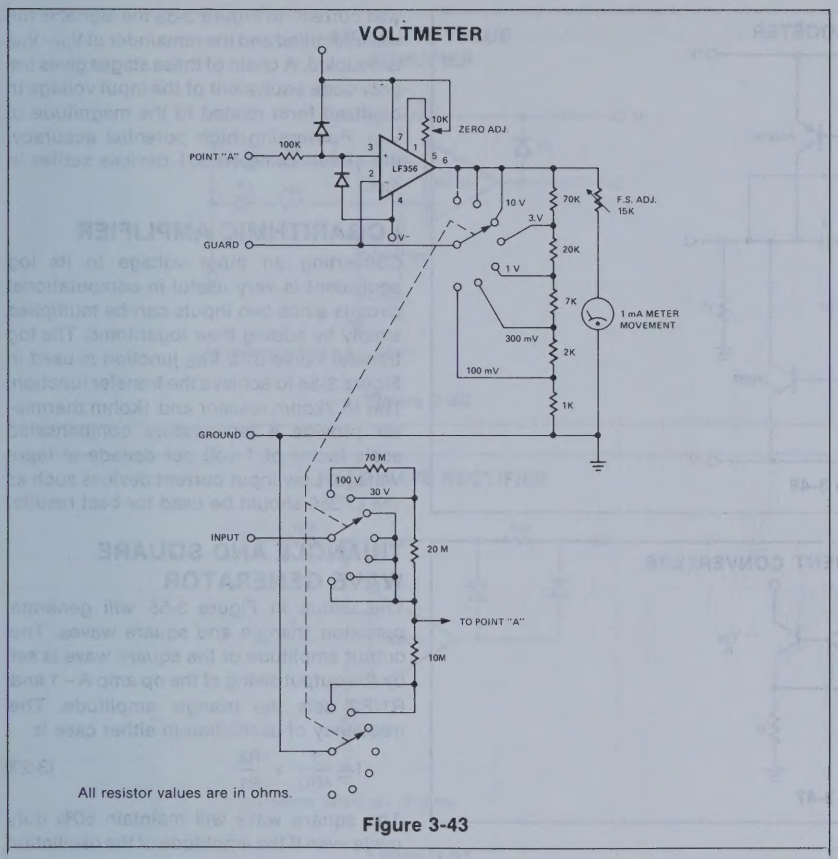


Figure 3-43

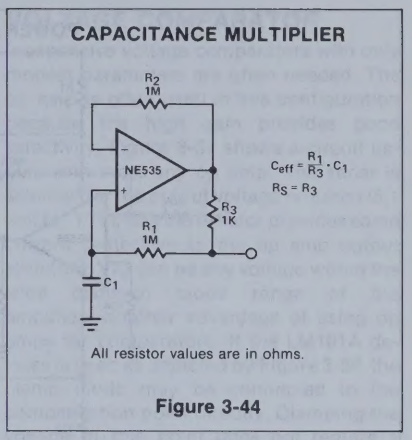


Figure 3-44

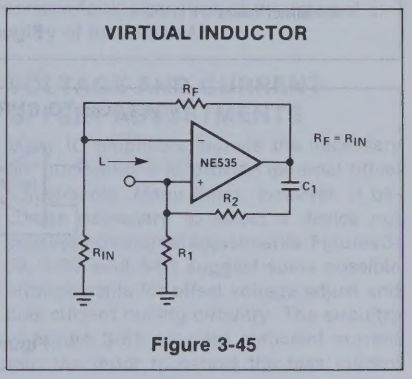


Figure 3-45

R1 values are changed because of the ICC current required by the amplifier. R1 should be calculated from the expression

$$R1 = \frac{600mV}{ICC} \qquad (3\text{-}22)$$

VOLTAGE-TO-CURRENT CONVERTERS

A simple voltage-to-current converter is shown in Figure 3-47. The current out is $I_{out} \simeq V_{in}/R$. For negative currents, a pnp can be used and for better accuracy, a Darlington pair can be substituted for the transistor. With careful design, this circuit can be used to control currents of many amps. Unity gain compensation is necessary.

The circuit in Figure 3-48 has a different input and will produce either polarity of output current. The main disadvantages are the error current flowing in R2, and the limited current available.

ACTIVE CLAMP LIMITING AMPLIFIER

The modified inverting amplifier in Figure 3-49 uses an active clamp to limit the output swing with precision. Allowance must be made for the Vbe of the transistors. The swing is limited by the base-emitter breakdown of the transistors. A simple circuit uses two back-to-back zener diodes across the feedback resistor, but tends to give less precise limiting and cannot be easily controlled.

ABSOLUTE VALUE AMPLIFIER

The circuit in Figure 3-50 generates a positive output voltage for either polarity of input. For positive signals, it acts as an non-inverting amplifier and for negative signals, as an inverting amplifier. The accuracy is poor for input voltages under 1V, but for less stringent applications, it can be effective.

HALF WAVE RECTIFIER

Figure 3-51 provides a circuit for accurate half wave rectification of the incoming signal. For positive signals, the gain is 0, for negative signals, the gain is -1. By reversing both diodes, the polarity can be inverted. This circuit provides an accurate output, but the output impedance differs for the two input polarities and buffering may be needed. The output must slew through two diode drops when the input polarity reverses. The NE535 device will work up to 10kHz with less than 5% distortion.

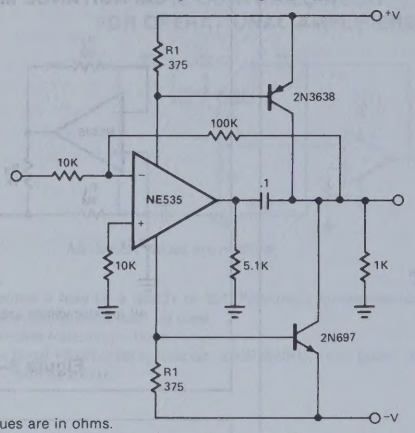
PRECISION FULL WAVE RECTIFIER

The circuit in Figure 3-52 provides accurate full wave rectification. The output impedance is low for both input polarities, and the errors are small at all signal levels. Note that the output will not sink heavy currents, except a small amount through the 10kΩ resistors. Therefore, the load applied should be referenced to ground or a negative voltage. Reversal of all diode polarities will reverse the polarity of the output. Since the outputs of the amplifiers must slew through two diode drops when the input polarity changes, 741 type devices give 5% distortion at about 300Hz.

CYCLIC A TO D CONVERTER

One interesting, but, much ignored A/D converter is the cyclic converter. This consists of a chain of identical stages, each of which senses the polarity of the input. The stage then subtracts V_{ref} from the input and doubles the remainder if the polarity

POWER BOOSTER



All resistor values are in ohms.

Figure 3-46

VOLTAGE TO CURRENT CONVERTERS

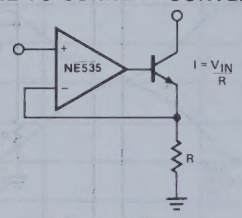


Figure 3-47

VOLTAGE TO CURRENT CONVERTER

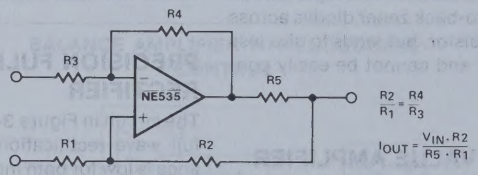


Figure 3-48

ACTIVE CLAMP LIMITING AMPLIFIER

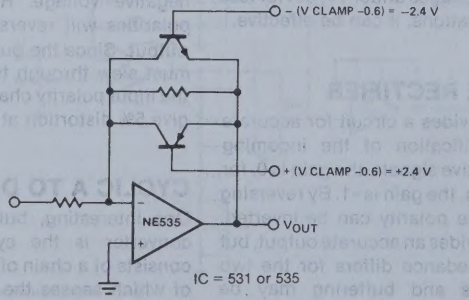


Figure 3-49

was correct. In Figure 3-53 the signal is full wave rectified and the remainder of $V_{in} - V_{ref}$ is doubled. A chain of these stages gives the gray code equivalent of the input voltage in digitized form related to the magnitude of V_{ref}. Possessing high potential accuracy, the circuit using NE531 devices settles in 5μs.

LOGARITHMIC AMPLIFIER

Converting an input voltage to its log equivalent is very useful in computational circuits since two inputs can be multiplied simply by adding their logarithms. The log transfer curve of a V_{BE} junction is used in Figure 3-54 to achieve the transfer function. The 15.7kohm resistor and 1kohm thermistor provide a temperature compensated scale factor of 1 volt per decade of input voltage. Low input current devices such as the LF356 should be used for best results.

TRIANGLE AND SQUARE WAVE GENERATOR

The circuit in Figure 3-55 will generate precision triangle and square waves. The output amplitude of the square wave is set by the output swing of the op amp A - 1 and R1/R2 sets the triangle amplitude. The frequency of oscillation in either case is

$$f = \frac{1}{4RC} \cdot \frac{R2}{R1} \qquad (3\text{-}23)$$

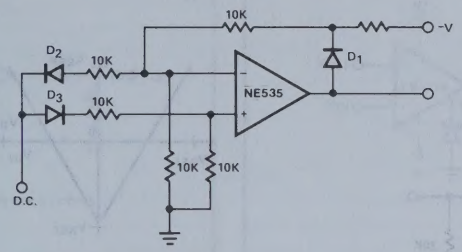
The square wave will maintain 50% duty cycle even if the amplitude of the oscillation is not symmetrical.

The use of the NE531 in this circuit will allow good square waves to be generated to quite high frequencies. Since the amplifier A1 runs open loop, there is no need for compensation. The triangle-generating amplifier must be compensated.The NE5535device can be used as well, except for the lower frequency response.

TWO-PHASE SINE WAVE OSCILLATOR

This circuit (referring to Figure 3-56), uses a 2-pole pass Butterworth filter, followed by a phase shifting single pole stage, fed back through a voltage limiter to achieve sine and cosine outputs. The values shown using 741 amplifiers give about 1.5% distortion at the sine output and about 3% distortion at the cosine output. By careful trimming of C_G and/or the limiting network, better distortion figures are possible. The component values shown give a frequency of oscillation of about 2kHz. The values can be readily selected for other frequencies. The NE535 should be used at higher frequencies to reduce distortion due to slew limiting.

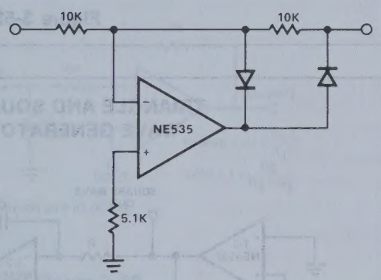
ABSOLUTE VALUE AMPLIFIER



All resistor values are in ohms.

Figure 3-50

HALF WAVE RECTIFIER



All resistor values are in ohms.

Figure 3-51

PRECISION FULL WAVE RECTIFIER

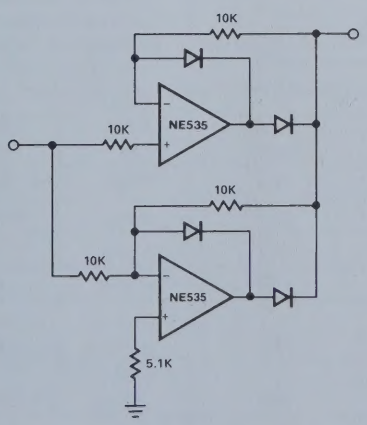


Figure 3-52

VOLTAGE COMPARATOR

Inexpensive voltage comparators with only modest parameters are often needed. The op amp is often used in this configuration because the high gain provides good selectivity. Figure 3-57 shows a circuit usable with most any op amp. The zener is selected for the output voltage required (5.1 volt for TTL), and the resistor provides some current protection to the op amp output structure. V_{ref} can be any voltage within the wide common mode range of the amplifier—another advantage of using op amps for comparators. If the LM101A devices is used as depicted by Figure 3-58, the clamp diode may be connected to the compensation point directly. Clamping the voltage at this point does not require a series resistor because of the internal circuitry of the LM101A.

VOLTAGE AND CURRENT OFFSET ADJUSTMENTS

Many IC amplifiers include the necessary pin connections to provide external offset adjustments. Many times, however, it becomes necessary to select a device not possessing external adjustments. Figures 3-59, 3-60, and 3-61 suggest some possible arrangements for offset voltage adjust and bias current nulling circuitry. The circuitry of Figure 3-61 provides sufficient current into the input to cancel the bias current requirement. Although more simplified arrangements are possible the addition of Q2 and Q3 provide a fixed current level to Q1, thus, bias cancellation can be provided without regard to input voltage level.

THE LF 156, IMPROVED FET OP AMP

Introduction

Advanced analog processing at Signetics has led to the improved JFET input op amp. The LF156 incorporates well-matched, high-voltage JFET's on the same chip with bipolar transistors. The design gives low voltage and current noise and a low I/f noise corner. Specific applications which can utilize the advanced characteristics of the LF156 follow:

Applications

A change in capacitance must cause a change in charge, and that charge is displaced into the summing point, which must be balanced by an equivalent displacement of charge across the feedback capacitor, C_f, caused in turn by a change in the output voltage e. This circuit has the desirable property of being virtually independent of shunt capacitance across the

CYCLIC A TO D CONVERTER

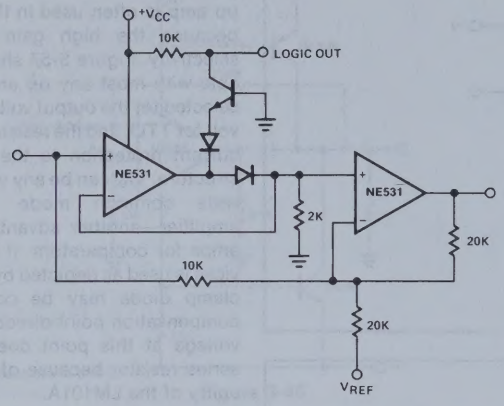


Figure 3-53a

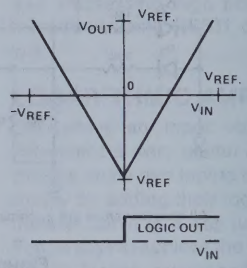
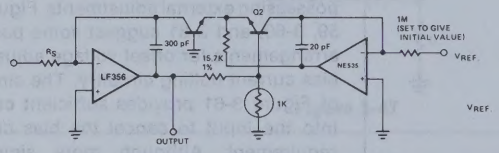


Figure 3-53b

LOGARITHMIC AMPLIFIER



All resistor values are in ohms.

Figure 3-54

TRIANGLE AND SQUARE WAVE GENERATOR

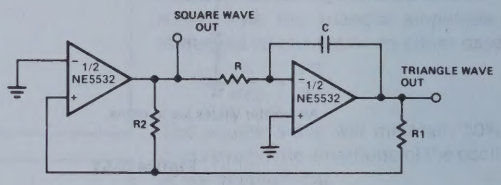
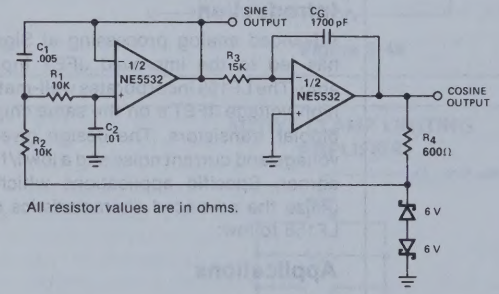


Figure 3-55

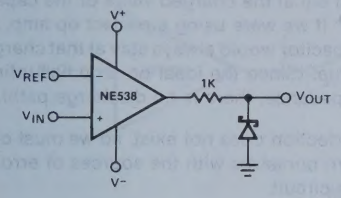
TWO-PHASE SINE WAVE OSCILLATOR



All resistor values are in ohms.

Figure 3-56

VOLTAGE COMPARATOR



All resistor values are in ohms.

Figure 3-57

VOLTAGE COMPARATOR

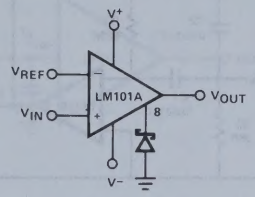
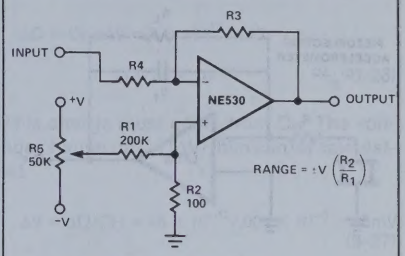


Figure 3-58

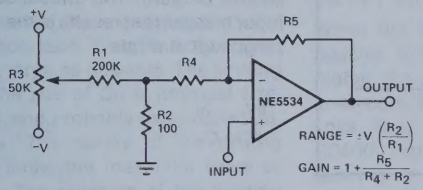
UNIVERSAL OFFSET NULL FOR INVERTING AMPLIFIERS



All resistor values are in ohms.

Figure 3-59

UNIVERSAL OFFSET NULL FOR NONINVERTING AMPLIFIERS



All resistor values are in ohms.

Figure 3-60

BIAS CURRENT COMPENSATION

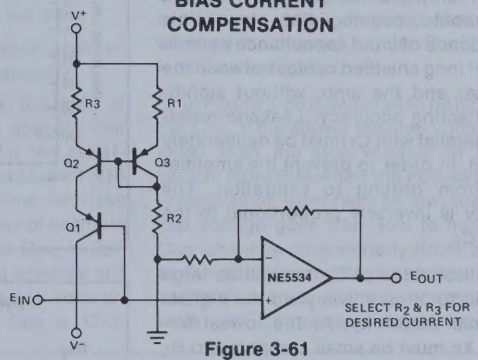


Figure 3-61

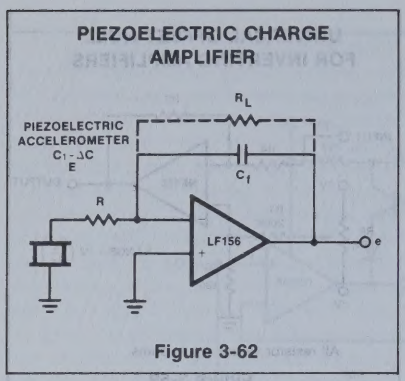


Figure 3-62

input, since such capacitance is connected from the summing point to ground, and has across it only the residual null voltage, which should be negligibly low. This independence of input capacitance permits the use of long shielded cables between the transducer and the amp, without significantly affecting accuracy. Leakage resistance in parallel with C_f must be deliberately sustained, in order to prevent the amplifier output from drifting to saturation. The sensitivity is inversely proportional to the value of C_f.

The smallest value of C_f that will be large compared to "strays" will yield the highest predictable sensitivity. At the lowest frequency, Xc must be small compared to R_L and the op amp's offset current is sufficiently small to prevent saturation with the required value of R.

Another application for which the LF156 is well suited is the high frequency, high impedance active filter. An example follows:

Other applications for the LF156 include: high impedance buffers, wideband low noise low drift amplifiers, precision high speed integrators, sample and hold circuits and fast D/A and A/D converters.

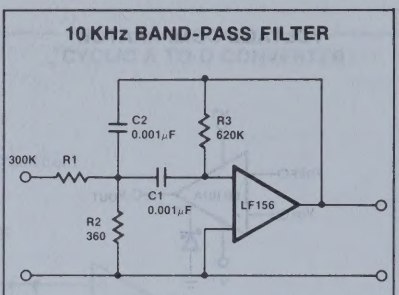


Figure 3-63a

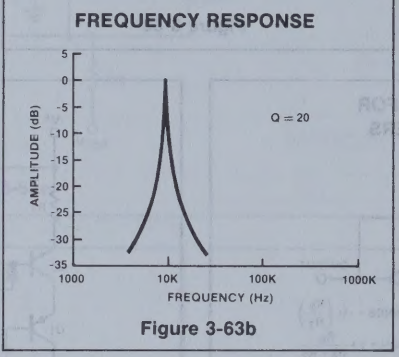


Figure 3-63b

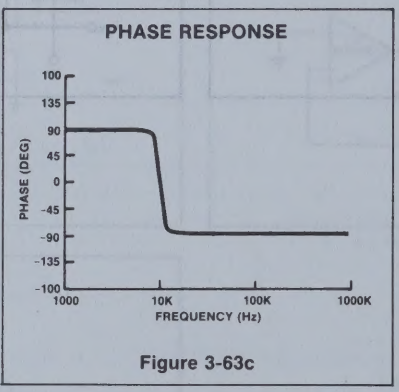


Figure 3-63c

DESIGNING A SAMPLE & HOLD CIRCUIT

Ideally, a sample and hold circuit is designed to operate in two basic states. In the first, or sample, state, an input signal is applied to the circuit. The output will follow the input. In the second, or hold, state, the output will remain constant at a value equal to the input when it went to the hold state. The output will stay at that value for an indefinite period of time, independent of any change on the input.

Generally the sample and hold circuit consists of a driver (A_1), a switch (S_1), a capacitor (C_H) and an output buffer (A_2). The basic operation of such a circuit is shown in Figure 3-64. With S closed, the output will follow the input. Note that the capacitor also follows the input. When S is open, the output will equal the charged value of the capacitor. If we were using a perfect op amp, the capacitor would always stay at that charged value. (Since the ideal op amp has infinite impedance, there is no discharge path).

Perfection does not exist, so we must concern ourselves with the sources of error in the circuit.

Output Buffer

To begin, let's examine the effects of a non-perfect output op amp (A_2). As stated earlier, when the switch (S_1) is open, the only discharge path for the capacitor is into the output buffer. The input bias current for A_2 should be zero. The effects of a non-zero input bias current results in the output dropping (sag) at a rate

$$\frac{dV}{dT} = \frac{I_B}{C_H} \qquad (3\text{-}24)$$

where I_B = Input bias current
C_H = Holding capacitor

By way of comparison, Table 3-1 demonstrates the effects of I_B on the output sag for various types of op amps.

As you can see by Table 3-1, the FET input op amps are far superior in sample and hold applications. Another observation is that the I_B for a FET input op amp increases considerably with an increase in temperature. As a rule of thumb, the input bias of a FET input op amp doubles for every 10°C temperature rise. To minimize the effect of temperature variations, it is recommended

Operational Amplifier	Type Input	Worst Case I_B	dV/dT CH = .1μF	dV/dT CH = 1.0μF
LF155A	FET	50pA	500μV/s	50μV/s
LF355A	FET	50pA	500μV/s	50μV/s
LF155/255	FET	100pA	1000μV/s	100μV/s
uA740C	FET	2nA	20mV/s	2mV/s
LF355A at 70°C	FET	5nA	50mV/s	5mV/s
LF155A at 125°C	FET	25nA	250mV/s	25mV/s
LM107	Bipolar	75nA	750mV/s	750mV/s
LM101A	Bipolar	500nA	500mV/s	5V/s

Table 3-1

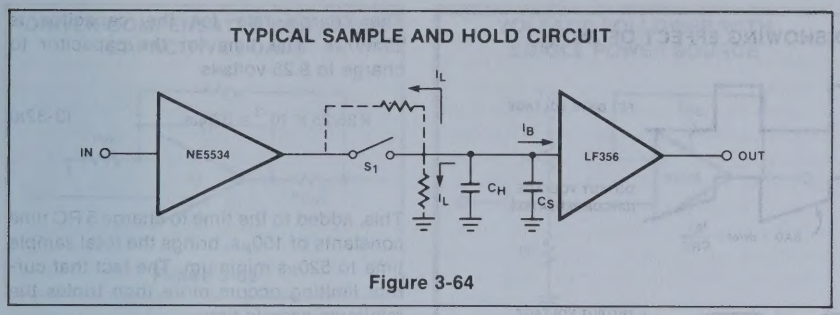


Figure 3-64

that the FET input op amp be used with a heat sink. This will reduce the function temperature change and minimize I_B increases.

Even with this increasing I_B with temperature, the FETs are better than most bipolar types. Compare the I_B values of the LF155A at 125°C with the LM107 at 25°C. It can be seen by Table 3-1 that as the value of capacitance is increased, the sag during the holding time is decreased. Thus the holding cap should be as large as possible. The limiting factors for the size of C_H is physical size, cost, leakage, and, probably most important, sample time. The ability of the driving source also limits the maximum value of capacitance. The qualities of the holding capacitor that are most important are minimum leakage and no dielectric polarization. For large capacitors teflon, polyethylene and polycarbonate dielectrics should be used. With small capacitor values, glass or silvered mica capacitors work well.

Leakages

Any leakage path for the holding cap will have the same effect as I_B and add to the dV/dT of the output. The board layout for the circuit should keep a minimum distance from the switch to the holding cap and input to the buffer amp. Drain to source leakage current in a FET switch is another source of possible droop in the output. For D-MOS FET switches (SD210-215 and SD5000 series) this leakage is typically *1nA. The total droop or dV/dT then becomes

$$dV/dT = \frac{I_B + I_L}{C_H + C_S} \qquad (3\text{-}25)$$

where I_B = Input bias current
I_L = Leakage currents
C_H = Holding capacitor
C_S = Stray capacitance

In reality, C_S is usually so small compared to C_H that its effects are negligible. The leakage currents generally do not total more than 1nA and can be minimized.

Switching Errors

The leakage of the switch is not the only source of error generated by the FET. The drain to gate capacitance of the FET can in some cases cause more than 100% of the total output error. The switch, generally, is connected with the drain toward the holding capacitor and the source to the driver. This drain to gate capacitance (C_{DG}) is a function of the voltage difference between source and drain and the voltage on the gate.

Figure 3-65 shows the capacitance model of the FET with the holding capacitor.

When the FET switch is on, the gate is positive with respect to the source. The higher the potential, the lower the resistance path (i.e., with V_{GS} in excess of +10 volts, R_{ON} is typically 30 ohms with the SD5000 series of switch.) By way of example (see Figure 3-65), assume that C_{DG} is 3pF and C_H is .001μF. C_H is holding a charge of 3 volts. With the switch on, and +15 volts on the gate, the potential across C_{DG} is (15-3) 12V. When the switch turns off, the voltage on the gate changes 15V. Thus the capacitance takes a charge (ΔQ). This charge

$$\Delta Q = C_{DG}\Delta V = 3 \times 10^{-12} \times 15$$

$$Q = 45 \times 10^{-12} \qquad (3\text{-}26)$$

This charge must come from C_H. The voltage change on C_H (ΔV) then can be calculated.

$$\Delta V = \Delta Q/CH = 45 \times 10^{-12}/.001 \times 10^{-6} = 45mV \qquad (3\text{-}27)$$

The voltage output drops 45 mV immediately after the FET is turned off.

This offset can be compensated to a large extent by injecting a charge from another capacitance and voltage so that the net effect of the charges cancel. Such a circuit is shown in Figure 3-66.

C_C in Figure 3-66 is selected to be larger than the C_{DG}. This allows the step voltage to be lower than the step voltage on the FET switch. Note that when the FET switch gate voltage goes from high to low, the charge cap voltage goes from low to high. Since C_{DG} changes considerably (from 3 to 1pF) as the difference voltage between the gate and drain increases, the compensating network can completely cancel the charge

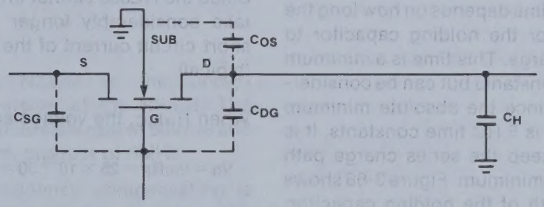


Figure 3-65

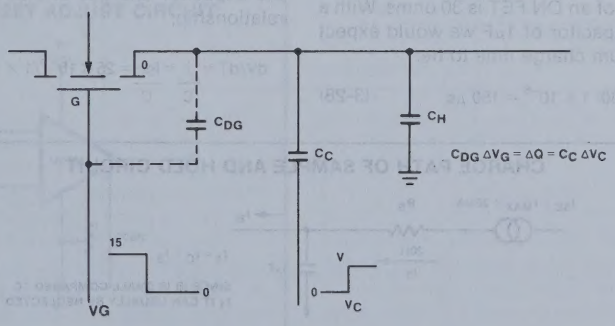


Figure 3-66

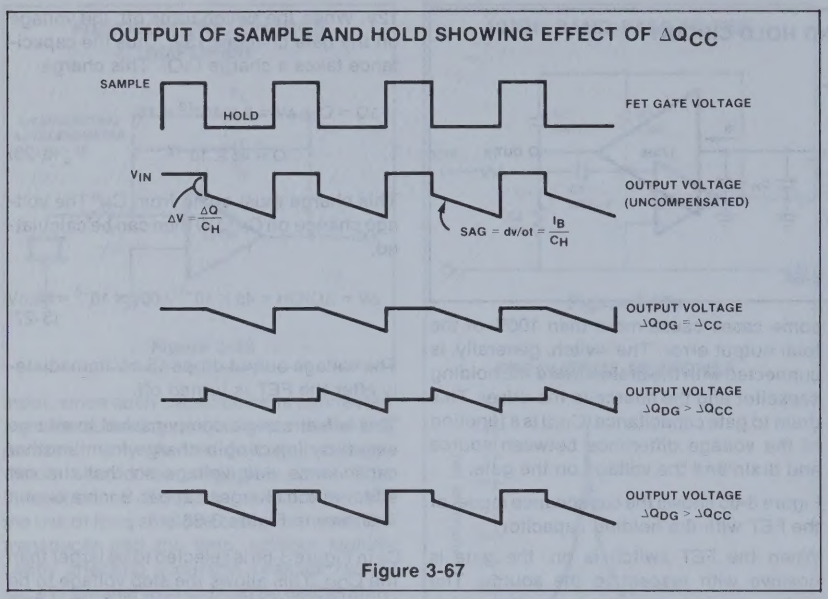


Figure 3-67

error for only one set of conditions. Figure 3-67 shows the comparative effects of C for different hold voltages. Because of this charge effect, the holding capacitor should be as large as possible for the desired sampling time. With a holding capacitor of .1μF this error is only .45mV.

Sampling Time

The sampling time depends on how long the circuit takes for the holding capacitor to reach a full charge. This time is a minimum of 5 RC time constants but can be considerably longer. Since the absolute minimum sampling time is 5 RC time constants, it is important to keep the series charge path resistance at a minimum. Figure 3-68 shows the charge path of the holding capacitor, with R_S equal to the ON resistance of the FET switch. Let's assume, for the moment, that the slew rate of the driver amplifier is not a factor. Since I_B is only 50pA, we can ignore its effect on the charge time. Typical resistance of an ON FET is 30 ohms. With a holding capacitor of 1μF we would expect the minimum charge time to be:

$$5RC = 5\ (30)\ 1 \times 10^{-6} = 150\ \mu s \qquad (3\text{-}28)$$

But the 5 RC time is based on an unlimited current source. The current required is:

$$I_1 = V_{IN}/R_S \qquad (3\text{-}29)$$

for a 10 volt step;

$$I_1 = 10V/30\ ohm = 333mA \qquad (3\text{-}29a)$$

Since the NE535 cannot drive 333mA, it will take considerably longer to charge. The short circuit current of the NE535 is 25mA (typical).

When $I_1 \alpha I_{SC}$, the voltage across R_S is

$$V_R = I_{SC}R_S = 25 \times 10^{-3}\ 30 = .75\ volt \qquad (3\text{-}30)$$

The voltage across the capacitor

$$V_C = V_{IN} - V_R = 9.25V \qquad (3\text{-}31)$$

The charge rate will be current limited until the capacitor charges to 9.25V. Using the relationship;

$$dV/dT = \frac{i}{C} = \frac{I_{SC}}{C} = 25 \times 10^{-3}/1 \times 10^{-6} \qquad (3\text{-}32)$$

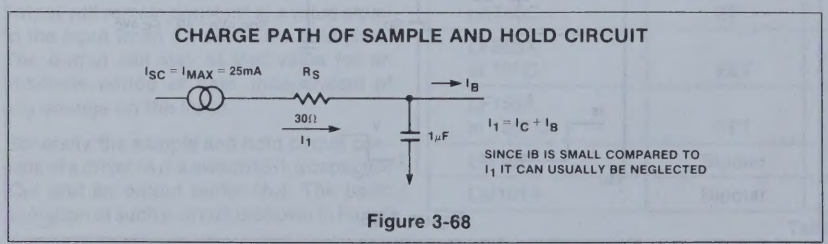


Figure 3-68

The charge rate for the capacitor is 25mV/μs. The time for the capacitor to charge to 9.25 volts is

$$9.25/25 \times 10^{-3} = 370\mu s \qquad (3\text{-}32a)$$

This, added to the time to charge 5 RC time constants of 150μs, brings the total sample time to 520μs minimum. The fact that current limiting occurs more than triples the minimum sample time.

Note that the charge rate is a function of the size of the capacitor and the short circuit current of the driver. Since the size of the holding capacitor affects output accuracy, it would be more desirable to provide more current to shorten the sample time. If we use the NE5534, we can shorten the minimum sampling time. The output current (I_{SC}) of the NE5534 is rated as typically 38mA. The charge rate now becomes:

$$dV/dT = 38 \times 10{-}3/1 \times 10{-}6 = 38mV/\mu s$$

Thus, the time to reach 9.25 volts is 243μs. The total charge time and thus minimum sample time is reduced to 393μs. When large holding capacitors are used, slew rate of the op amp will not improve performance significantly. The performance of a μA741C in the circuit discussed above is about the same as the NE535 since the I_{SC} is typically the same.

As the size of the holding capacitor is reduced, the slew rate of the op amp becomes a factor. The 1μF holding capacitor example above had a charge rate of 28mV/μs. Since the μA741 has a slew rate of 600mV/μs, it was not a factor. If the holding capacitor is .01μF, the charge rate is 2.8V/μs. It is obvious in this case that the .6V/μs of the μA741 would become a limiting factor.

Other Considerations

Some op amps used as a driver may present problems of instability when driving the capacitive load of the holding capacitor. Figure 3-69 shows a method of compensating an op amp for large capacitive loads. The capacitive load is isolated by R_{OUT} which is typically 50 ohms. C_F should yield a capacitative reactance of one tenth R_F at the unity gain crossover frequency of the driver. It is important to note that R_{OUT} will affect the RC charge path and lengthen the sample time requirements. This is usually of no concern for large holding capacitor circuits which have long sample time requirements anyway.

DRIVER COMPENSATED FOR LARGE CAPACITIVE LOADS

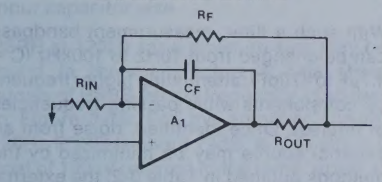


Figure 3-69

With large holding capacitors, an isolation resistor should be used between the input to the FET amplifier and the holding capacitor. This resistor prevents excessive input currents to the amplifier during power shut downs with a full charge on the capacitor.

Signetics also provides high-performance Sample and Hold circuits which require a minimum of external components. See the data sheets for the NE5537 and LF398 series devices.

SE/NE535, OP AMP APPLICATIONS

Introduction

The NE535 is a new generation monolithic op amp which features improved input characteristics. The device is compensated to unity gain and has a minimum guaranteed unity gain slew rate of 10V/μs. This is achieved by employing a clamped super beta input stage which has lower input bias current.

Applications

These improved parameters can be put to good use in applications such as sample and hold circuits which require low input current and in voltage follower circuits which require high slew rates. The circuit that follows will yield maximum small signal transient response and slew rate for the NE535 at unity gain.

It is always good practice in designing a system to use dual tracking regulators such as the Signetics NE5554 to power the dual supply op amps. This will guarantee the positive and negative supply voltage will be equal during power up. With the NE535, it is possible to degrade the input circuit characteristics by not applying the power supplies simultaneously. The NE535 is capable of directly replacing the μA741 with higher input resistance which will improve such designed as active filters, sample and hold, as well as voltage followers.

The NE535 can be used either with single or split power suplies.

VOLTAGE FOLLOWER WITH SINGLE POWER SOURCE

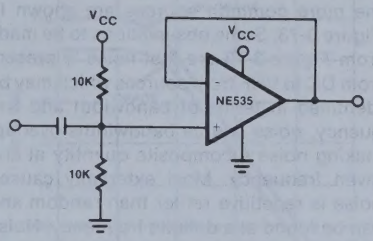


Figure 3-70

INVERTING AMP WITH SINGLE POWER SUPPLY

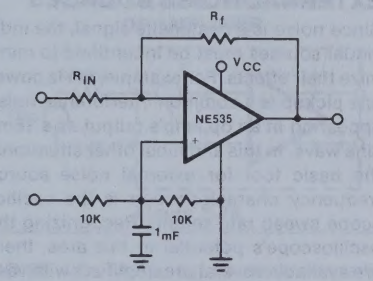


Figure 3-71

NE538

Introduction

The Signetics NE538 is the undercompensated version of the NE535. The NE538 has a typical slew rate of 50V/μs and a gain bandwidth product of 6MHz.

The internal frequency compensation is designed for a minimum inverting gain of 4 and a minimum non-inverting gain of 5. Below these gains the NE538 will be unstable and the NE535 should be used.

OFFSET ADJUST CIRCUIT

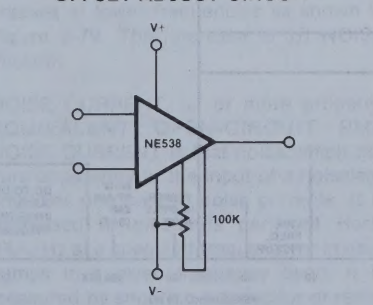


Figure 3-72

The higher slew rate of the NE538 has made this device quite appealing for high speed designs and the fact that it has a standard pinout will allow it to be used to upgrade existing systems that now use the μA741 or μA748.

INTRODUCTION TO NOISE

Since fabrication techniques in the integrated circuit industry have improved so tremendously in the past few years, input offset voltages and bias currents are being minimized and noise parameters (whether measured at the output or referred to the input) have become a major source of concern. Reducing noise by improved process techniques and by use of peripheral component control will be the thrust of this application as a secondary effort, in understanding the noise components themselves.

An inspection of industry specifications show several methods of rating amplifier noise performance.

1. Output signal to noise ratio.
2. Output noise level (with specified loads and bandwidth).
3. Output noise level referenced to normal operating level.
4. Equivalent input noise (at a specified gain, source impedance and bandwidth).
5. Noise figure.

BASIC NOISE PROPERTIES

Noise, for purposes of this discussion, is defined as any signal appearing in an op amp's output that could not have been predicted by DC and AC input error analysis. Noise can be random or repetitive, internally or externally generated, current or voltage type, narrowband or wideband, high frequency or low frequency; whatever its nature, it can be minimized.

The first step in minimizing noise is source identification in terms of bandwidth and location in the frequency spectrum; some of the more common sources are shown in Figure 3-73. Some observations to be made from Figure 3-73 are that noise is present from DC to VHF from sources which may be identified in terms of bandwidth and frequency, noise source bandwidths overlap, making noise a composite quantity at any given frequency. Most externally caused noise is repetitive rather than random and can be found at a definite frequency. Noise effects from external sources must be reduced to insignificant levels to realize the full performance available from a low noise op amp.

EXTERNAL NOISE SOURCES

Since noise is a composite signal, the individual sources must be indentified to minimize their effects. For example, 60Hz power line pickup is a common interference noise appearing at an op amp's output as a 16ms sine wave. In this and most other situations, the basic tool for external noise source frequency characterization is the oscilloscope sweep rate setting. Recognizing the oscilloscope's potential in this area, there are available several preamplifiers with variable bandwidth and frequency which allow quick noise source frequency identification. Another basic identification tool is the simple low pass filter as shown in Figure 3-74 where the bandpass is calculated by:

$$1)\ f_0 = \frac{1}{2\pi RC} \qquad (3\text{-}34)$$

With such a filter, measurement bandpass can be changed from 10Hz to 100kHz (C = 4.7μF to 470pF), attenuating higher frequency components while passing frequencies of interest. Once identified, noise from an external source may be minimized by the methods outlined in Table 3-2, the external noise chart.

POWER SUPPLY RIPPLE

Power supply ripple at 120Hz is not usually thought of as noise, but it should be. In an actual op amp application, it is quite possible to have a 120Hz noise component that is equal in magnitude to all other noise sources combined, and, for this reason, it deserves a special discussion.

To be negligible, 120Hz ripple noise should be between 10nV and 100nV referred to the input of an op amp. Achieving these low levels requires consideration of three factors: the op amp's 120Hz power supply

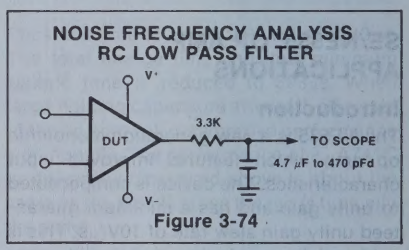


Figure 3-74

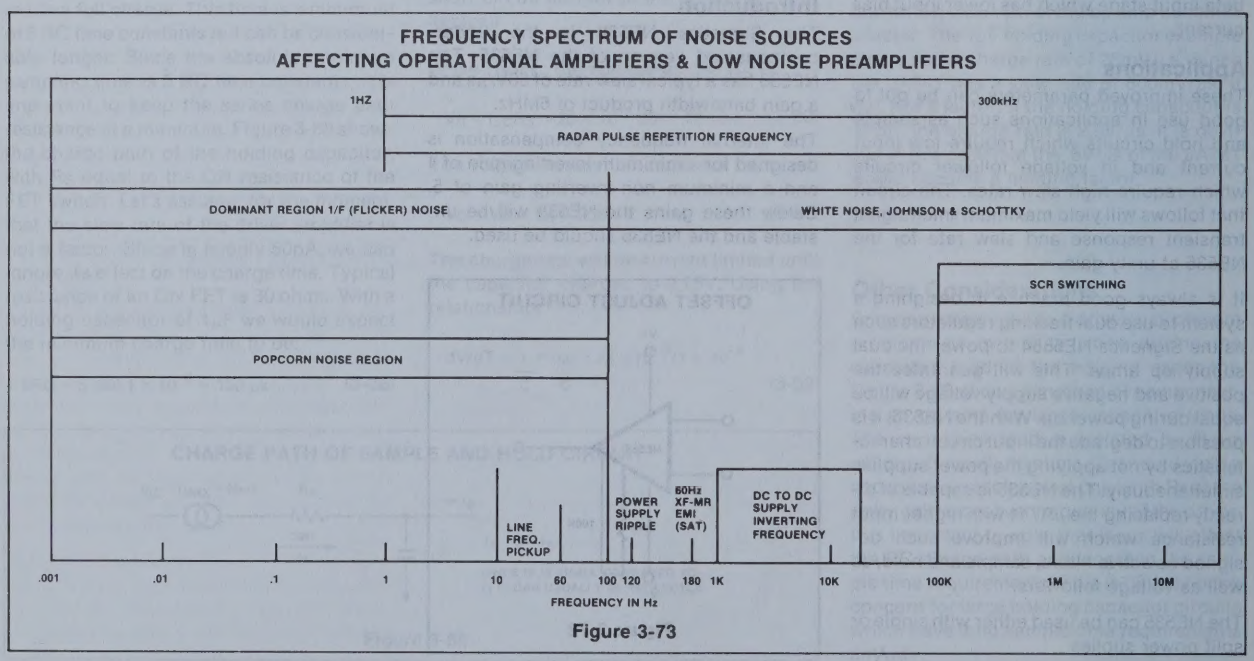


Figure 3-73

rejection ratio (PSRR), the regulator's ripple rejection ratio, and, finally, the regulator's input capacitor size.

PSRR at 120Hz for a given op amp may be found in the manufacturer's data sheet curves of PSRR versus frequency as shown in Figure 3-75. For the amplifier shown, 120Hz PSRR is about 74dB, and to attain a goal of 100nV referred to the input, ripple at the power terminals must be less than 5mV. Today's IC regulators provide about 60dB of ripple rejection; in this case the regulator input capacitor must be made large enough to limit input ripple to .5V.

Externally compensated low noise op amps can provide improved 120Hz PSRR in high closed-loop gain configurations. The PSRR versus frequency curves of such an op amp are shown in Figure 3-76. When compensated for a closed loop gain of 1000, 120Hz PSRR is 115dB. PSRR is still excellent at much higher frequencies, allowing low ripple noise operation in exceptionally severe environment.

POWER SUPPLY DECOUPLING

Usually, 120Hz ripple is not the only power supply associated noise. Series regulator outputs typically contain at least 150μV of noise in the 100Hz to 10kHz range, switching types contain even more. Unpredictable amounts of induced noise can also be present on power leads from many sources. Since high frequency PSRR decreases at 20dB/decade, these higher frequency supply noise components must not be allowed to reach the op amp's power terminals. RC decoupling, as shown in Figure 3-77, will adequately filter most wideband noise. Some caution must be exercised with this type of decoupling, as load current changes will modulate the voltage as the op amp's supply pins.

POWER SUPPLY REGULATION

Any change in power supply voltage will have a resultant effect referred to an op amp's inputs. For the op amp of Figure 3-75, PSRR at DC is 110dB (3μV/V) which may be considered as a potential low frequency noise source. Power supplies for low noise op amp applications should, therefore, be both low in ripple and well-regulated. Inadequate supply regulation is often mistaken to be low frequency op amp noise.

When noise from external sources has been effectively minimized, further improvements in low noise performance are obtained by specifying the right op amp, and through careful selection and application of the peripheral components.

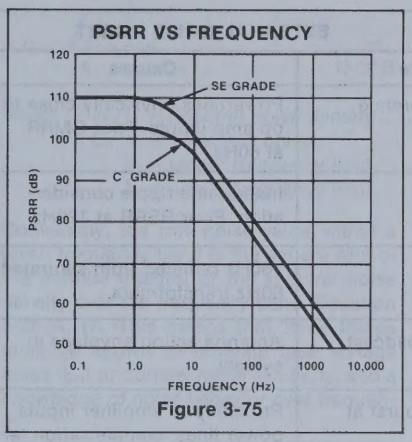


Figure 3-75

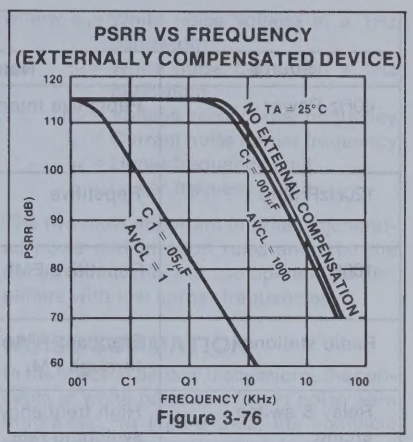


Figure 3-76

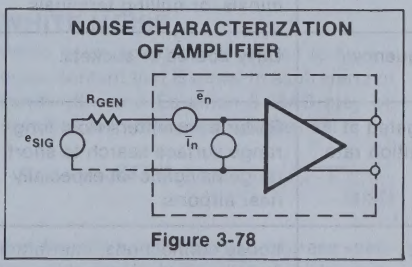


Figure 3-78

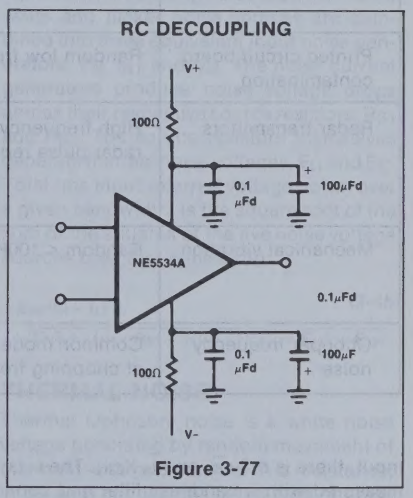


Figure 3-77

NOISE VOLTAGE, e_n, or more properly, EQUIVALENT SHORT-CIRCUIT INPUT RMS NOISE VOLTAGE is simply that noise voltage which would appear to originate at the input of a noiseless amplifier (referring to Figure 3-78) if the input terminals were shorted. It is expressed in nanovolts per root Hertz nV/$\sqrt{Hz}$ at a specified frequency, or in microvolts for a given frequency band. It is determined, or measured, by shorting the input terminals, measuring the output rms noise, dividing by amplifier gain, and referencing to the input. Hence the term, equivalent noise voltage. An output bandpass filter of known characteristic is used in measurements, and the measured value is divided by the square root of the bandwidth $\sqrt{B}$, if data is to be expressed per unit bandwidth or per root Hertz. The level of $\bar{e}_n$ is not constant over the frequency band; typically it increases at lower frequencies as shown in Figure 3-79. This increase is 1/f NOISE (flicker).

NOISE CURRENT, i_n, or more properly, EQUIVALENT OPEN-CIRCUIT RMS NOISE CURRENT is that noise which occurs apparently at the input of a noiseless amplifier due only to noise currents. It is expressed in picoamps per root Hertz pA/$\sqrt{Hz}$ at a specified frequency or in nanoamps in a given frequency band. It is measured by shunting a capacitor or resistor across the input terminals such that the noise current will give rise to an additional

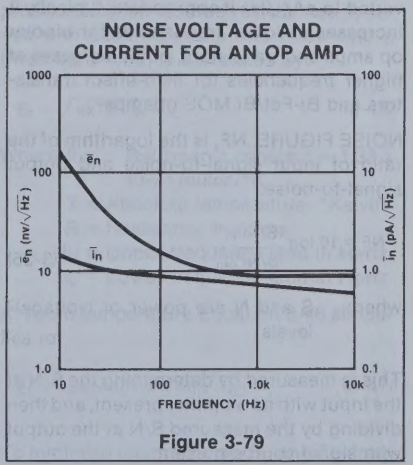


Figure 3-79

noise voltage which is $i_n \times R_{in}$ (or X_{cin}). The output is measured, divided by amplifier gain, referenced to input, and that contribution known to be due to $\bar{e}_n$ and resistor noise is appropriately subtracted from the total measured noise. If a capacitor is used at the

EXTERNAL NOISE CHART			
Source	**Nature**	**Causes**	**Minimization Methods**
60Hz Power	Repetitive Interference	Powerlines physically close to op amp inputs. Poor CMRR at 60Hz.	Reorientation of power wiring. Shielded transformers.
120HzRipple	Repetitive	Inadequate ripple consideration. Poor RSRR at 120Hz	Thorough design to minimize ripple. RC decoupling at the op amp.
180Hz	Repetitive EMI	180Hz radiated from saturated 60Hz transformers.	Physical reorientation of components. Shielding. Battery power.
Radio stations	Standard AM broadcast through FM	Antenna action anyplace in system.	Shielding. Output filtering. Limited circuit bandwidth.
Relay & switch arcing	High frequency burst at switching rate.	Proximity to amplifier inputs, power lines, compensation terminals, or nulling terminals.	Filtering of HF components. Shielding. Avoidance of ground loops. Arc suppressors at switching source.
Printed circuit board contamination	Random low frequency	Dirty boards or sockets.	Thorough cleaning and humidity sealant.
Radar transmitters	High frequency gated at radar pulse repetition rate.	Radar transmitters from long range surface search to short range navigational especially near airports.	Shielding. Output filtering of frequencies >> PRR.
Mechanical vibration	Random < 100Hz	Loose connections, intermittent metallic contact in mobile equipment.	Attention to connectors and cable conditions. Shock mounting in severe environments.
Chopper frequency noise	Common mode input current at chopping frequency	Abnormally high noise chopper amplifier in system	Balanced source resistors. Use bipolar input op amps instead.

Table 3-2

input, there is only $\bar{e}_n$ and $\bar{i}_n X_{CIN}$. The $\bar{i}_n$ is measured with a bandpass filter and converted to pA/$\sqrt{Hz}$ if appropriate; typically it increases at lower frequencies for bipolar op amps and transistors, but it increases at higher frequencies for field-effect transistors and Bi-Fet/Bi MOS opamps.

NOISE FIGURE, NF, is the logarithm of the ratio of input signal-to-noise and output signal-to-noise.

$$NF = 10 \log \frac{(S/N)_{in}}{(S/N)_{out}} \qquad (3\text{-}35)$$

where: S and N are power or (voltage)^2 levels

This is measured by determining the S/N at the input with no amplifier present, and then dividing by the measured S/N at the output with signal source present.

The values of R_{gen} and any X_{gen} as well as frequency must be known to properly express NF in meaningxul terms. This is because the amplifier $i_n \times Z_{gen}$ as well as R_{gen} itself produces input noise. The signal source in Figure 3-73 contains some noise. However, e_{sig} is generally considered to be noise free and input noise is present as the THERMAL NOISE of the resistive component of the signal generator impedance R_{gen}. This thermal noise is WHITE in nature as it contains constant NOISE POWER DENSITY per unit bandwidth. It is easily seen from Equation 2 that the $\bar{e}_n^2$ has the units V^2/Hz and that $(\bar{e}_n)$ has the units $V/\sqrt{Hz}$

$$\bar{e}_R^2 = 4kTRB \qquad (3\text{-}36)$$

where: T is temperature in °K
R is resistor value in ohms
B is bandwidth in Hz
k is Boltzman's constant

OPERATIONAL AMPLIFIER INTERNAL NOISE OP AMP NOISE SPECIFICATIONS

Most completely specified low noise op amp data sheets specify current and voltage noises in a 1Hz bandwidth and low frequency noise over a range of .1Hz to 10Hz. To minimize total noise, a knowledge of the derivation of these specifications is useful. In this section, the reader is provided with an explanation of basic op amp associated random noise mechanisms and introduced to a simplified method for calculating total input-referred noise in typical applications.

RANDOM NOISE CHARACTERISTICS

Op amp associated noise currents and voltages are random. They are aperiodic and uncorrelated to each other and have Gaussian amplitude distributions, the highest noise amplitudes having the lowest probability. Gaussian amplitude distribution allows random noises to be expressed as rms quantities; multiplying a Gaussian rms quantity by six, results in a peak to peak value that will not be exceeded 99.73% of the time.

The two basic types of op amp associated noises are white noise and flicker noise (I/f). White noise contains equal amounts of power in each Hertz of bandwidth. Flicker noise is different in that it contains equal amounts of power in each decade of bandwidth. This is best illustrated by spectral

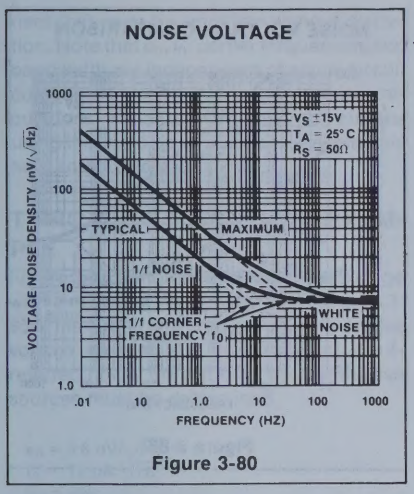


Figure 3-80

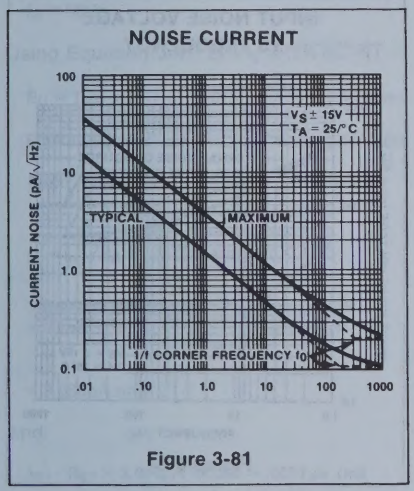


Figure 3-81

noise density plots such as in Figure 3-80 and 3-81. Above a certain corner frequency, white noise dominates; below that frequency, flicker (1/f) noise is dominant. Low noise corner frequencies distinguish low noise op amps from general purpose devices.

SPECTRAL NOISE DENSITY

To utilize Figures 3-80 and 3-81, let us consider the definition of spectral noise density: the square root of the rate of change of mean-square noise voltage (or current) with frequency Eq. 3-37A

$$e_n^2 = \frac{d}{dF}(E_n)^2 \qquad (3\text{-}37A)$$

$$i_n^2 = \frac{d}{dF}(I_n)^2 \qquad (3\text{-}37B)$$

$$E_n = \sqrt{\int_{f_L}^{f_H} e_n^2\, dF} \qquad (3\text{-}38A)$$

$$I_n = \sqrt{\int_{f_L}^{f_H} i_n^2\, dF} \qquad (3\text{-}38B)$$

where e_n, i_n = Spectral noise density
E_n, I_n = Total rms noise
f_H = Upper frequency limit
f_L = Lower frequency limit

Conversely, the rms noise value within a given frequency band is the square root of the definite integral of the spectral noise density over the frequency band (Equation 3-38 A, B). This means that three things must be known to evaluate total voltage noise (E_n) or current noise (I_n): f_H, f_L, and a knowledge of noise behavior over frequency.

WHITE NOISE

White noise sources are defined to have a noise content that is equal in each Hertz of bandwidth, and Equation 3-38AB may be rewritten for white noise sources as:

$$E_n(\omega) = e_n\sqrt{f_H - f_L} \qquad I_n(\omega) = i_n\sqrt{f_H - f_L} \qquad (3\text{-}39)$$

It is therefore convenient to express spectral noise density in $V/\sqrt{Hz}$ or $A/\sqrt{Hz}$ where $f_H - f_L = 1Hz$. When $f_H \geq 10\, f_L$, the white noise expressions may be further reduced to:

$$E_n(\omega) = e_n\sqrt{f_H} \qquad I_n(\omega) = i_n\sqrt{f_H} \qquad (3\text{-}40)$$

FLICKER NOISE & WHITE NOISE

Since flicker noise content is equal in each decade of bandwidth, total flicker noise may be calculated if noise in one decade is known. The .1Hz to 1Hz decade noise content (K) is widely used for this purpose because the white noise contribution below 10Hz is usually negligible.

$$E_n(f) \cong K\sqrt{\frac{1}{f}}\,, \quad I_n(f) \cong K\sqrt{\frac{1}{f}} \qquad (3\text{-}41\ a\ and\ b)$$

When substituted in Equation 3-36, the expressions may be rewritten to:

$$E_n(f) = K\sqrt{I_n\left(\frac{f_H}{f_L}\right)}, \quad I_n(f) = K\sqrt{I_n\left(\frac{f_H}{f_L}\right)} \qquad (3\text{-}42a\ and\ b)$$

When corner frequencies are known, simplified expressions for total voltage and current noise, (E_N and I_N), may be written:

$$E_N(f_H - f_L) = e_n\sqrt{f_{ce}\, I_n\left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \qquad (3\text{-}43)$$

$$I_N(f_H - f_L) = i_n\sqrt{f_{ci}\, I_n\left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \qquad (3\text{-}44)$$

where: e_n = White noise voltage in a 1Hz bandwidth
i_n = White noise current in a 1Hz bandwidth
f_{ce} = Voltage noise corner frequency
f_{ci} = Current noise corner frequency
f_H = Upper frequency limit
f_L = Lower frequency limit

The two most important internally generated noise minimization rules are: limit the circuit bandwidth and use operational amplifiers with low corner frequencies.

NOISE SUMMATION

In the spectral density discussions, the concepts of white noise and flicker noise were introduced. In Figure 3-82, the complete input-referred op amp noise model, internal white and flicker noise sources are combined into three equivalent input noise generators, E_N, I_{N1} and I_{N2}. The noise current generators produce noise voltage drops across their respective source resistors, R_{S1} and R_{S2}. The source resistors themselves generate thermal noise voltages, E_{t1} and E_{t2}. Total rms input referred voltage noise, over a given bandwidth, is the square root of the sum of the squares of the five noise voltage sources over that bandwidth.

$$E_{NT}(f_H - f_L) = \sqrt{E_N^2 + (I_{N1}\cdot R_{S1})^2 + (I_{N2}\cdot R_{S2})^2 + E_{t1}^2 + E_{t2}^2} \qquad (3\text{-}45)$$

THERMAL NOISE

Thermal (Johnson) noise is a white noise voltage generated by random movement of thermally-charged carriers in a resistance; in op amp circuits this is the type of noise produced by the source resistances in series with each input. Its rms value over a given bandwidth is calculated by:

$$E_t = \sqrt{4kTR\,(f_H - f_L)} \qquad (3\text{-}46)$$

Where: k = Boltzman's constant = 1.38 x 10^{-23} joules/°K
T = Absolute temperature, °Kelvin
R = Resistance in ohms
f_H = Upper frequency limit in Hertz
f_L = Lower frequency limit in Hertz

At room temperature Equation 3-46 simplifies to:

$$E_t = 1.28 \times 10^{-10}\sqrt{R(f_H - f_L)} \qquad (3\text{-}47)$$

To minimize thermal noise (E_{t1} and E_{t2}) from R_{S1} and R_{S2}, large source resistors and excessive system bandwidth should be avoided.

Thermal noise is also generated inside the op amp, principally from r_{bb}, the base-spreading resistances in the input stage

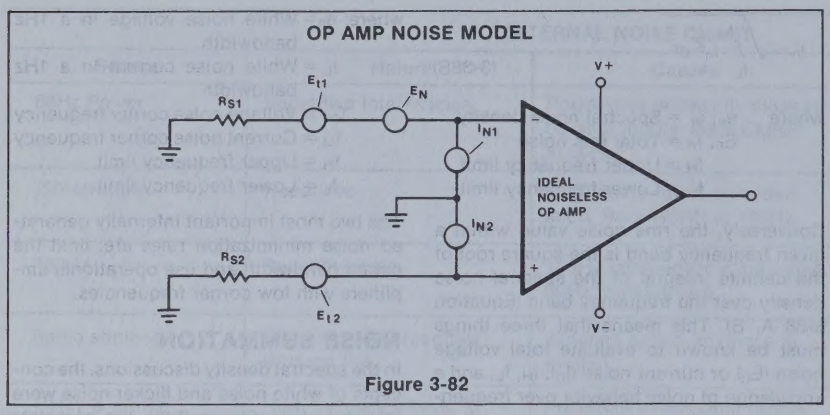


Figure 3-82

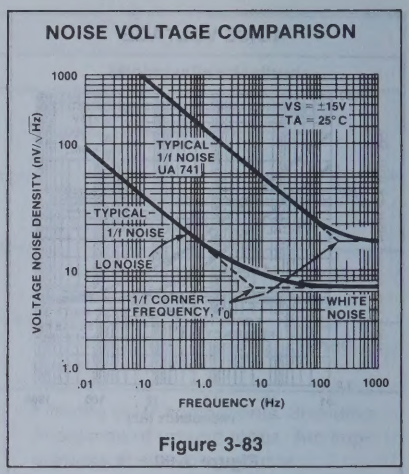


Figure 3-83

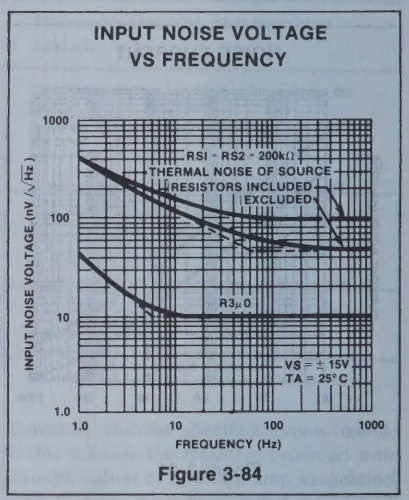


Figure 3-84

transistors. These noises are included in E_N, the total equivalent input voltage noise generator.

SHOT NOISE

Shot noise (Shottky noise) is a white noise current associated with the fact that current flow is actually a movement of discrete charged particles (electrons). In figure 3-82 I_{N1} and I_{N2}, above the 1/f frequency, are shot noise currents which are related to the amplifier's DC input bias currents:

$$I_{sh} = \sqrt{2qI_{BIAS}(f_H - f_L)} \qquad (3\text{-}48)$$

where: I_{sh} = RMS shot noise value in amps
q = Charge of an electron = 1.59×10^{-19}
I_{BIAS} = Bias current in amps
f_H = Upper frequency limit in Hertz
f_L = Lower frequency limit in Hertz

At room temperature Equation 3-48 simplifies to:

$$I_{sh} = 5.64 \times 10^{-10} \sqrt{I_{BIAS}(f_H - f_L)} \qquad (3\text{-}49)$$

Shot noise currents also flow in the input stage emitter dynamic resistances, (r_e), producing input noise voltages. These voltages, along with the r_{bb}, thermal noise, make up the white noise portion of E_N, the total equivalent input noise voltage generator.

FLICKER NOISE

In limited bandwidth applications, flicker (1/f) noise is the most critical noise source. An op amp designer minimizes flicker noise by keeping current noise components in the input and second stages from contributing to input voltage noise. Equation 3-50 illustrates this relationship:

$$\frac{i_n \text{ second stage}}{gm \text{ first stage}} = e_n \text{ input} \qquad (3\text{-}50)$$

Another critical factor is corner frequency. For minimum noise the current and voltage noise corner frequencies must be low; this is crucial. As shown in Figure 3-83 low noise corner frequencies distinguish low noise op amps from ordinary industry standard 741 types.

POPCORN NOISE

Popcorn noise (burst noise) is a momentary change in input bias current usually occurring below 100Hz, and is caused by imperfect semiconductor surface conditions incurred during wafer processing. Minimization of this problem can be accomplished through careful surface treatment, general cleanliness, and a special three-step process known as "Triple Passivation".

Op amp manufacturers face a difficult decision in dealing with popcorn noise. Through careful low noise processing, it can be significantly reduced in almost all devices; alternatively, the processing may be relaxed, and finished devices must be individually tested for this parameter. Special noise testing takes valuable labor time, adds significant amounts to manufacturing cost, and ultimately increases the price a customer has to pay.

TOTAL NOISE CALCULATION

With data sheet curves and specifications, and a knowledge of source resistance values, total input-referred noise may be calculated for a given application. To illustrate the method, noise information from a data sheet is reproduced in Figure 3-84. The first step is to determine the current and voltage noise corner frequencies so that the E_N and I_N terms of Equation 3-45 may be calculated using Equations 3-43 and 3-44.

CORNER FREQUENCY DETERMINATION

In the input shot noise versus frequency curves of Figure 3-84, it may be seen that voltage noise ($R_S = 0$) begins to rise at about 10Hz. Lines projected from the horizontal (white noise) portion and sloped (flicker noise) portion intersect at 6Hz, the voltage noise corner frequency (f_{ce}). In the center curve, excluding thermal noise from the source resistance, current noise multiplied by 200Ω is plotted as a voltage noise. Lines projected from the horizontal portion and sloped portions intersect at 60Hz, the current noise corner frequency (f_{ci}). Equations 3-43 and 3-44 also require e_n and i_n for calculation of E_N and I_N. To find e_n and i_n, use the data sheet specification a decade or more above the respective corner frequencies; in this case e_n is 9.6 nV/$\sqrt{Hz}$ (1000Hz), and i_n is 0.12 pA/$\sqrt{Hz}$ (1000Hz).

BANDWIDTH OF INTEREST

To be summed correctly, each of the five noise quantities must be expressed over the same bandwidth, ($f_H - f_L$). At this time, assume f_H to be the highest frequency compo-

nent that must be amplified without distortion. Note that e_n, i_n, corner frequencies and bandwidth are independent of actual circuit component values. When doing noise calculations for a large number of circuits using the same op amp, these numbers only have to be calculated once.

TYPICAL APPLICATION EXAMPLE

Figure 3-85A shows a typical X10 gain stage with a 10kΩ source resistance. In Figure 3-85B, the circuit is redrawn to show five noise voltage sources. To evaluate total input-referred noise, the values of each of the five sources must be determined.

$e_n = 9.6\ nV/\sqrt{Hz}$
$I_n = .12\ pA/\sqrt{Hz}$
$f_{ce} = 6Hz$
$f_{ci} = 60Hz$

Using Equation 3-47: $E_t = \sqrt{4KTR\,(f_H - f_L)}$

$E_{t1} = 1.28 \times 10^{10} \sqrt{(900\Omega)\,(100Hz)} = 0.4\mu V$ rms

$E_{t2} = 1.28 \times 10^{-10} \sqrt{(10K\Omega)\,(100Hz)} = .128\mu V$ rms

Next, calculate I_N using Equation 3-44

$$I_N = i_n \sqrt{f_{ci}\, I_n \left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$$

$$= .12pA \sqrt{60\, I_n \left(\frac{100Hz}{0.01\ Hz}\right) + (100 - 0.01)}$$

$= 3.066pA$ rms

and:

$I_{N1} \cdot R_{S1} \cong 3.066pA\ (900\Omega) = .0027\mu V$ rms

$I_{N2} \cdot R_{S2} = 3.066pA\ (10k\Omega) = .0306\mu V$ rms

Finally, E_N from Equation 3-43

$$E_N = e_n \sqrt{f_{ce}\, I_n \left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$$

$$= 9.6nV \sqrt{6\, I_n \left(\frac{100Hz}{0.01Hz}\right) + (100 - 0.01)}$$

$= 0.120\mu V$ rms

Substituting in Equation 3-45

$$E_{NT}\,(f_H - f_L) = \sqrt{E_N^2 + I_{N1}^2 R_{S1}^2 + (I_{N2} R_{S2})^2 + E_{t1}^2 + E_{t2}^2}$$

$$= \sqrt{(.120\mu V)^2 + (.0027\mu V)^2 + (.0306\mu V)^2 + (.04\mu V)^2 + (.128\mu V)^2}$$

$= 0.183\mu V$rms

Using the factor of 6, total input-referred noise = $1.1\mu V$ peak to peak (0.01Hz to 100Hz).

741 CALCULATION EXAMPLE

The preceeding calculation determined total noise in a given bandwidth using a low noise op amp. To place this level of performance into perspective, a calculation using the industry-standard 741 op amp in the circuit of Figure 3-85 is useful. Once again the starting point is corner frequency determination, using the data sheet curves:

$f_{ce} = 200Hz$; $f_{ci} = 2kHz$; $e_n = 20nV/\sqrt{Hz}$; $i_n = .5pA/\sqrt{Hz}$.

Using these corner frequencies and noise magnitudes, E_N and I_N are calculated to be $0.88\mu V$ rms and 68pA rms respectively. Multiplying this noise current by the source resistance gives terms 2 and 3 of Equation 3-45 as shown below.

$$E_{NT}\,(f_H - f_L) = \sqrt{E_N^2 + I_{N1}^2 R_{S1}^2 + I_{N2}^2 R_{S2}^2 + E_{+1}^2 + E_{t2}^2} \qquad (3\text{-}45)$$

Substituting in Equation 3-45

$$= \sqrt{(0.88\mu V)^2 + (.061\mu V)^2 + (.68\mu V)^2 + (0.4\mu V)^2 + (.128\mu V)^2}$$

$= 1.12\mu V$ rms

Total input-referred noise = $6.7\mu V$ peak to peak (0.01Hz to 100Hz)

This is 5.9 times that of the low noise op amp example.

The calculation examples illustrate three rules for minimizing noise in operational amplifier applications:

RULE 1. Use an op amp with low corner frequencies.

RULE 2. Keep source resistances as low as possible.

RULE 3. Limit circuit bandwidth to signal bandwidth.

NOISE PERFORMANCE

This segment shall be concerned with determining the signal to noise characteristics and the noise figure of amplifiers.

The amplifier noise is composed of thermal noise generated in the base resistance shot noise caused by the arrival of discrete charges at diode junction and 1/f noise.

For simplification these noise sources can be combined and the amplifier modeled by a noise source and a noiseless amplifier as in Figure 3-86.

e_n = Amplifier's equivalent mean square noise voltage $/\sqrt{Hz}$
i_N = Amplifier's equivalent mean square noise current$/\sqrt{Hz}$

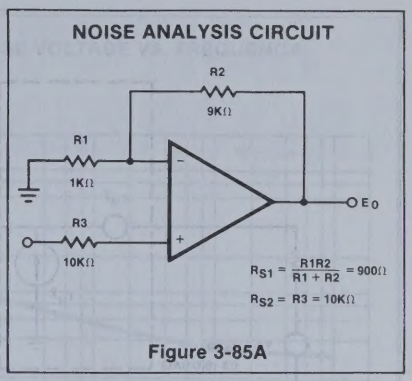


Figure 3-85A

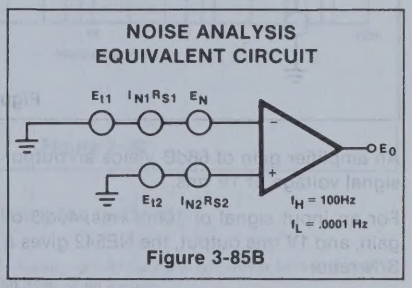


Figure 3-85B

The total output noise can now be computed by Equation 3-41.

$$e_t = (e_n^2 + i_n^2 R_s^2 + 4KTR_s)^{1/2} B^{1/2}\ A \text{ rms volts} \qquad (3\text{-}41)$$

*assuming R_S small compared to amplifier input.

If we now compare the total output noise to the output signal, A-Es, we find the output signal to noise ratio.

$$S/N = \frac{E_s}{(e_n^2 + i_n^2 R_s^2 + 4KTR_s)\,1/2B1/2} \qquad (3\text{-}46)$$

The denominator of the S/N ratio is the total output noise divided by the midband gain or the equivalent input noise as shown on NE542 specification sheet.

$$E_{IN} = (e_n^2 + i_n^2 R_s^2 + 4KTR_s)\,1/2B1/2 \text{ rms volts} \qquad (3\text{-}47)$$

The S/N ratio may now be computed independent of the amplifier gain. However, the gain should be chosen to maintain linear operation of the amplifier. For example: If the input signal to the NE542 is $400\mu V$ rms from a source resistance of 680 ohm with a bandwidth of 100Hz to 10kHz, the S/N ratio becomes, in dB:

$$S/N = 20 \log \frac{400\ \mu V}{0.77\mu V}$$

$= 54.3dB$

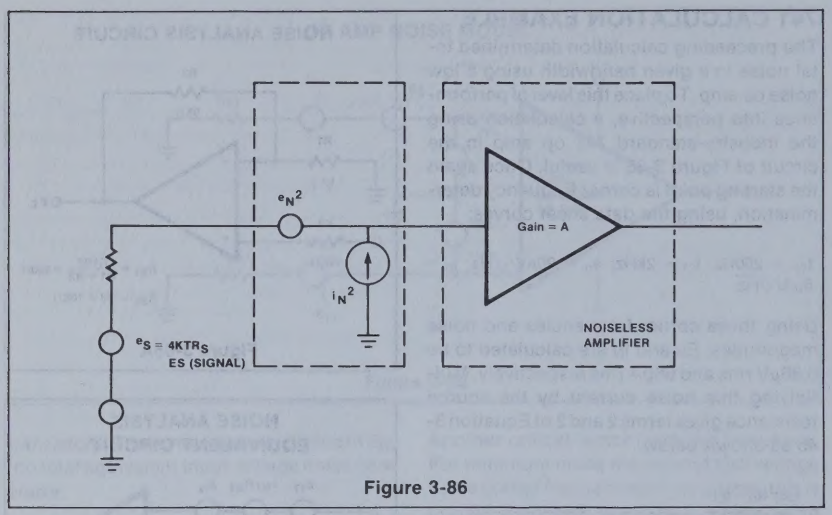


Figure 3-86

An amplifier gain of 68dB yields an output signal voltage of 1V rms.

For an input signal of 10mV rms, 40dB of gain, and 1V rms output, the NE542 gives a S/N ratio:

$$S/N = 20 \log \frac{10{,}000}{0.77} = 82.3dB$$

Another popular figure of merit for measuring the noise performance of an amplifier is noise figure. We first define noise factor (F) as

$$F = \frac{\text{Noise power input(Tot.)}}{\text{Thermal noise power}}$$

in terms of voltage this can be expressed as:

$$F = \frac{4KTR_s + (e_n^2 + i_n^2 R_s^2)}{4KTR_s} = 5.34,\ R_S = 680\Omega \quad (3\text{-}48)$$

The noise figure is now defined as:

$$N.F. = 10 \log F\ (dB)$$

or

$$N.F. = 10 \log \frac{4KTR_s + e_n^2 + i_n^2 R_s^2}{4KTR_s} (dB) \quad (3\text{-}49)$$

A noiseless amplifier will, therefore, have a noise figure of "0" dB. Although the bandwidth has been eliminated from this calculation, it is still an influencing factor on the noise figure since the value of e_n and i_n will be dependent on the bandwidth of interest. This is especially true if l/f or high frequency noise is in this bandwidth.

From Figures 3-87 and 3-88 we can calculate the noise figure. For the NE542 the noise figure for 100Hz to 10kHz, 3dB bandwidth (15.7 kHz equivalent noise bandwidth) and a source resistance of 5K ohms is:

$$N.F. = 10 \log \left(1 + \frac{e_n^2 + i_n^2 R_s^2}{4KTRS}\right) \quad (3\text{-}50)$$

$$NF = 10 \log \left(1 + \frac{(7)^2 \times 10^{-18} + (.25)^2 \times 10^{-24} \times R_S^2}{75 \times 10^{-18}}\right)$$

$$4 \times 1.38 \times 15^{23} \times 300° K \times R_S$$

$$= 10 \log \times$$

$= 7.27@\ R_S = 680\Omega$
$= 2.07@\ R_S = 5K\Omega$
$= 1.25@\ R_S = 10K\Omega$

To this point, the discussion has been limited to flat band response and no mention of the effect of equalization networks has been made. In instances where the gain of the amplifier is changing significantly across the frequency band of interest, as is the case for NAB and RIAA equalization, the noise performance is significantly improved.

The following table lists the spectral voltage and current noise densities and the respective corner frequencies for several different operational amplifiers and low noise preamplifiers.

where I_N = total current noise over a specified bandwidth.
E_N = total voltage noise over a specified bandwidth.
E_{ti} = thermal (Johnson) noise of the source resistance.
*R_S = equivalent input source (or generator) resistance.

NOTE
* If R_S is a complex function, Z_S, then this function must be calculated for the R_{SS} mean of each bandwidth considered. For example the input is a capacitor in parallel with a resistor, the input impedance is therefore:

$$Z_{in} = \frac{R}{1 + jwCR}.$$

Therefore as the frequency varies the absolute value of Z_{in} will vary and will affect the $I_N R_S$*, input noise value.

GENERAL EQUATIONS

Total Spectral Voltage Noise

$$E_N\ (f_H - f_L) = e_n \sqrt{f_{CE} \ln \left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \quad (3\text{-}51)$$

Total Spectral Noise Current

$$I_n\ (f_H - f_L) = i_n \sqrt{f_{ci} \ln \left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \quad (3\text{-}52)$$

Thermal

$E_t = 4\ KTR\ (f_H - f_L)$
$K = 1.38 \times 10^{-23}$ joules/°K (3-53)
T = abs. temp in °K
k = ohms
$f_t = 1.28 \times 10^{-10} \sqrt{R(f_H - f_L)}$ at Room Temp.

Shot at Room

(3-54)

$$I_{SH} = 5.64 \times 10^{-10} \sqrt{I_{bias}\ (f_H - f_L)}$$

Total Noise*

$$\left| E_{NT} \right|_{f_L}^{f_H} = \sqrt{E_n^2 + (I_N R_{S1})^2 + I_{N2} R_{S2}^2 + E_{t1}^2 + E_{t2}^2} \quad (3\text{-}55)$$

SPECTRAL VOLTAGE AND CURRENT NOISE DENSITIES

	μA741	NE535	5534	LF357	NE542	LM387
e_n (nv/√Hz)	40	15	4	12	7	9
i_n (pa/√Hz)	.25	.15	.6	.01	.25	0.7
e_n fce (Hz)	200	15	90	50	800	850
i_n fci (Hz)	1.5k	90	200	1	700	2

TABLE 3-3

NOTES
1. The current spectral noise is omitted for the LF series since current noise levels in J-FET devices are insignificant.
2. The spectral current noise for the LM387 is relatively linear over the frequency spectrum of 100Hz to 10 kHz and is not specified below 100Hz.

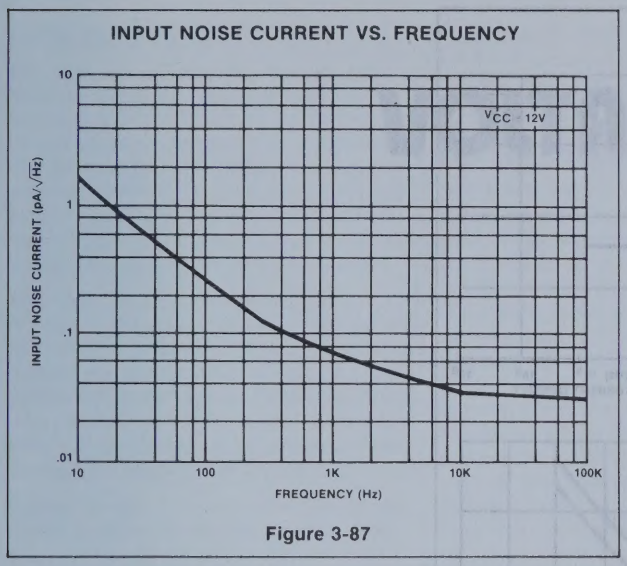


Figure 3-87

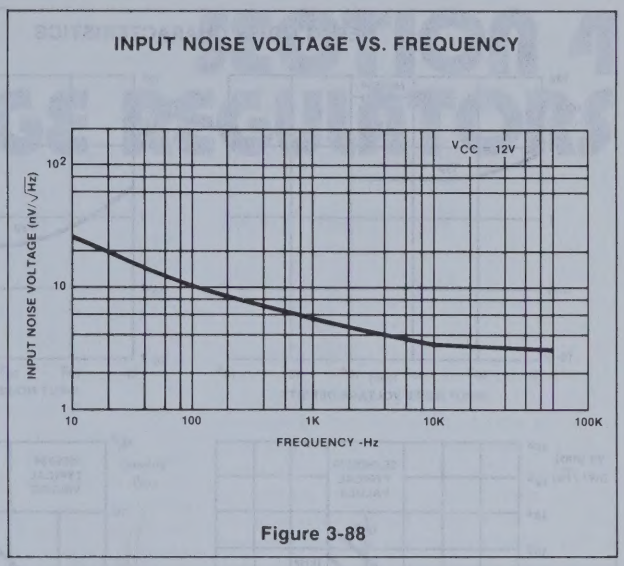


Figure 3-88

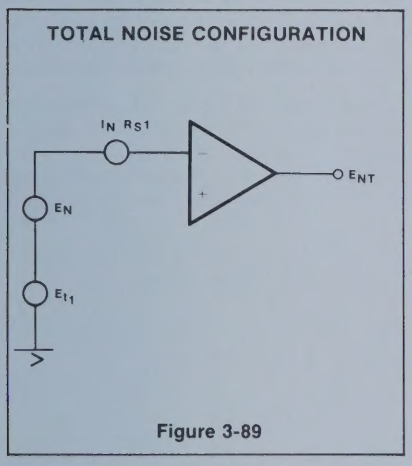


Figure 3-89

Example:

In order to determine the total noise of any device the following basic procedures can be used.

1. Determine the spectral voltage noise value $\overline{e_n}$ and the 3dB corner frequency. (If the value is not listed, but a curve given, the spectral noise value will be that value above the 3dB corner frequency on the flat portion of the curve.)
2. Determine the spectral current noise value $\overline{i_n}$ and the 3dB corner frequency. (The same note holds true as for the spectral voltage noise, except that the corner frequencies are generally not the same).
3. Determine the thermal noise of the input port source resistances by using the basic equal at room temperature of
   $E_T = 1.28 \times 10^{-10} \sqrt{R}/\sqrt{Hz}$
4. Using Equation 1, 2, and 4 and using Figure 3-73 as a basic block, we then can determine the total current and voltage noise at the input ports.
5. Employing Equation 5 we can then determine the total RSS voltage noise referred to the input of the amplifier.
6. If the closed loop gain of the system is known, then the total output noise is then
   $E_{Nout} = E_{Nin} \times A_{CL}$

Given: From Table 3-3: the NE5534 operating over the range of 10Hz to 1kHz and 1kHz to 10kHz, with $R_S = 10k\Omega$: determine total input noise over each bandwidth.

$$E_N (f_H - f_L) = e_n \sqrt{f_{ce} I_n \frac{f_H}{f_L} + (f_H - f_L)} \quad (3\text{-}51)$$

$$I_N (f_H - f_L) = i_n \sqrt{f_{c1} I_n \frac{f_H}{f_L} + (f_H - f_L)} \quad (3\text{-}52)$$

$$E_T = 1.28 \times 10^{-10} \sqrt{R(f_H - f_L)} \quad (3\text{-}54)$$

$$\left| E_{NT} \right|_{f_L}^{f_H} = \sqrt{(E_N)^2 + (I_{n1} R_{s1})^2 + (E_t)^2} \quad (3\text{-}55)$$

For the first band (10Hz to 1kHz)

$$E_N = 4 \times 10^{-9} \sqrt{90 \ln (100) + (990)} = .15\mu V \text{ rms}$$

$$I_N R_S = .6 \times 10^{-12} \sqrt{200 \ln (100) + (990) \times (10^4)} = .26\mu V \text{ rms}$$

$$E_T = 1.28 \times 10^{-8} \sqrt{990} = 0.4\mu V \text{ rms}$$

$$E_{TH}{}_{10}^{1000} = \sqrt{(E_N)^2 + (I_N R_S)^2 + E_T{}^2} = 0.50\mu V \text{ rms}$$

Using the factor of 6

$f_{noise\ p-p} = 3.00\mu V$ p-p will never be exceeded in 99.73% of all cases.

For the second band (1kHz to 10kHz)

$$*E_N = 4 \times 10^{-9} \sqrt{9000} = .38\mu V \text{ rms}$$

$$*I_N R_S = .6 \times 10^{-12} \sqrt{9000 \times (10^4)} = .58\mu V \text{ rms}$$

$$E_t = 1.28 \times 10^{-10} \sqrt{10^4 (9000)} = 1.21\mu V \text{ rms}$$

NOTE
* For frequencies above 1kHz only white noise is a consideration.

$$\left| E_{TH} \right|_{1kHz}^{10kHz} = \sqrt{(.38)^2 + (.57)^2 + (1.21)^2}\ \mu V \text{ rms}$$

$$RSS \left| E_{TH} \right|_{1kHz}^{10kHz} = \sqrt{1.39}\mu V \text{ rms}$$

$$E_{TH}{}_{max} = 8.34\mu V \text{ p-p}$$

CONCLUSION

The designer should look at the previous application note as a reasonable approach to determine system noise levels. The variations of parameters, such as resistance values, temperature, bandwidth are controllable by design procedure; however, the parametric variations of the monolithic op amps are controlled by the IC manufacturer. Signetics manufactures a wide variety of operational amplifiers designed to meet all contingencies.

NE5534 NOISE CHARACTERISTICS

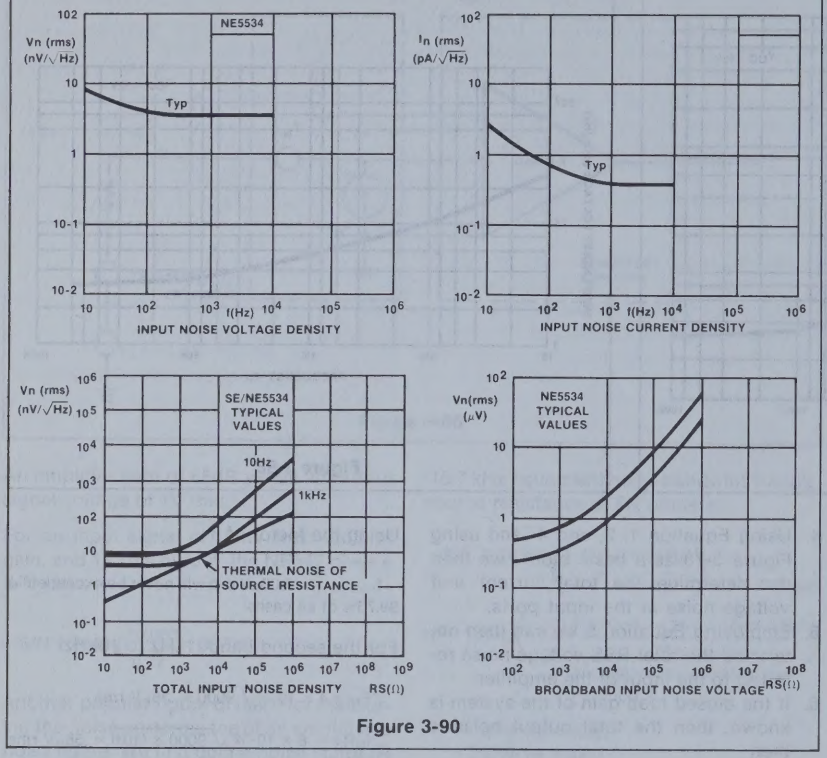
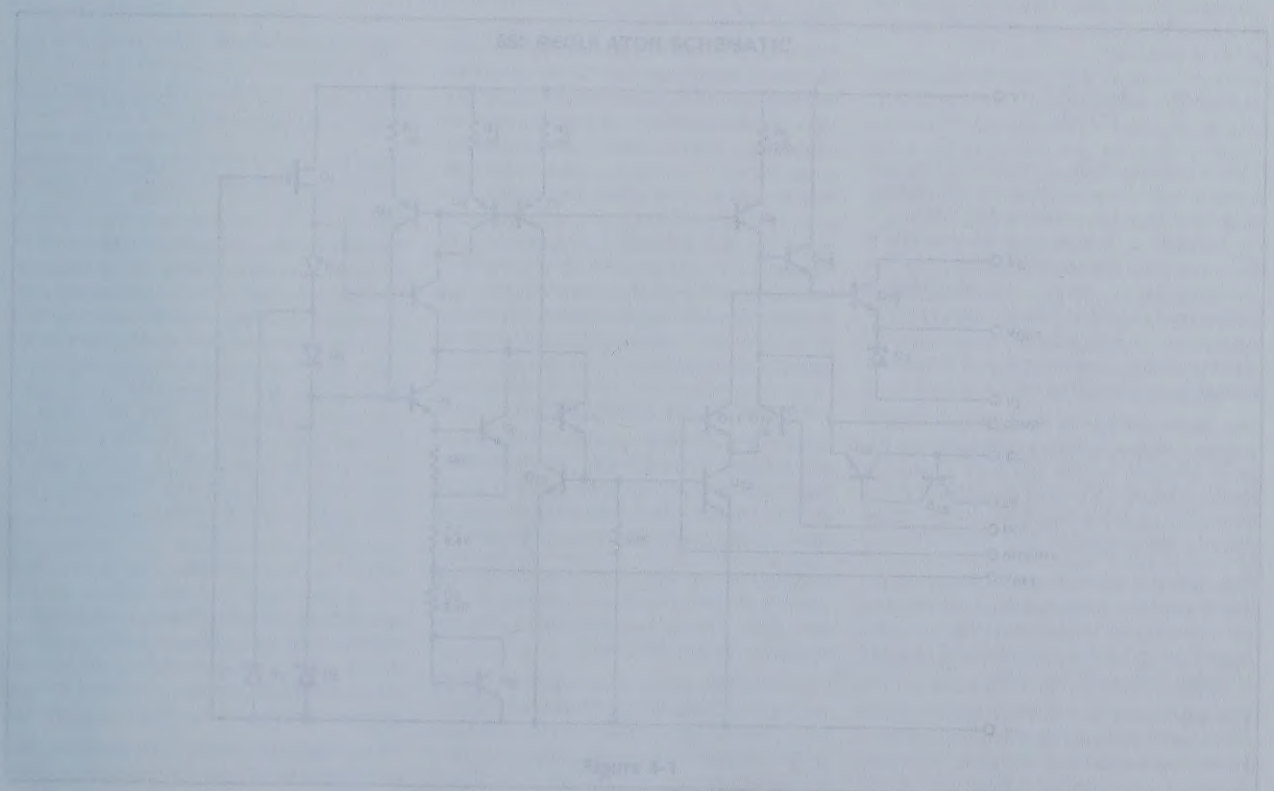


Figure 3-90

SECTION 4
VOLTAGE REGULATORS



INTRODUCTION

The wide use of integrated circuits in systems has frequently led to the power supply and regulator portions taking a disproportionate share of the volume of the system. The introduction of flexible, high performance regulator ICs such as the NE550 has made it possible for a designer to produce a highly regulated power supply in a small space with greatly reduced design effort.

The objective of a voltage regulator is to provide a constant output voltage independent of input supply voltage, output load current, and temperature. In general, it is desirable that the regulator should limit its own dissipation and its output current so that fault conditions and overload will not damage the regulator or the load.

Supply regulators contain four basic elements: a reference source, an error detector, a control device, and protection circuitry. For the devices discussed here, the reference source is a constant voltage, the control device is a pass transistor, and the protection is primarily by current limiting.

Because the application of voltage regulators depends a great deal upon the internal workings of the integrated circuit, a brief discussion of the design is included before actual applications are presented.

A schematic of the NE550 is present in Figure 4-1. For the sake of brevity this discussion will deal with the NE550 but in most cases will apply also to the μA723 device.

THE REFERENCE SOURCE

The NE550 reference voltage is developed across the zener diode D2. The voltage is temperature compensated by the base-emitter drops in Q4, Q5 and Q6, in combination with the resistance divider R2—R6. The voltage appearing at the emitter of Q5 has a temperature coefficient of approximately +7mV/° C while that at the base of Q6 is approximately -2.3mV/° C. Thus, by choosing the appropriate tap on the resistor R2—R6, it is possible to obtain a zero temperature coeffient. Naturally, the actual value of the temperature coefficient will fluctuate from unit to unit, but accurate compensation is easier to achieve here than with other methods. The effective impedance at this point is predominantly the parallel impedance of R2 and R6, increased by the diode impedances, and is typically 2k ohms.

The reference circuit as it stands is not self starting, necessitating the addition of FET Q1, D1, D4, and D5. When there is no current in D2, Q1 will feed current through D4 and D5 into the base of Q4, thus starting the current sources. When these are operating, D1 drops approximately the same voltage as D2, so D5 has no voltage across it and it no longer affects the reference circuit. The current through Q1 drives the base of Q17, with D1 and D4 providing the correct bias point for the proper operation of Q4 and Q5.

ERROR AMPLIFIER

The error amplifier in the NE550 is a differential amplifier composed of Q11 and Q12, with biasing provided by Q7, Q8, Q9, Q10 and Q13. Q7 and Q8 act as equal current sources, driven by Q2, with R4 and R5 improving the balance and output impedance characteristics. The current from Q7 is inverted in Q10 and Q13. Q13 has twice the area of Q10, so the current sink of Q13 is twice the value of the source Q7 and Q8. Q9 eliminates the error term caused by the basic currents of Q12 and Q13. Thus, the sum of the emitter currents of Q4 and Q12 is twice the current in source Q8. In balance, the current flow into the base of Q14 can be neglected, so the collector current of Q12 is equal to the current from Q8. Ignoring the base current of Q12, the emitter current of Q12 is half the collector current of Q13, so Q11 must carry the remainder. Hence, the currents in Q11 and Q12 are equally matched at balance, or no error condition. An unbalanced condition where the base of

550 REGULATOR SCHEMATIC

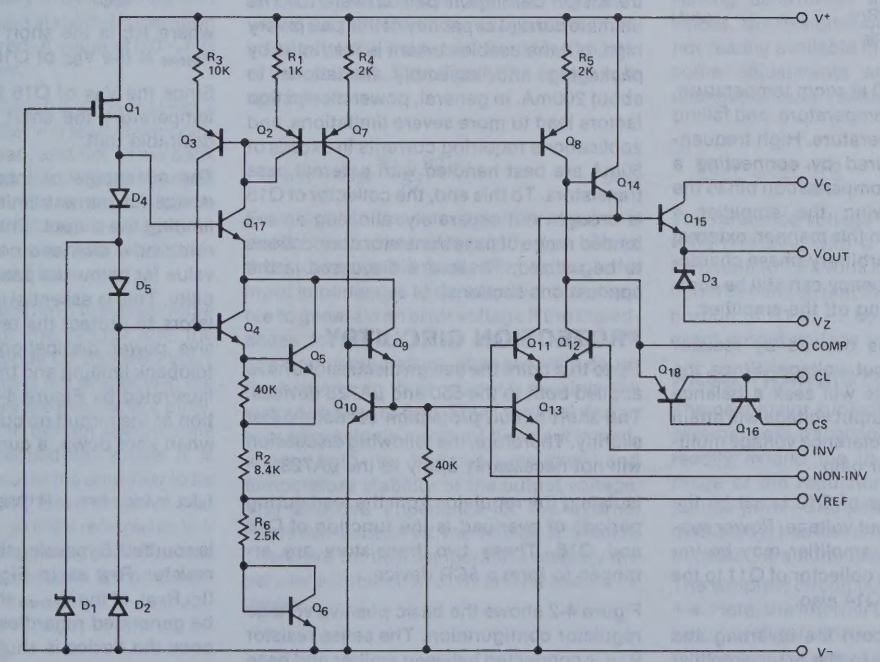


Figure 4-1

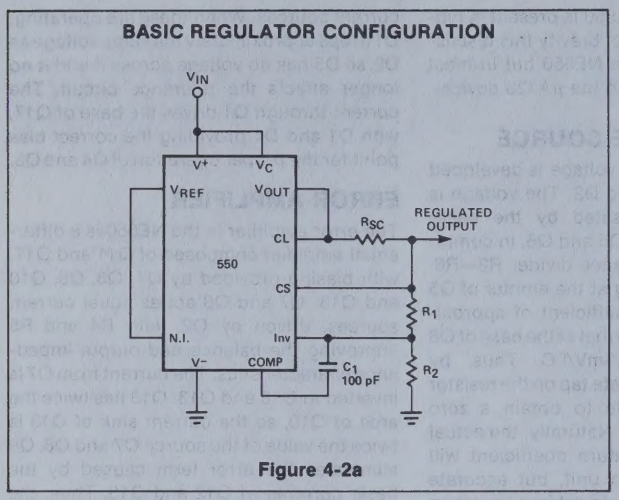


Figure 4-2a

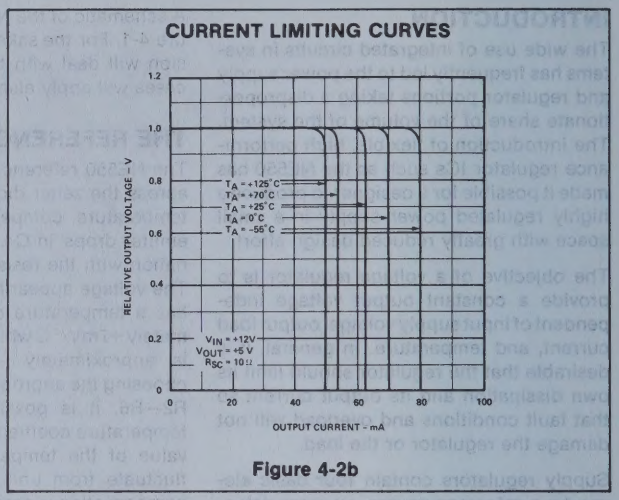


Figure 4-2b

Q11 is more positive (negative) than that of Q12 will lead to an increase (decrease) of current in Q11, a decrease (increase) of current in Q12, and a rise (fall) of the voltage at the base of Q14 and Q15. Thus, a positive voltage change on the base of Q11 will lead to a higher current from V_{OUT}, the emitter of Q15. The effect of voltage changes on the base of Q12 is, of course, the opposite. The voltage gain of the error amplifier is given by

$$AV \cong \frac{RC}{2r_e} = \frac{R_{C12}/\!/R_{C8}}{2kT/qI_E} \qquad (4\text{-}1)$$

This is typically 5000 at room temperature, rising a little at low temperature, and falling slightly at high temperature. High frequency stability is ensured by connecting a capacitor from the compensation pin to the inverting input, giving the amplifier a 6dB/octave roll off. In this manner, external pass elements with arbitrary phase characteristics at high frequency can still be compensated for by rolling off the amplifier.

The error voltage is derived by resistor division of the output voltage. Since the error amplifier inputs will seek a balance between them, the output voltage will attain a value equal to the reference voltage multiplied by the amplifier gain.

The collector voltage of Q12 is set by the nearly constant output voltage. Power supply rejection of the amplifier may be improved by taking the collector of Q11 to the constant voltage of Q14 also.

The availability of both the inverting and non-inverting inputs to the error amplifier allows the regulator to be used in a wide variety of applications.

In some applications where the output is fed back to the non-inverting input, a non-destructive latch-up can occur in Q11. By feeding current into the compensation pin through a diode this phenomenon can be avoided. Those applications requiring the additional diode are shown with the necessary connections.

CONTROL DEVICE

The control element is formed by the pass transistor Darlington pair Q14—Q15. The ultimate current capability of this pair is very high, but the usable current is restricted by packaging and assembly limitations to about 200mA. In general, power dissipation factors lead to more severe limitations, and applications requiring currents in excess of 50mA are best handled with external pass transistors. To this end, the collector of Q15 is brought out separately, allowing an extended range of pass transistor connections to be utilized. These are discussed in the applications sections.

PROTECTION CIRCUITRY

Up to this point the design discussions have applied both to the 550 and μA723 devices. The short circuit protection sections differ slightly. Therefore, the following discussion will not necessarily apply to the μA723.

Isolating the regulator from the load during periods of overload is the function of Q16 and Q18. These two transistors are arranged to form a 5CR device.

Figure 4-2 shows the basic positive voltage regulator configuration. The sense resistor R_{SC} is connected between emitter and base of Q16. When load current increases to such a value as to turn on Q16 the 5CR device turns on removing the 120μA base drive provided by Q8 to Q14, thus isolating the load.

After the SCS turns on, Q16 need only provide the small base current required by Q18 to sustain current limiting. The current at which current limiting occurs is given by:

$$I_{SC} = \frac{V_{sense}}{R_{SC}} \qquad (4\text{-}2)$$

where Isc is the short circuit current and V_{sense} is the V_{BE} of Q16.

Since the V_{BE} of Q16 falls with increasing temperature the short circuit also falls, a desirable trait.

The advantage of incorporating the 5CR device for current limiting lies in foldback limiting the output. That is, the output current under overload conditions drops to a value far below the peak load current capability. This is essential in high current regulators to protect the regulator from excessive power dissipation. The technique of foldback limiting and the resultant locus are illustrated by Figure 4-3. In normal operation of the circuit no current is sourced, but when shut down, a current

$$I_{CL} \cong I_{Q8} \bullet h_{FEL} / (1+h_{FEL}) \qquad 4\text{-}3)$$

is sourced. Bypassing this current through a resistor R_{FB} as in Figure 4-3, a portion, ($I_{CL}R_{FB}$), of the V_{sense} shutdown voltage can be generated regardless of current in R_{SC}, once the device is shut down.

Thus, when Q16 — Q18 are conducting the major portion of IQ8, the shutdown condi-

FOLD BACK CURRENT LIMITING

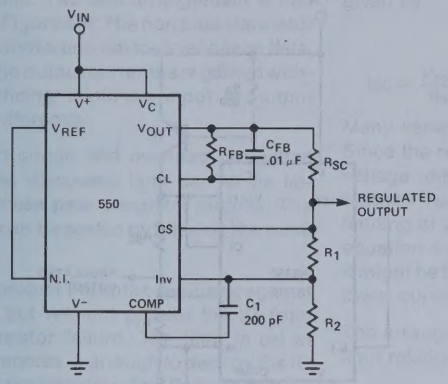


Figure 4-3a

FOLDBACK CURRENT LIMITED OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

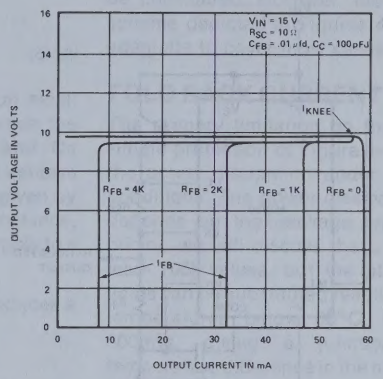


Figure 4-3b

tion changes from equation 4-3 to, (ignoring small terms),

(4-4)

$$I_{SC}R_{SC} + I_{CL} \bullet R_{FB} = V_{sense}$$

Thus, the actual short circuit current can be much less than the peak load current given by equation 4-2. The load current-voltage characteristics of Figure 4-3 are shown in the curve for various values of R_{FB}.

Since the input impedance of the C_L terminal is negative over some range of voltages, it is normally necessary to by-pass R_{FB} with a capacitor to maintain stability if operation in this range is desired. A value of 0.01μF is generally satisfactory.

By increasing R_{FB} to such a value that $R_{FB} \bullet I_{CL} > V_{sense}$, the circuit will shut down completely under overload, and not come back into operation unless the voltage between the C_L and C_S terminals is reduced below V_{sense} by some external means. In general, this is most useful in remote shutdown applications discussed later.

The final feature available in the dual in-line package versions of the NE550 and the μA723 is the zener diode D3 between V_{OUT} and V_Z, (the V_Z output is not available in the L package since there are insufficient pins). This diode is useful in certain applications such as negative regulators, where it is desirable for the output of the amplifier to be level shifted to a point more negative that V_{OUT} is permitted to go (+2V referred to V-). The Zener voltage is typically 6.4V. The use of this feature is discussed in the next section.

APPLICATIONS

Designing basic voltage regulators with high performance IC regulators is relatively straightforward. Each functional block of the regulator should be considered as to its contribution to the system. Basic regulation of an output voltage is achieved by multiplying a reference voltage by the gain of an amplifier. Thus, the error amplifier may be treated as an operational amplifier where the 'virtual ground' and 'zero differential voltage' statements developed in section three apply. The reference voltage is applied to the positive input and a sample of the output voltage is fed back to the negative input via a resistor divider network. Since the junction of R1 and R2 in Figure 4-3 will equal the reference voltage (zero differential rule), the output will be set by the ratio of the resistors. Specifically the output voltage becomes:

$$V_{OUT} = V_{REF}\frac{R1 + R2}{R2} \qquad (4\text{-}5)$$

Each input to the error amplifier requires a small bias current of typically 1μA. Since these currents will be flowing through the input impedances to the amplifier it is possible to generate an error voltage if the impedances to the amplifier are not equal. In addition temperature changes will cause fluctuations in bias current causing the output voltage to drift. Thus, the final design should provide a match of the input impedances both to improve accuracy and temperature stability of the output voltage. The effective impedance of the internal reference voltage of the NE550 is 2kohm. Therefore for best temperature stability the parallel combination of R1 and R2 should be 2kohm.

$$R_S = 2k = \frac{R1 \bullet R2}{R1 + R2} \qquad (4\text{-}6)$$

The design of the regulator should satisfy both equation 4-5 and equation 4-6 simultaneously. Solving both leads to equations 4-7 and 4-8 which express the resistor values as a function of output voltage.

$$R2 = \frac{2000V_{OUT}}{V_{OUT}\text{-}V_{REF}} \text{ OHMS} \qquad (4\text{-}7)$$

$$R1 = \frac{2000V_{OUT}}{V_{REF}} \text{ OHMS} \qquad (4\text{-}8)$$

Having determined the required resistor values, the designer may find that they are not readily available in standard values and some adjustments are necessary. Such changes should maintain the ratio:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R1 + R2}{R2} \qquad (4\text{-}9)$$

The reference voltage of the NE550 is 1.63 volts typically, with a spread of 1.53 volts minimum to 1.73 volts maximum. This variation from unit to unit may require that some portion of R1 or R2 be made adjustable for exact output voltage trimming.

PASS TRANSISTOR CIRCUITS

The next major subject concerns the use of external pass transistor options. These can readily extend the usable output current range of the regulator to many amps and reduce power dissipation in the IC as well. In this way, thermal effects, (discussed later in detail), are minimized.

The simplest circuit is that shown in Figure 4-4. Here, the internal Darlington pass transistor configuration is extended to a triplet by the external npn transistor. For further extension, this external device can be a Darlington, extending the string to a quad.

USE OF EXTERNAL NPN PASS TRANSISTOR

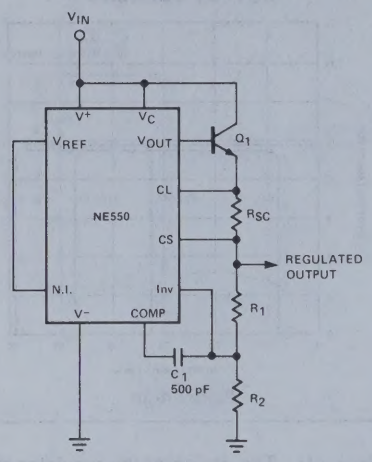
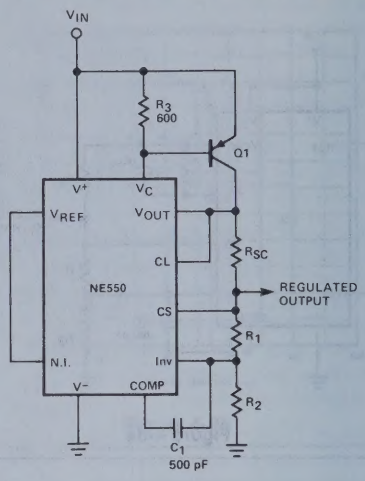


Figure 4-4

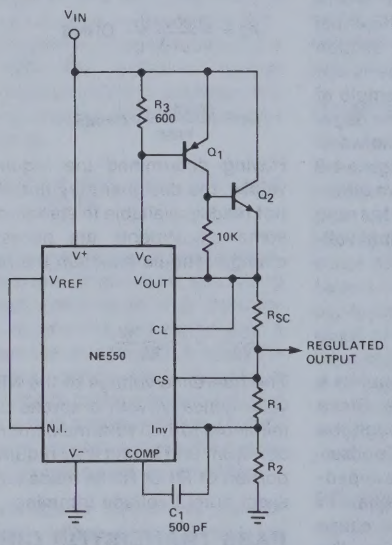
USE OF PNP PASS TRANSISTOR



ALL RESISTOR VALUES ARE IN OHMS

Figure 4-5

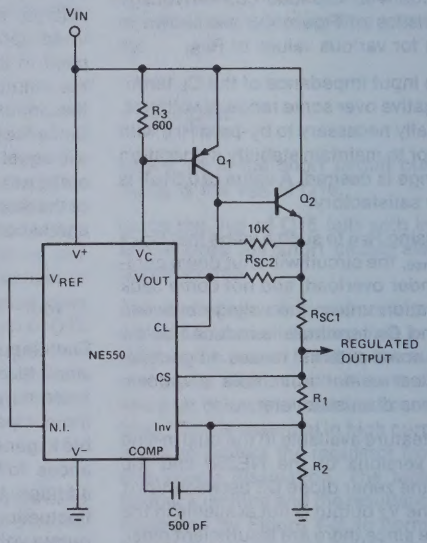
USE OF PNP-NPN PASS TRANSISTOR



ALL RESISTOR VALUES ARE IN OHMS

Figure 4-6

OVERLOAD PROTECTION OF THE INTEGRATED CIRCUIT AND THE PASS TRANSISTORS



All resistor values are in ohms

Figure 4-7

This arrangement has the merit of economy, since npn power transistors are generally cheaper than pnp, but has the disadvantage that the minimum differential voltage between input and output is increased by the V_{BEs} of the external transistors. The load regulation is also somewhat degraded since the error amplifier gain is finite and the V_{BE} drops of the external transistors is a function of load current.

An alternative circuit avoiding the disadvantages mentioned above is shown in Figure 4-5. This circuit uses the pnp transistor whose base drive is obtained from the V_C terminal.

The resistor R3 is used to ensure Q1 turns off under no load conditions, avoiding the excessive buildup of leakage current that can sometimes occur at high temperature. The effect of Q1 is to multiply the h_{FE} of the output transistor in the IC, without increasing the V_{BE}, hence this circuit optimizes the load regulation also. Once again, this device

can be replaced by a Darlington pair, but the V_{BE} buildup begins to affect the differential voltage limit. The best arrangement is that shown in Figure 4-6. The npn pass transistor is driven from a pnp device to enhance beta. Thus, large output currents are gained without sacrificing minimum input to output voltage differential.

The short circuit and overload protection techniques discussed later can all be applied to these pass transistor circuits. The currents can be scaled by altering the value of R_{SC}.

This will protect the entire regulator against overload but will not protect the IC from pass transistor failure. The limit is set at several amperes — enough to destroy the IC — should the transistor fail. Protection from such failure can be provided by the circuit of Figure 4-7.

R_{SC1} performs the main short circuit protection, but R_{SC2} limits the IC output current to a safe value if the pass transistors fail. The normal voltage drop in R_{SC2} should be small compared with the voltage drop in R_{SC1}. This circuit may be modified to include all the protection techniques discussed next.

OVERLOAD PROTECTION

The simple short circuit protection arrangement of Figure 4-2A gives the typical output characteristic illustrated in 4-2B. This shows the variation of limit current with temperature and the sharp knee between the constant voltage and constant current regions. Adequate for most applications, this method has the benefit of simplicity. The value of the short circuit resistor R_{SC} is given by:

$$I_{SC} \simeq \frac{V_{sense}}{R_{SC}} \qquad (4\text{-}10)$$

Many variations of the basic circuit exist. Since the regulator is shut down when the voltage difference between C_L and C_S reaches V_{sense}, a set of resistors to achieve limiting or a locus other than that given by equation 4-10 can be chosen. For instance, it might be beneficial to limit one supply to a lower current level than another.

The arrangement of Figure 4-8 produces a limit relationship

$$I_{L1}R_{SC1} + I_{L2}(R_{SC1} + R_{SC2}) < V_{sense} \qquad (4\text{-}11)$$

This allows a higher limit on output 1 [V_{sense}/R_{SC1} if $I_{L2}=0$] than on output 2 [$V_{sense}/R_{SC1} + R_{SC2}$) if $I_{L1} = 0$], but protects both outputs to less than these limits if the other is carrying current. The price paid is that only one output can be well regulated. The other output has an effective output impedance derived from the R_{SC}'s. If output 1 is stabilized (by tying R1 to it), then the output impedance of output 2 will be R_{SC2} higher; if output 2 is stabilized, then output 1 has a low output impedance, but a high mutual impedance from the load current I_{L2}.

In general, any linear combination of load currents and input or output voltages can be used to set the overload operating conditions. In extreme cases the use of an op-amp summing amplifier to drive C_L or C_S could be considered. However, the simple limit scheme depicted in Figures 4-2 and 4-3 is adequate to cover most cases.

FOLD BACK CURRENT LIMITING

The primary limitation on the use of the simple protection of Figure 4-2 arises from the power dissipation under short circuit conditions. The power dissipation allowed depends on the package type. For simplicity, we will discuss the L package (10 lead T05) values, but the other package limits can be substituted readily. At ambient temperatures below 30°C, this limit is 800mW, giving a junction-to-ambient temperature difference in the neighborhood of 120°C. Above this temperature, derating at 6.8mW/°C, we find at an ambient of 50°C, 680mW, at 75°C, 510mW, at 100°C, 300mW, and at 125°C, 170mW.

Clearly, under short circuit output conditions, the dissipation becomes the product of the full input voltage and the short circuit current. Consider a device with 20V_{IN}, 15V_{OUT}, and 60mA current limit, operating at ambient temperature of $T_A = 25°C$. The standby current will be assumed to be 2mA or a dissipation of 40mW. The pass transistor dissipation just before overload is 5V at 60mA, or 300mW, for a total of 340mW, well within ratings. But under short circuit conditions, the initial pass transistor dissipation is 20V at 60mA, or 1.2W (a total of 1.24W), in excess of the allowed ratings. If the 340mW

MODIFIED SHORT CIRCUIT PROTECTION

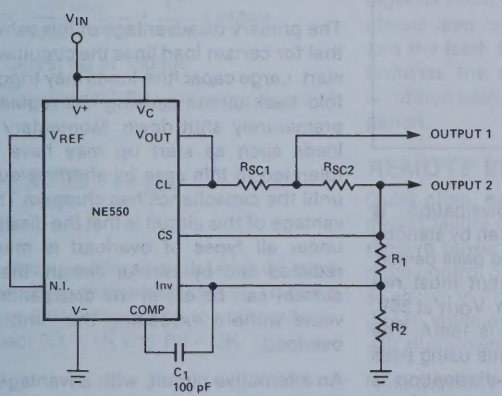
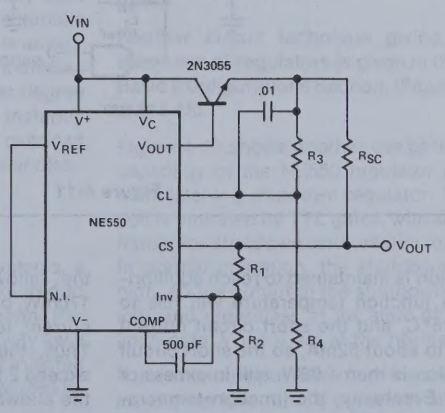


Figure 4-8

SCHEMATIC OF 10 VOLT-1 AMP REGULATOR



$$I_{KNEE} = \frac{V_{OUT}\,R_3 + (V_{SENSE} - I_{CL}\,R_3)(R_3 + R_4)}{R_4\,R_{SC}}$$

$$I_{SC} = \frac{(R_3 + R_4)(V_{SENSE} - I_{CL}\,R_3)}{R_{SC}\,R_4}$$

Figure 4-9a

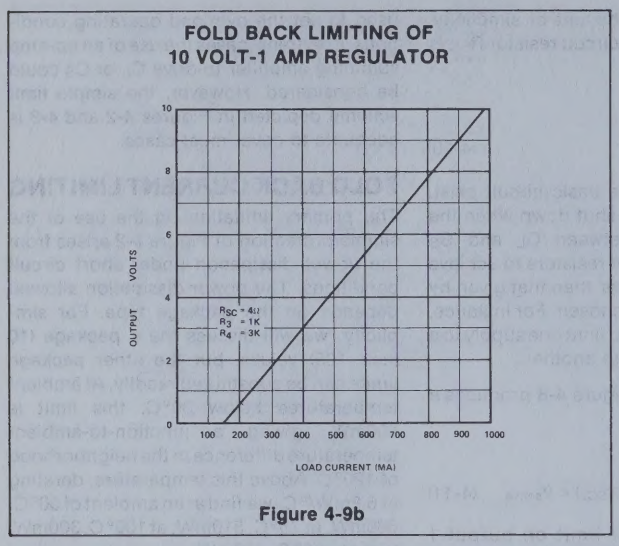


Figure 4-9b

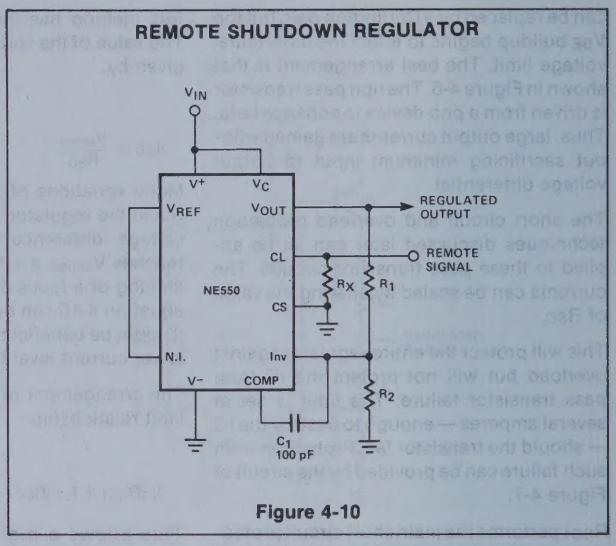


Figure 4-10

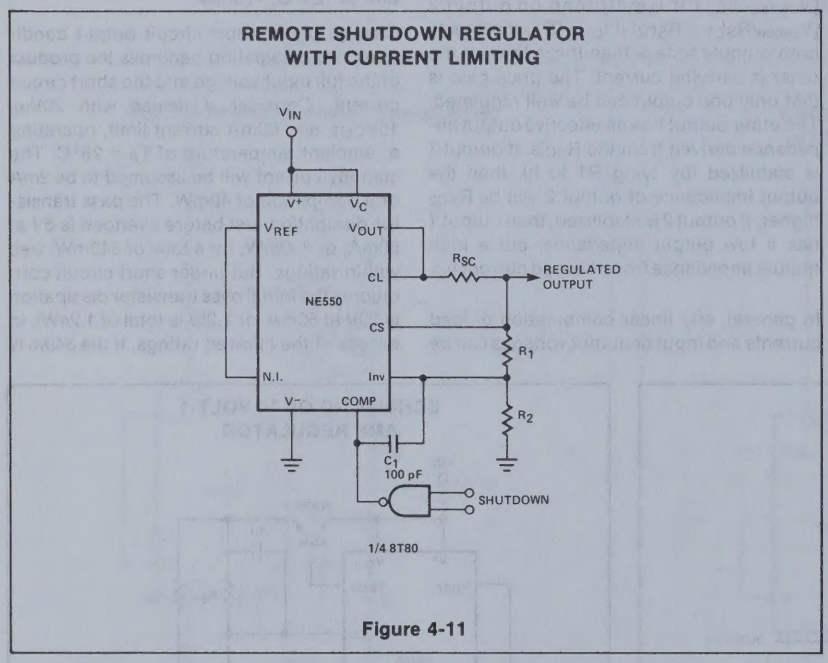


Figure 4-11

dissipation is maintained to reach equilibrium, the junction temperature will rise to about 75°C, and the short circuit current will fall to about 52mA, so the short circuit dissipation is then 1.08W, still in excess of ratings. Eventually, the junction temperature will reach 150°C, where the short circuit current will be about 37mA, and the total dissipation about 800mW, just acceptable at an ambient temperature of 25°C. High ambient temperature will degrade the situation. Taking a worst case situation, with V_{IN} = 40V, T_A = 125°C, and I standby=2.0mA, the allowable package dissipation is 170mW, of which 80mW is taken by standby current, leaving 90mW for the pass device. Thus, the short circuit current must not exceed 2.2mA. However, with V_{OUT} at 35V, the allowable output current is 18mA. The same problem arises in circuits using pass transistors, except that the dissipation is transferred to the pass transistor itself.

The solution to this problem is found in foldback current limiting circuits. The NE550 device is particularly well suited to this type of circuit. The basic NE550 foldback circuit is shown in Figure 4-3. The internal operation of this circuit was described earlier and will not be repeated here. The current that can be drawn without significant drop in V_{OUT} called the knee current, (I_{knee}), can be considerably greater than the short-circuited output current, I_{SC}. The equations controlling the currents are, for I_{knee},

$$I_{knee} = V_{sense}/R_{SC} \quad (4\text{-}12)$$

and for I_{SC},

$$I_{SC} = (V_{sense} - I_{CL}R_{FB})/R_{SC}$$
$$= (V_{sense} - R_{FB} \bullet 125\mu A)/R_{SC} \quad (4\text{-}13)$$

where I_{CL} is 125μA.

The primary disadvantage of this scheme is that for certain load lines the circuit will not start. Large capacitive loads may trigger the fold back circuit causing the regulator to prematurely shut down. Momentary overloads such as start up may have to be tolerated in this case by shorting out R_{SC} until the capacitance has charged. The advantage of this circuit is that the dissipation under all types of overload is markedly reduced and by careful design, the knee current can be set at the dissipation limit value without exceeding this limit under overload.

An alternative circuit, with advantages and disadvantages of its own, is shown in Figure 4-9. This circuit can be used with the 550 and the μA723 devices, and is basically a variant of the "linear combination of voltage and current" type.

Here, the combination is of load current and output voltage, such that

$$V_{sense} = \left[V_{OUT} + I_{knee} \bullet R_{SC}\right]\left[\frac{R4}{R3+R4}\right] - V_{OUT} + I_{cl}R3 \quad (4\text{-}14)$$

(where $I_{cl} \approx 125\mu A$ for the NE550)

Solving for I_{knee} we find

$$I_{knee} = \frac{(R3 + R4)(V_{sense} - I_{cl}R3) + V_{OUT}R3}{R_{SC}R4} \quad (4\text{-}15)$$

The short circuit current is less than the full load or "knee" current and is described by

$$I_{sc} = \frac{(R3 + R4)(V_{sense} - I_{cl}R3)}{R_{SC}R4} \quad (4\text{-}16)$$

The parallel combination of R3 and R4 form a feedback resistor so the impedance should be less than 1 kohm. Values larger than 1 kohm cause the inherent foldback characteristic of the NE550 to latch back before assuming the linear load line of Figure 4-9.

Ignoring small quantities the resistor values of R3 and R4 are selected from the ratio

$$\frac{R4}{R3} = \frac{(V_{OUT}\ I_{sc})}{V_{sense}\ (I_{knee} - I_{sc})} - 1 \quad (4\text{-}17)$$

A design example is included here to illustrate the design procedure.

Design Example
18 Volt Input
10 Volts Output @ 1 Amp
Foldback Current Limiting

Step 1 Compute minimum I short circuit with I_{knee} = 1 amp by

$$\frac{I_{sc}}{I_{knee}} > \frac{2V_{sense}}{V_{sense} + V_{OUT}} > \frac{1.2}{10.6} > 113mA$$

Step 2 Select I_{sc} at 150mA

Step 3 Calculate R3/R4 ratio using equation 4-17

$$\frac{R4}{R3} = \frac{(10)(150)}{.6\ (.850)} - 1 = 2.94$$

Step 4 Because R3 in parallel with R4 must be less than 1 kohm select R3 at 1k. Thus, R4 becomes 2.94K. Rounding to standard values select R3 = 1K and R4 = 3K.

Step 5 Using equation 4-16 and solving for R_{SC} by

$$R_{sc} = \frac{(4)(.475) + 10}{3} = 3.96\Omega$$

Step 6 Select standard value of R_{SC} = 4 ohms

Step 7 Recalculate I_{knee} using the selected standard values by equation 4-15

$$I_{knee} = \frac{(4)(.475) + 10}{4.3} = .991\ amp$$

Step 8 Recalculate I_{sc} using selected values by equation 4-16

$$I_{sc} = \frac{(4)(.475)}{12} = 158mA$$

Figure 4-9a illustrates the final regulator arrangement with the shut down locus given by Figure 4-9b. Excellent alignment of calculated and measured results was obtained. The foldback characteristic is of the type shown in Figure 4-9b and should be contrasted with that of Figure 4-3.

Two distinct disadvantages of this circuit are readily apparent. First, the voltage drop across R_{SC} becomes large and adds directly to the minimum differential voltage required between V_{IN} and V_{OUT}. This in turn causes excessive power consumption in the regulator since the power dissipated by the pass transistor is equal to the input-output voltage differential multiplied by the peak load current.

Secondly, since R_{SC} is larger than normal, and must handle all load current, its wattage must be increased. It should be noted that load regulation will be adversely affected as well.

With these disadvantages in mind, large peak current regulators are usually best protected by the foldback characteristic shown by Figure 4-3. This circuit is advantageous because R_{SC} is small and therefore affects load regulation to a smaller degree and the latch back characteristic instantly switches the regulator from an overload condition back into one of safe power dissipation.

REMOTE SHUTDOWN

Quite often, especially in large systems, a circuit failure or alarm may be required to remove power from the main system. Remote control of the NE550 is relatively easy as shown in Figure 4-10. A current injected into R_x sufficient to develop V_{sense} across R_x will shut down the regulator.

Note that for the NE550 if $I_{cl} \bullet R_x$ is greater than V_{sense} ($I_{cl} = 125\mu A$), the regulator will latch in the shut down mode until R_x is sufficiently reduced. This action can be beneficial in avoiding the requirement for an external latch should the initial remote command be removed when the supply shuts down. Use of this technique will be discussed in more detail later.

A remote control circuit which retains any of the current limiting protection schemes so far discussed and adds control via a standard TTL logic level is shown in Figure 4-11. The gate listed in the figure is a suitable open collector gate with high voltage breakdown.

Selection of any other open collector gate should be based upon a breakdown at least 2 volts higher than the maximum V_{OUT} and with output leakage well below 50μA.

Naturally, no gate inputs or other loads should be tied to the line, but any number of gates meeting the above needs in total may be used in a wired-OR configuration. Tri-state outputs may not be used. Note that if the normal V_{OUT} is high, the load capacitance may be discharged through the reverse emitter base diodes of the pass transistors and the gate. This current can be limited by a series resistor not to exceed 2 kohms. Remote shut down is especially useful to ensure turn off of multiple supplies if any one supply becomes overloaded.

A schematic showing one possible technique for doing this is shown in Figure 4-12, where the use of open collector AND gates gives a simple logic structure. The diodes are not needed for supplies not exceeding the V_{CC} logic level, and it has been assumed that each supply has a load adequate to turn on the gate input.

The string may be reset by shutting down the V_{CC} supply to the gates, which must be separate from the string of controlled supplies.

Another circuit technique giving linked shutdown of regulators is given in the Non-Basic Configurations Section, (Figures 4-17 and 4-18).

Figure 4-13 shows another use of the latch capability of the NE550 regulator in a remote latching shutdown regulator. The circuit is operated by TTL gates, with separate inputs for shutdown and unlatch (or reset). In normal operation, the shutdown line is high, so the output of the shutdown gate is low, and regardless of the state of the unlatch gate, V_{OUT} is set at the normal level.

If the unlatch input is low, and the shutdown input goes low, the CL input will be pulled up by R3 (and R4 if needed), the regulator will shut down, and the current sourced from the CL terminal will latch the regulator shutdown, even after the shutdown line goes high again, while the unlatch input remains low. When the unlatch line goes high, the sourced current is taken through

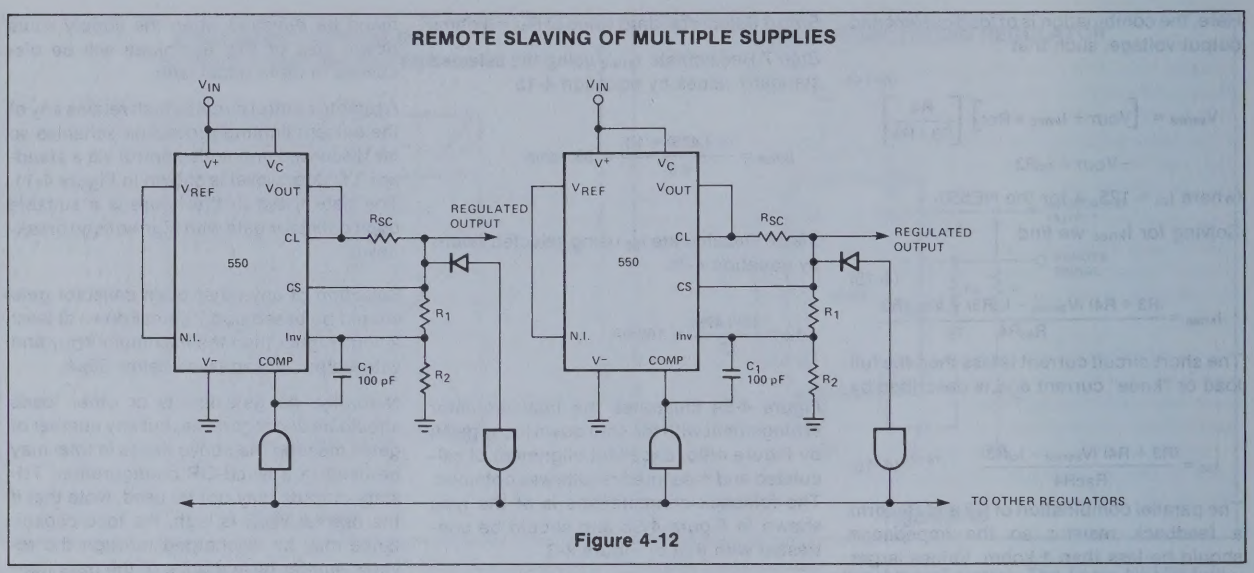


Figure 4-12

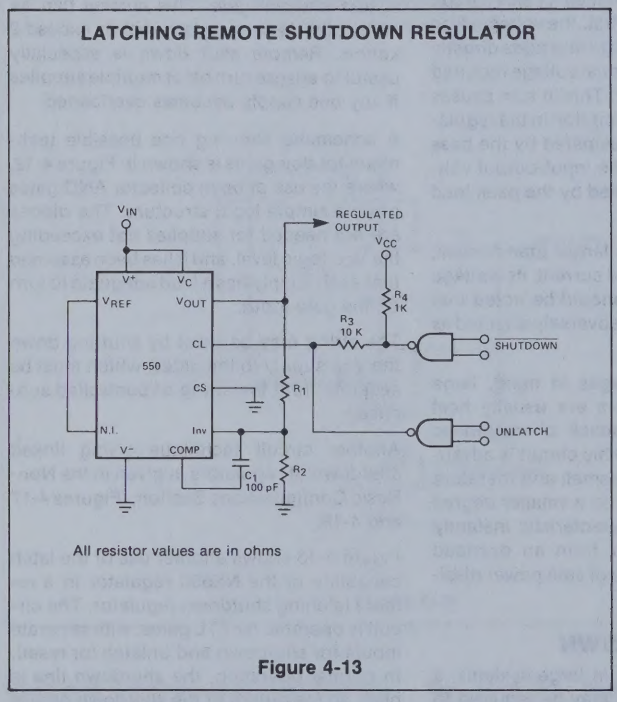


Figure 4-13

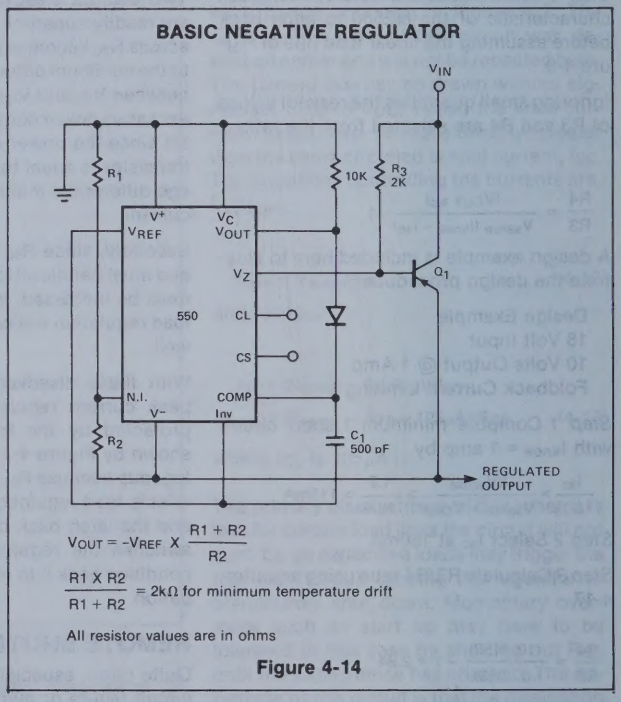


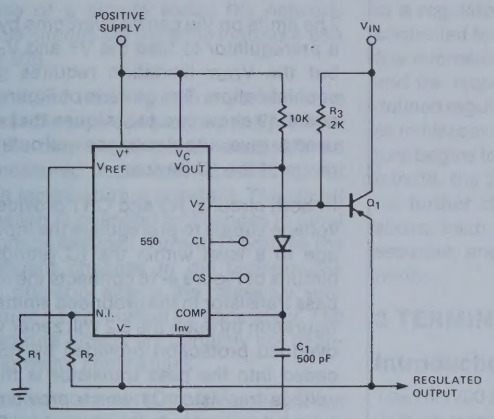
Figure 4-14

the unlatched gate, the CL terminal drops below V_{sense}, and the regulator resets. The figure lists some suitable gates, but any open collector gate can be used for the unlatch gate, and any gate at all for the shutdown gate. If an active pullup gate is used in the latter position, R4 may be omitted. Using 8T90 gates, a pulse width into the shutdown input of 50ns was found adequate to ensure latched shutdown, although the regulator output in the configuration tested did not decay fully until more than 1μs after the pulse. Since this circuit uses the internal shutdown components, additional short circuit protection would require an external transistor, connected to the compensation terminal. This basic arrangement can also be used with MOS logic driving the C_L input, although diode gating will normally be needed to ensure correct operation.

NON-BASIC CONFIGURATIONS

All the circuits discussed so far have been variations on the basic positive voltage regulator. There are many other circuit configurations that can be used, however, including negative voltage regulators, floating regulators (for voltages exceeding the maximum voltage ratings) and switching regulators for highly efficient regulation. Many of

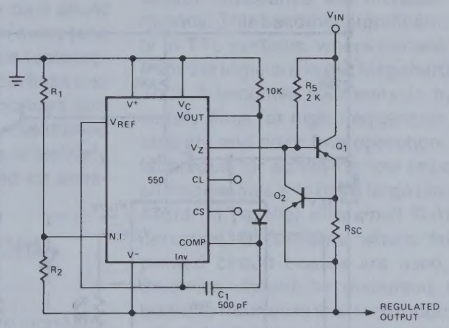
NEGATIVE REGULATOR (LESS THAN -8.5 VOLTS)



All resistor values are in ohms

Figure 4-15

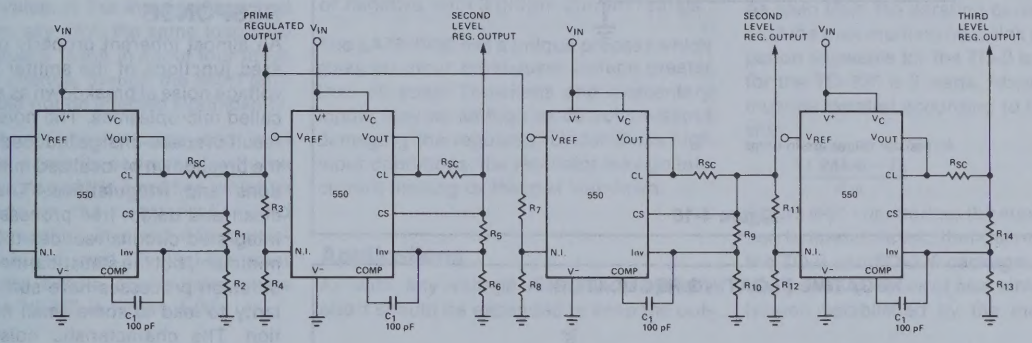
PROVIDING NEGATIVE REGULATOR OVERLOAD PROTECTION



All resistor values are in ohms

Figure 4-16

CASCADING REGULATORS



All resistor values are in ohms

Figure 4-17

the pass transistor and overload protection circuits discussed in the previous section are applicable to these configurations also.

NEGATIVE REGULATORS

The basic negative voltage regulator circuits are shown in Figure 4-14.

Note that for units not having the V_Z terminal (those in 10 pin packages) an external 6.2V Zener can be used.

The inverting and non-inverting input connections are reversed, and the pass transistor Q1 acts as a level shifted emitter follower from V_{OUT} to drive the output. The regulator is driven from its own output, so the line regulation is excellent, the load regulation is controlled by the h_{FE} of Q1 and the load regulation of the IC. R3 must be of sufficient value to drive the maximum load current through Q1 at the minimum input voltage, and large enough not to draw more than 10mA through the internal Zener (the V_Z terminal) at minimum load and maximum V_{IN}. This places a lower limit on the h_{FE} of Q1, which for large currents may need to be a Darlington pair or equivalent.

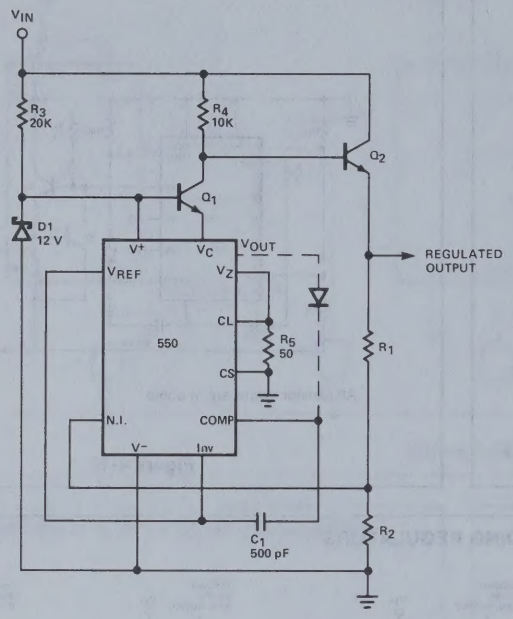
The supply voltage for the regulator is derived from the output voltage. For this reason the output voltage available is limited to values more negative than -8.5 volts.

A circuit such as in Figure 4-15 overcomes this limitation but assumes the presence of a positive supply. This is usually acceptable since the majority of negative regulator requirements arise from the need for symmetrical positive and negative voltages.

The diode and resistor frequently shown in negative regulator applications is necessary to avoid a possible forward base-collector bias on Q12 of Figure 4-1. Should forward base-collector bias occur, the regulator will latch up preventing regulation at initial power up. The diode can be a small signal type with a forward current of 100μA. Diode current flows only during initial turn on and sees approximately two volts reverse bias under normal operation. The resistor should be of sufficient value to allow approximately 100μA to flow into the V_{OUT} terminal.

Short circuit protection of negative regula-

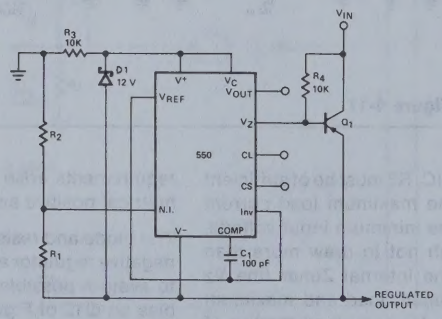
POSITIVE FLOATING REGULATOR



All resistor values are in ohms

Figure 4-18

NEGATIVE FLOATING REGULATOR



All resistor values are in ohms

Figure 4-19

tors cannot be implemented with the circuits previously described because of the inversion of the error amplifier inputs.

Protection can be provided with the addition of a transistor as illustrated by Figure 4-16. Note that the saturation voltage of Q2 at the maximum current through R5 must be less than the V_{BE} of Q1. Other components are not critical.

FLOATING REGULATORS

So far only output voltages less than the 40 volt maximum ratings of the NE550 have been covered. The maximum voltage limitation can be overcome by using floating regulator techniques.

The limits on V_{IN} can be overcome by using a preregulator to feed the V+ and V_C lines, but the V_{OUT} limitation requires greater sophistication. The circuits of Figures 4-18 and 4-19 show two techniques that can be used to give output voltages well outside the range of the IC device.

In both circuits, R3 and CR1 provide a low voltage supply to preregulate the input voltage to a level within the IC ratings. The circuits of Figure 4-18 connects the internal pass transistor in the grounded emitter configuration through the 6.2 volt zener V_Z with overload protection provided by R5. Cascaded into the pass transistor is the high voltage transistor Q1 which provides level translation and voltage control to Q2, the pass transistor.

Short circuit protection can be arranged by removing base drive from Q2 is desired.

NOISE, TEMPERATURE EFFECTS, AND TRANSIENT RESPONSE

An almost inherent property of reverse biased junctions of the emitter base type is voltage noise at breakdown as a result of so-called microplasmas. The noise arises as a result of space-charge induced instability of the breakdown of localized minor imperfections and irregularities. The inherently clean and defect free processing used for integrated circuits reduces this effect to a minimum, but the statistical inevitabilities of diffusion processes have sufficient irregularity to lead to some small noise generation. The characteristic noise pattern is displayed as step-function current change as each microplasma switches on and off. Each microplasma switches at roughly constant voltages, leading to approximately constant voltage transitions.

Since the reference voltage for the NE550 is derived from the breakdown of the emitter-base junction, this noise will appear at the reference terminal. Transformed by the internal network between the zener diode and the reference terminal, this is the major component of noise in the regulator. For applications where the noise level could be troublesome, it can be reduced by putting a low pass filter between the zener and the amplifier input. The low frequency component of the noise is quite small. Since the internal reference impedance of the NE550 is 2KΩ, placing a capacitor between V_{REF} and ground will generally be all that is required.

In circuits where the reference is divided down, the divider impedance provides some

effective series resistance, but in other applications better results may be obtained by the use of a simple series RC network. Suitable circuits are shown in Figures 4-86A and 4-86B.

The line and load regulation performance discussed in previous sections and presented in the data sheets are all values defined and measured under such conditions that the die temperature is constant. The circuit dissipation is changed by changes in input line voltage and load current. Therefore, the consequent changes in die temperature, which primarily affects the reference voltage, must be accounted for separately. The temperature effects are certainly not negligible in many applications.

A regulator operating at $10V_{in}$ and $5V_{out}$ with a load current that steps from 1mA to 50mA will have a short time (1-10msec) output voltage change of typically under 3mV. The dissipation increases, however, by 250mW, leading to a temperature rise of about 25°C at the die. With temperature coefficient of 0.005%/°C, this leads to an output voltage change of 6mV, twice the short time value. If the input voltage had been higher, say 15V, the same load step would eventually result in about four times the voltage change, though the short term change would not be affected significantly.

The effects of transient line and load changes are primarily concerned with the impulse response of the amplifier, which in turn depends on the compensation and external connections involved in the particular circuit being used. Typical transient responses for simple configurations are given for the NE550 in Figure 4-20.

There are three effects to be considered, then, upon imposition of a line or load step to a regulator circuit; the initial reaction is controlled by the transient response. After a few microseconds, the transient dies away and the response becomes the data sheet defined regulation. After a time of many tens of milliseconds, the changing die temperature begins to take effect. After perhaps one minute, the die temperature stabilizes and no further changes occur. As mentioned above, each of these effects is effectively separate, and should be allowed for separately.

3 TERMINAL REGULATORS

Introduction

The 78HV00 series regulators are monolithic three terminal devices intended for fixed voltage outputs. Since no external elements are required they are excellent candidates for PC card and subsystem regulation. With the use of these devices much system crosstalk and power supply distributed noise can be eliminated. These devices are available in 5, 6, 8, 12, 15, 18 and 24 volts, positive or negative, with 3 output current ratings.

The μA78HV00 has a unique process which gives an input breakdown voltage greater than 60 volts. Transients and momentary inputs may be as high as 60 volts without damaging the regulator. Under these high input conditions, the regulator may go into current limiting or thermal shutdown.

Applications

As with any voltage distribution system, effort should be expended to keep the output impedance of three terminal regulators as low as possible.

Possessing 20 to 30 milliohms output impedance at low frequencies, the regulator's output impedance will increase with frequency. This becomes significant, especially in TTL systems, where current impulses from the logic are in the Megahertz regions. Thus it becomes necessary to bypass the supply lines for high frequencies to insure stability and error free operation. The best technique for achieving low impedance at all frequencies is to use a large tantalum (10-47μfd) in parallel with small (0.01μfd) disc ceramics. In systems where fairly large printed circuit boards are used, the disc ceramics should be disbursed upon the board to neutralize the trace inductance. No other stabilization techniques should be required.

Thermal Limitations

The maximum allowable junction temperature and the ambient temperature expected determine whether a heat sink will be required for a particular regulator application.

As seen from the derating curves of Figure 4-32 the maximum no heat sink power dissipation allowable for the TO-3 is 3 watts and for the TO-220 is 2 watts. Above 25°C this must be derated according to the relationship

$$\frac{T_J(MAX) - T_A}{\Theta_{JA}} \qquad (4\text{-}18)$$

Figure 4-21 summarizes the maximum junction temperature and thermal resistivities of the TO-3 and TO-220 packages. The power dissipation qualities of heat sinks are usually well established by the manufacturer.

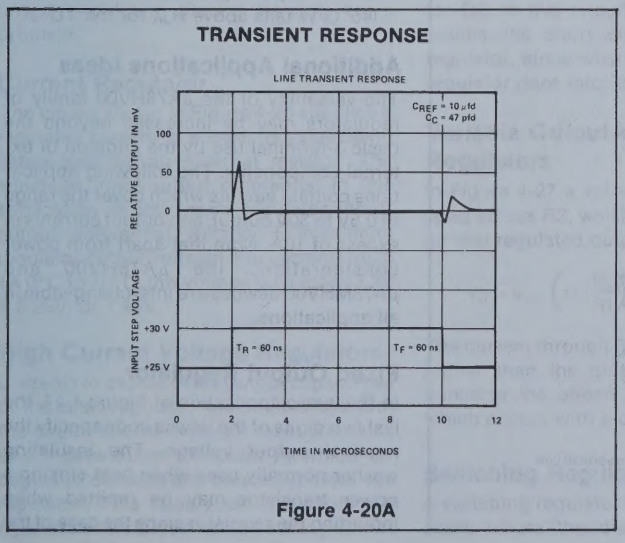


Figure 4-20A

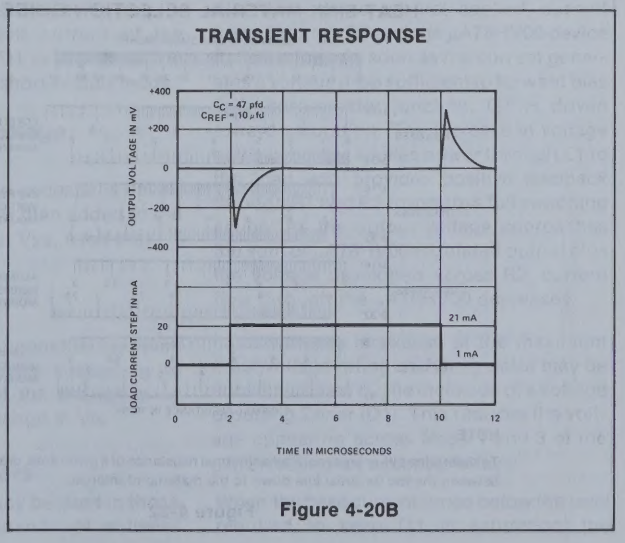


Figure 4-20B

SERIES PACKAGE	78HV00 TO-3	78HV00C TO-3	78HV00C TO-220	78MHV00 TO-39	78MHV00C TO-39	78MHV00C TO-220	UNIT
Maximum junction temperature, T_J(MAX)	150	125	125	175	175	125	°C
Minimum ambient temperature, T_J(MIN)	-55	0	0	-55	0	0	°C
Thermal resistance junction-to-case, Θ_{JC}	4	4	4	20	20	5	°C/W
Thermal resistance junction-to-case, Θ_{JA}	35	35	50	150	150	50	°C/W
Maximum allowable dissipation, P_D(MAX)	15	15	15	5	5	5	W

Figure 4-21

Since the common terminal of these devices is common they may be bolted directly to the chassis, using the surface area as the heat sink.

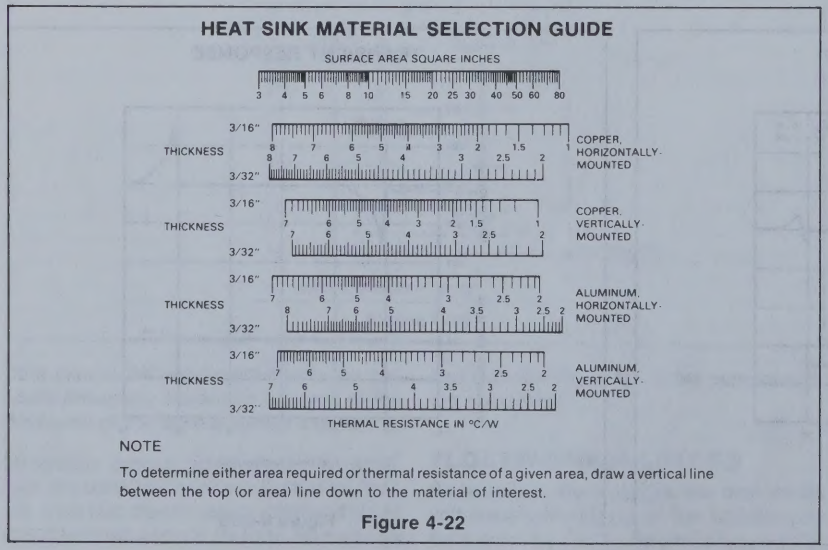
Figure 4-22 provides a selection chart which relates surface area of the chassis material to the thermal resistivity. It should be noted that the surface area refers to both sides of the material.

In order to find a thermal resistivity scribe a vertical line from the surface area across the appropriate material.

Heat Sinks

As a further aid in determining which package/heat sink combination is best suited to a given application, the following nomograph (Figure 4-24) solves for Θ_{JA} from basic current, input/output voltage differential and ambient temperature information. The package thermal resistances have been superimposed on the Θ_{JA} line E. If the required Θ_{JA} is less than Θ_{JC} for a package, then that package cannot be considered. Even if an infinite heat sink were possible, the junction temperature would exceed 125°C. If the required Θ_{JA} is greater than Θ_{JA} for a package, that package may be used without a heat sink. In all other cases a package/heat sink combination is necessary. Subtract Θ_{JC} for the preferred package from the required Θ_{JA} to arrive at the necessary heat sink thermal resistance Θ_{HS}.

To use the nomograph, select the maximum load current on Line A and the maximum input/output voltage differential on Line D. The line joining these points intersects Line B at a point representing the maximum power dissipation. Join this Line B intersection to a point on Line C representing the maximum expected ambient temperature. Extend this line so it intersects Line E. The Line E intersection represents the total junction-to-ambient thermal resistance required for the particular application. If the Line E intersection falls above the junction-to-ambient thermal resistance, Θ_{JA}, no heat sink is required.



NOTE

To determine either area required or thermal resistance of a given area, draw a vertical line between the top (or area) line down to the material of interest.

Figure 4-22

To determine the thermal resistance of a heat sink, subtract the junction-to-case thermal resistance, Θ_{JC}, of the selected package from the Line E intersection.

- For TO-39, subtract 20°C/W
- For TO-3, subtract 4°C/W
- For TO-220, subtract 4°C/W

Example:

Choose a regulator to supply 275mA (max) with an input/output voltage differential of 6V (max) at an ambient temperature of 50°C (max). Join the 275mA point on Line A to the 6V point on Line D. The intersection with Line B gives a power dissipation of 1.7W. Join 1.7W to the 50°C point on Line C and extrapolate to an intersection with Line E. This gives a total junction-to-ambient thermal resistance requirement of 45°C/W. The regulator package choices are

- A TO-39 package with a heat sink of 25°C/W thermal resistance (subtract 20°C/W Θ_{JC}).
- A TO-220 package with a heat sink of 41°C/W thermal resistance (subtract 4°C/W Θ_{JC}).
- A TO-3 package with no heat sink (45°C/W falls above Θ_{JA} for the TO-3).

Additional Applications Ideas

The versatility of the μA78HV00 family of regulators may be increased beyond the basic 3-terminal use by the addition of external components. The following applications contain circuits which cover the range of 0.5V to 30V output, and output currents in excess of 10A. Note that apart from power considerations the μA78HV00 and μA78MHV00 devices are interchangeable in all applications.

Fixed Output Regulator

In this basic application of Figure 4-24, the last two digits of the device code specify the nominal output voltage. The insulating washer normally used when heat-sinking a power transistor may be omitted when mounting the regulator since the case of the

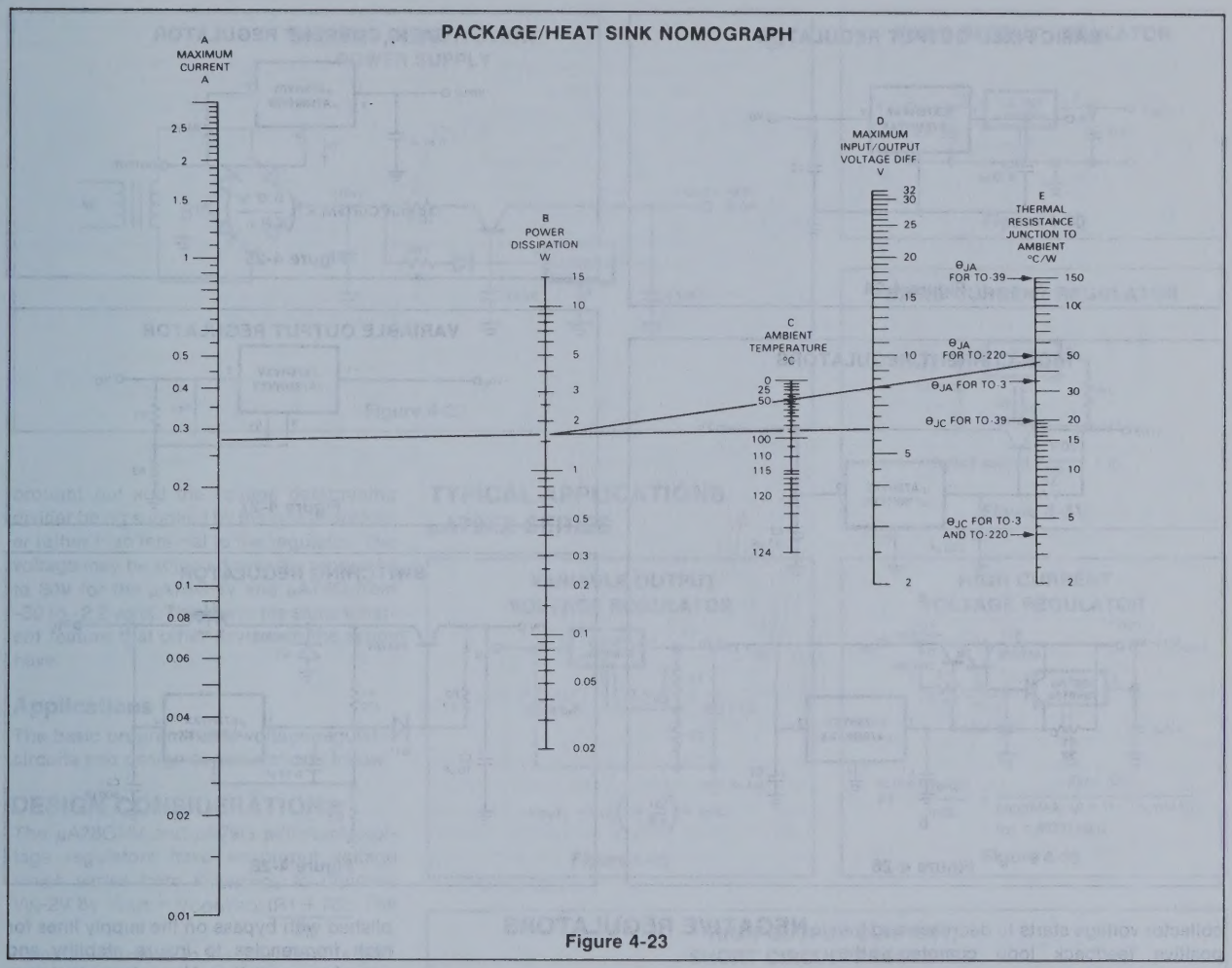


Figure 4-23

device is at ground potential. This is true unless circulating ground currents are a problem.

Current Regulator

The circuit shown in Figure 4-25 supplies a regulated current to a load, its value being determined by an external resistor. The minimum input/output differential in this application is (minimum regulator input/output differential voltage) + (maximum regulator output voltage). For currents up to 1A 0° C to 70° C, this voltage is typically 2.2V + 5.25V, or 7.45V.

High Current Voltage Regulators

Currents in excess of the output capabilities of the basic regulator can be obtained with the circuit shown in Figure 4-26. The value of R1 determines the point at which Q1 begins to conduct and hence bypasses the regulator. This supply can be protected against a short circuit load by adding a short circuit sense resistor, R2, and a pnp transistor Q2. In this circuit Q2 must be able to handle the short circuit current of the regulator, since when Q1 is bypassed, the regulator goes into its short-circuit mode.

Variable Output Voltage Regulators

In Figure 4-27 a voltage pedestal is developed across R2, which is then added to the normal regulated output V_{XX}, such that

$$V_O = V_{XX}\left(1+\frac{R2}{R1}\right)+I_qR2$$

The current through R1 should be set much higher than the quiescent current I_Q to minimize the effects of the change in I_Q which occurs with a change in V_{IN}.

Switching Regulators

A switching regulator may be used in those cases where the dissipation of a linear regulator is excessive. Figure 4-28 shows that when power is first applied, current flows through R3 and the μA78HV00 device to the output. As soon as the current generates a voltage drop sufficient to forward bias Q1's base-emitter junction, Q1 is driven toward saturation. The increase in voltage at the collector applies power through L1 to the load and provides positive feedback through R1 and R2 to assure a full switching action. As the output voltage approaches the sum of μA78HV00 regulated output plus the voltage developed across R2, current flow through the μA78HV00 decreases.

Input voltages in excess of the maximum input voltage rating of the regulator may be accommodated by the inclusion of a voltage dropping Zener (D1). This reduces the voltage appearing across leads 1 and 3 of the μA78HV00 to an acceptable level.

When the base current drops below the level required to keep Q1 in saturation, the

BASIC FIXED OUTPUT REGULATOR

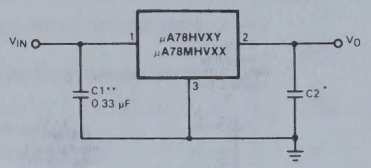
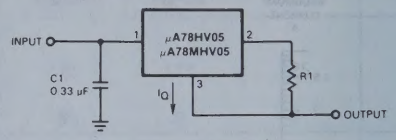


Figure 4-24

BASIC CURRENT REGULATOR



$$\text{Output Current} = \left(\frac{5.0\ V}{R1}\right) + I_Q$$

Figure 4-25

HIGH CURRENT REGULATORS

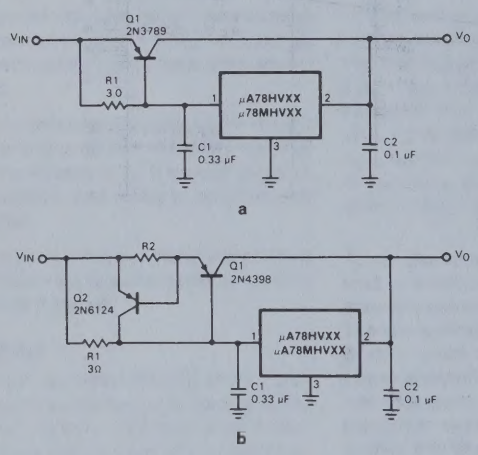


Figure 4-26

VARIABLE OUTPUT REGULATOR

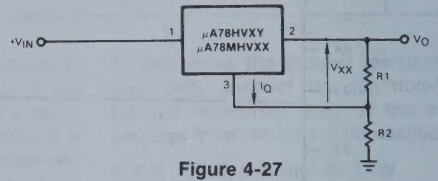


Figure 4-27

SWITCHING REGULATOR

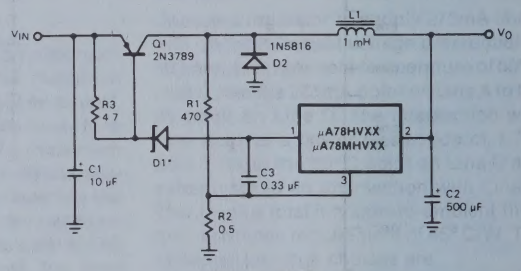


Figure 4-28

collector voltage starts to decrease and the positive feedback loop completes the switching action.

μA78HV14

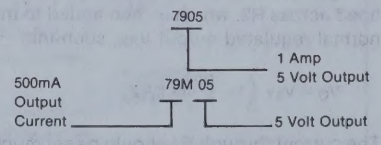
There is a sufficient requirement for a power supply output voltage of 13.8 volts. Therefore, Signetics Analog now offers the μA7814 type 1 amp three terminal regulator with 13.8 volts nominal output.

One of the main requirements for this 13.8 volt regulator is for AC line operation of automotive type equipment. With the increase in the number of CB sets and the servicing required on CB, AM/FM stereo radio, the battery substitution power supply is becoming more prevalent. Another major need for battery substitution power supplies is in the home operation of the portable automotive equipment. The portable CB can be removed from the vehicle to prevent theft and also utilized in the home with a battery substitution power supply using the μA78HV14.

NEGATIVE REGULATORS

Introduction

The μA79 series regulators are monolithic three terminal devices intended for negative fixed voltage outputs. They are an excellent choice for PC card and subsystem regulation due to their self-contained simplicity. These devices are available in negative 5, 6, 8, 12, 15, 18 and 24 volts. The voltage and power output ranges are designated as follows:



Voltages other than those listed are also available upon special order.

Applications

As with the μA78 voltage regulators, effort should be made to keep the output impedance as low as possible. This is accomplished with bypass on the supply lines for high frequencies to insure stability and error-free operation. Use a large tantalum (10-47μfd) in parallel with a small (.01μfd) disc ceramic. Output bypass capacitors will improve the transient response of the regulator. A good high frequency ceramic or tantalum of 1μf will generally suffice. Keep lead lengths as short as possible.

All of the applications for Signetics positive regulators can be used with the negative regulators. The polarities are inversed, the sense diode is reversed and the pnp's are replaced with NPN transistors. Specific circuit configurations are shown in figures 4-29 and 4-39.

PROGRAMMABLE REGULATORS

Introduction

The μA78GHV and μA79G are positive and negative programmable regulators respectively. They are identical to their μA78HV and μA79 counterparts with the exception to the reference to the error amplifier being

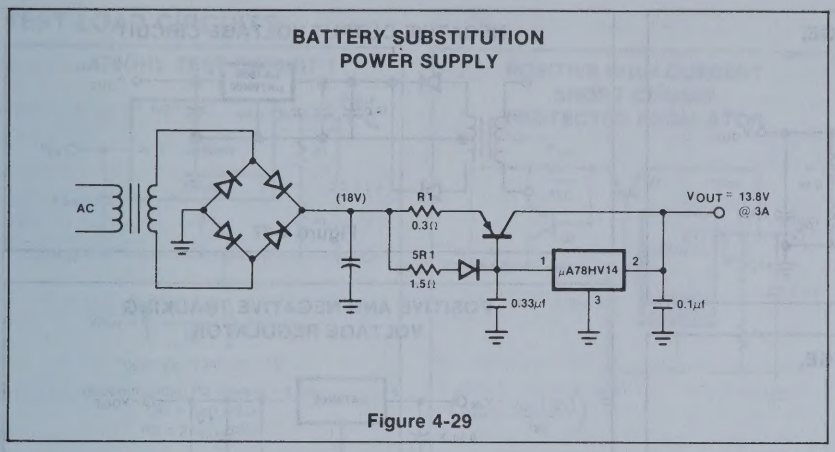


Figure 4-29

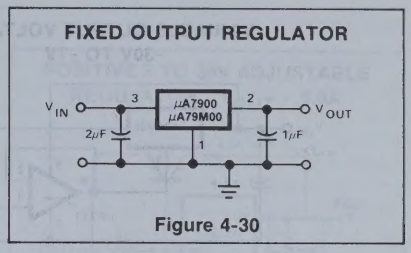


Figure 4-30

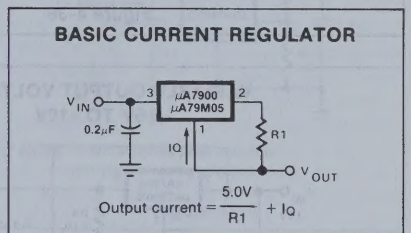


Figure 4-31

brought out and the voltage determining divider being supplied by the circuit designer rather than internal to the regulator. The voltage may be adjusted over the range of 5 to 30V for the μA78GHV and μA79G from -30 to -2.2 volts. They have the same inherent feature that other devices in the series have.

Applications

The basic programmable voltage regulator circuits and design considerations follow.

DESIGN CONSIDERATIONS

The μA78GHV and μA79G adjustable voltage regulators have an output voltage which varies from $V_{CONTROL}$ to typically V_{IN}-2V by $V_{OUT} = V_{CONTROL}\frac{(R1 + R2)}{R2}$. The nominal reference in the μA78GHV is 5.0V and μA79G is -2.23V. If we allow 1.0mA to flow in the control string to eliminate bias current effects, we can make R2 = 5kΩ in the μA78GHV. The output voltage is then: V_{OUT} = (R1 + R2) V, where R1 and R2 are in KΩs.

Example: If R2 = 5kΩ and R1 = 10kΩ then V_{OUT} = 15V nominal, for the μA78G: R2 = 2.2kΩ and R1 = 12.8kΩ then V_{OUT} = -for the μA79G.

By proper wiring of the feedback resistors, load regulation of the devices can be improved significantly.

Both μA78G and μA79G regulators have thermal overload protection from excessive power, internal short circuit protection which limits each circuit's maximum current, and output transistor safe area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be

TYPICAL APPLICATIONS μA79XX SERIES

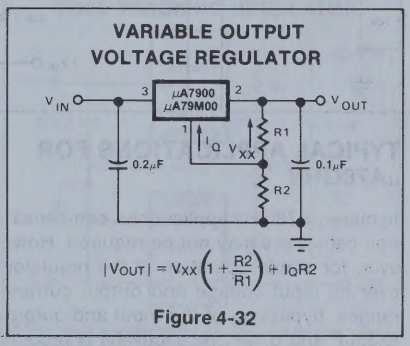


Figure 4-32

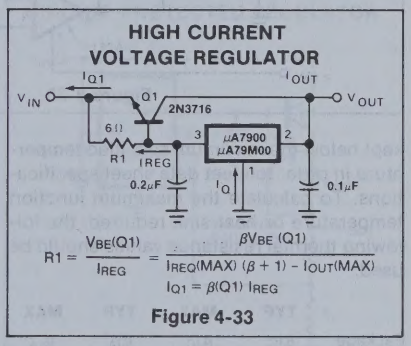


Figure 4-33

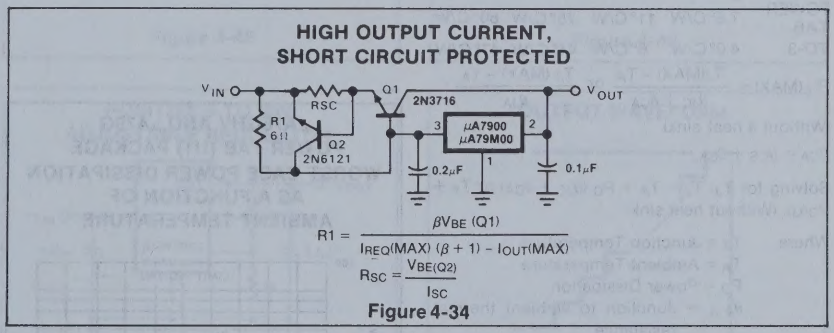


Figure 4-34

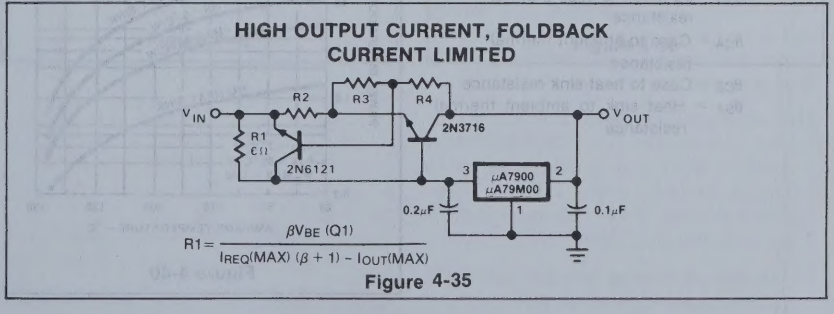


Figure 4-35

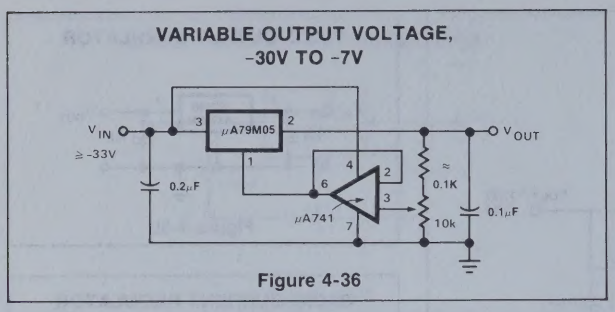


Figure 4-36

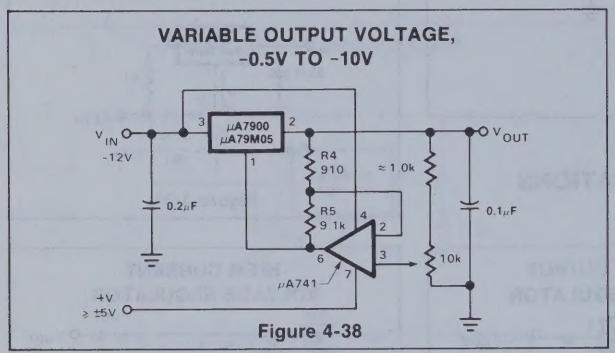


Figure 4-38

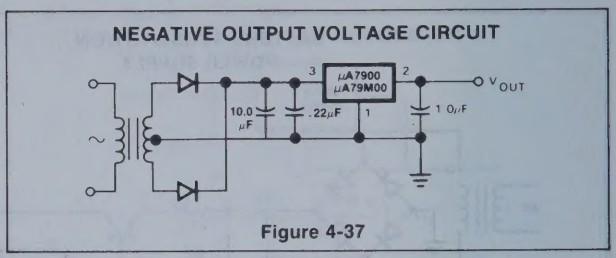


Figure 4-37

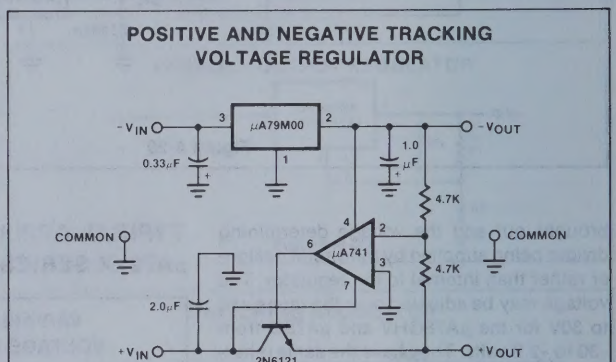


Figure 4-39

kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

	TYP	MAX	TYP	MAX
Package	θ_{JC}	θ_{JC}	θ_{JA}	θ_{JA}
POWER TAB	7.5°C/W	11°C/W	75°C/W	80°C/W
TO-3	4.0°C/W	6°C/W	44°C/W	47°C/W

$$P_D\,(MAX) = \frac{T_J(MAX) - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_J\,(MAX) - T_A}{\theta_{JA}}.$$

(Without a heat sink)

$\theta_{CA} = \theta_{CS} + \theta_{SA}$

Solving for T_J: $T_J = T_A + P_D\,(\theta_{JC} + \theta_{CA})$ or $T_A + P_D\theta_{JA}$ (Without heat sink)

Where
- T_J = Junction Temperature
- T_A = Ambient Temperature
- P_D = Power Dissipation
- θ_{J-A} = Junction to ambient thermal resistance
- θ_{JC} = Junction to case thermal resistance
- θ_{CA} = Case to ambient thermal resistance
- θ_{CS} = Case to heat sink resistance
- θ_{SA} = Heat sink to ambient thermal resistance

TYPICAL APPLICATIONS FOR μA78GHV

In many μA78GHV applications, compensation capacitors may not be required. However, for stable operation of the regulator over all input voltage and output current ranges, bypassing of the input and output (0.33μF and 0.1μF, respectively) is recommended. Input bypassing is necessary if the regulator is located far from the filter capacitor of the power supply. Bypassing the output will improve the transient response of the regulator.

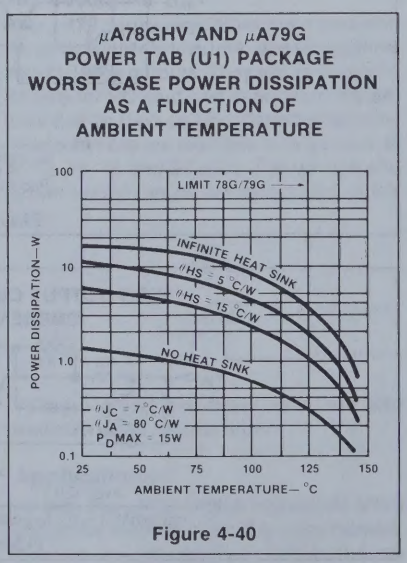


Figure 4-40

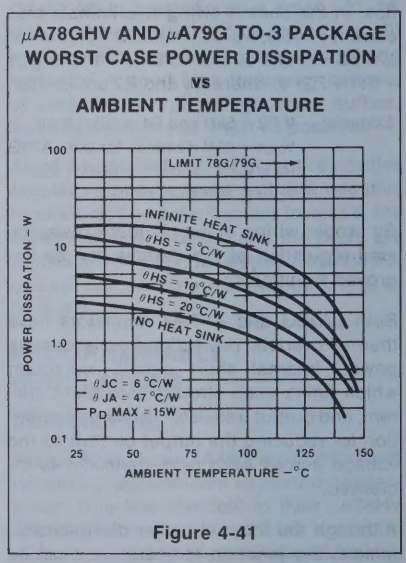
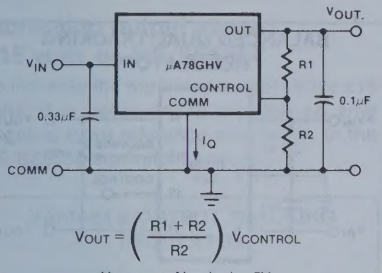


Figure 4-41

TEST LOAD CIRCUITS

μA78GHV TEST CIRCUIT 1



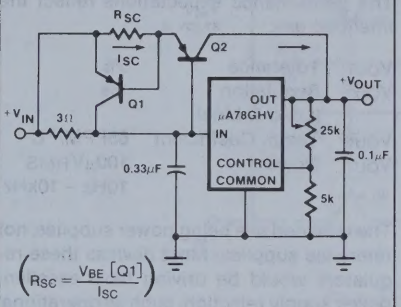
$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right) V_{CONTROL}$$

$V_{CONTROL}$ Nominal = 5V

Recommended R2 current ≈ 1mA
∴R2 = 5kΩ (78G)
R2 = 2.2kΩ (79G)

Figure 4-42

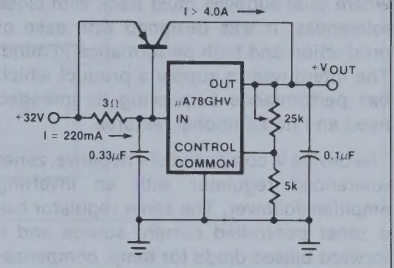
POSITIVE HIGH CURRENT SHORT CIRCUIT PROTECTED REGULATOR



$$\left(R_{SC} = \frac{V_{BE}\,[Q1]}{I_{SC}}\right)$$

Figure 4-45

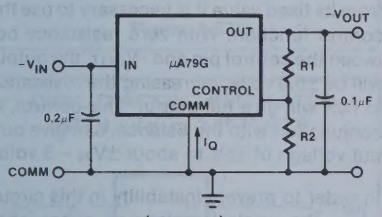
POSITIVE 5 TO 30V ADJUSTABLE REGULATOR $I_{OUT} > 5.0A$



NOTE: External series pass device is not short circuit protected.

Figure 4-48

μA79G TEST CIRCUIT 2



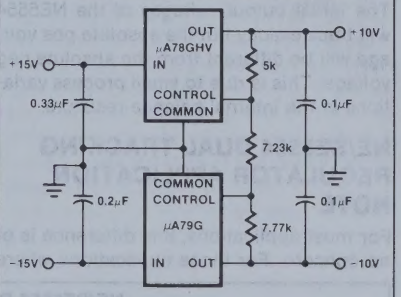
$$V_{OUT} = \left(\frac{R1 + R2}{R2}\right) V_{CONTROL}$$

$V_{CONTROL}$ Nominal = -2.23V

Recommended R2 current ≈ 1mA
∴R2 = 5kΩ (78G)
R2 = 2.2kΩ (79G)

Figure 4-43

± 10V, 1.0A DUAL TRACKING REGULATOR



If load is not ground referenced, connect reverse biased diodes from outputs to ground.

Figure 4-46

POSITIVE HIGH CURRENT SHORT CIRCUIT PROTECTED REGULATOR

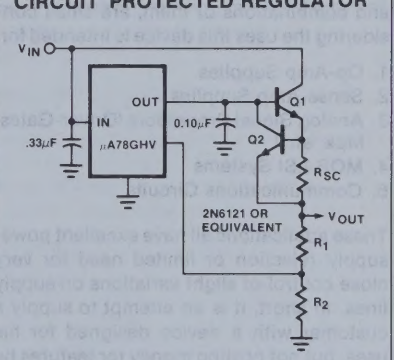
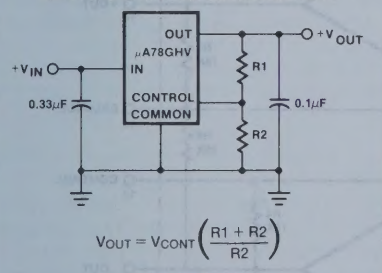


Figure 4-49

BASIC POSITIVE REGULATOR



$$V_{OUT} = V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

Figure 4-44

POSITIVE 5 TO 30V ADJUSTABLE REGULATOR

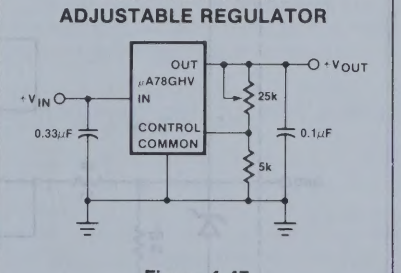


Figure 4-47

OUTPUT WAVEFORM

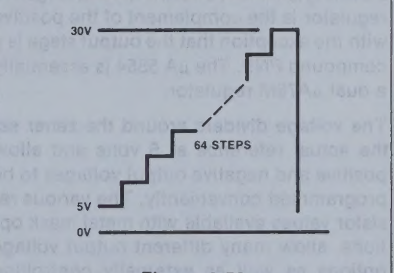


Figure 4-50

NE/SE5554 DUAL TRACKING REGULATOR

The Signetics NE/SE5554 is a monolithic dual tracking regulator designed for use where dual supplies must track with close tolerances. It was designed with ease of production and high performance in mind. The intent was to supply a product which has performance surpassing its intended need and no additional features.

The device is composed of a negative, zener referenced regulator with an inverting amplifier-follower. The zener regulator has a zener controlled current source and a forward biased diode for temp. compensation. This classical reference was used for one main reason . . . simplicity. The main justification to use this is the devices intended use. Considering 4 basic contributors to output voltage change, (1) Line regulation, (2) Load regulation, (3) Temperature Coefficient, (4) Popcorn noise, all of these, and combinations of them, are small considering the uses this device is intended for:

1. Op-Amp Supplies
2. Sense-Amp Supplies
3. Analog Signal Processors (Driver-Gates, Mpx, etc.)
4. MOS-LSI Systems
5. Communications Circuits

These applications all have excellent power supply rejection or limited need for very close control of slight variations on supply lines. In short, it is an attempt to supply a customer with a device designed for his uses, but not costing money for features he doesn't need.

Both actual regulators are differential amplifiers followed by a gain stage followed by a Darlington with current limit. The negative regulator is the complement of the positive with the exception that the output stage is a compound PNP. The μA 5554 is essentially a dual μA78M regulator.

The voltage dividers around the zener set the actual reference at 5 volts and allow positive and negative output voltages to be programmed conveniently. The various resistor values available with metal mask options, allow many different output voltage options as well as externally controlling output voltages by programming resistors to +Vout, -Vout, control and null.

The output current limit of 200mA was chosen as a compromise. The 100mA limit of the μA78LXX Family is only marginally useful for many systems, where 0.5 amp is too much dissipation for two regulators in a TO-5 package thus, the 200mA limit.

The regulators were designed to be on-chip compensated so external capacitors are not needed. This is a great advantage as most of the currently available devices require 10μf output capacitors or other cumbersome externally compensation.

The performance expectations reflect the intended use:

V_{OUT}	Tolerance	5%
V_{OUT}	Regulation (Load & Line)	1%
V_{OUT}	Temp. Coefficient	65PPM/°C
V_{OUT}	Noise	100μVRMS 10Hz - 10kHz

The intended use being power supplies, not reference supplies. Most devices these regulators would be driving have excellent power supply rejection, such as operational amplifiers, Analog switches, MOS logic, communication circuits, and will not be adversely affected by the output voltage tolerances, including noise and temperature coefficient.

The initial output voltages of the NE5554 will track exactly but the absolute pos voltage will be different from the absolute neg voltage. This is due to small process variations in the internal balance resistors.

NE/SE5554 DUAL TRACKING REGULATOR APPLICATION NOTE

For most applications, this difference is of no concern. For those applications where exact positive and negative voltages are necessary external balance potentiometer may be added as shown.

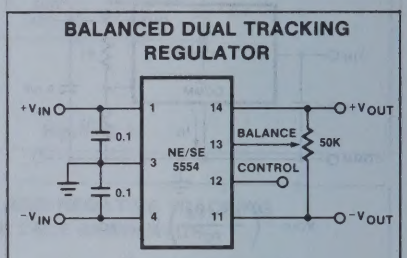


Figure 4-52

This output balance control may be used to change the positive regulated voltage from about 0.2 volts to ≥ 16 volts without changing the negative regulated voltage.

To change the negative regulator voltage from its fixed value it is necessary to use the control function. With zero resistance between the control pin and -V_{OUT}, the output will be ±5.0 volts. Increasing the resistance to 50K will give full output. This control, in conjunction with the balance, can give output voltage of ±5V to about ±V_{IN} - 3 volts.

In order to prevent instability in this circuit when the control resistance approaches zero ohms, it is necessary to use a filter capacitor on -V_{OUT} of 0.1μf or larger to

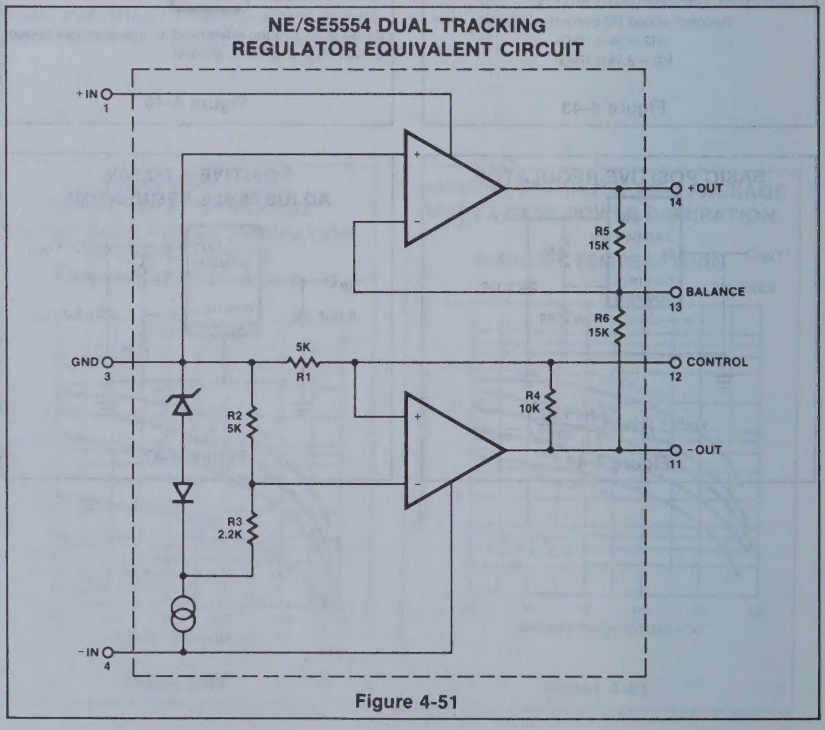


Figure 4-51

ground. A 10μf from $+V_{OUT}$ and $-V_{OUT}$ to ground will improve transient response, where this is of concern.

Increasing output above ±15 volts on NE/SE5554

To increase the regulated output above ±15 volts, it is necessary to trim the op amp negative input reference resistor (R_1 in the NE/SE5554 equivalent circuit).

VARIABLE OUTPUT TRACKING REGULATOR

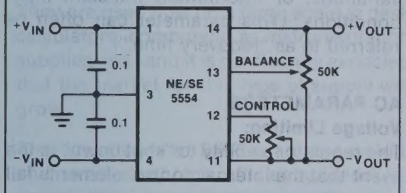


Figure 4-53

DUAL TRACKING REGULATOR WITH $\pm V_{OUT}$ > 15 VOLTS

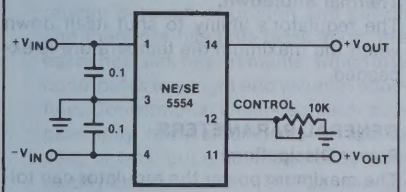
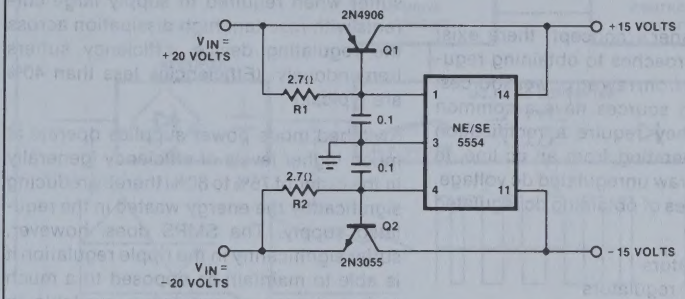


Figure 4-54

HIGH CURRENT DUAL TRACKING REGULATOR



$$\beta(Q) \geq \frac{I_{OUT(MAX)}}{I_{REQ(MAX)}}$$

$$R1 = R2 = \frac{\beta V_{BE}}{I_{REG(MAX)}\,(\beta + 1) - I_{OUT(MAX)}}$$

Figure 4-55

SWITCHED MODE POWER SUPPLY

Introduction

From the designer's concept, there exist three basic approaches to obtaining regulated dc votages from raw ac power sources. The three basic sources have a common denominator; they require a rectification media when operating from an ac line, in order to obtain raw unregulated dc voltage. The three sources of obtaining dc regulated voltages are:

- Shunt regulators
- Series linear regulators
- Series switched mode regulators

(The series switched mode regulators will be referred to as switched mode power supplies (or SMPS) during the course of this article.)

Briefly stated, if all three types of regulation can perform the same function, following are some of the key parameters to be addressed:

- From an economical point of view, cost of the system is paramount.
- From an operations point of view, weight of the system is critical.
- From a design criteria, system efficiency is the first order of business.

The series and shunt regulators operate on the same principle of sensing the DC output voltage, comparing to an internal reference level and varying a resistor (active device) to maintain the output levels within prespecified limits.

Switched mode power supplies (SMPS) are basically DC to DC converters, operating at frequencies in the 20kHz and higher region. Basically the SMPS is a power source which utilizes the energy stored during one portion of its operating cycle to supply power during the remaining segment of its operating cycle.

Linear regulators, both shunt and series, suffer when required to supply large currents with resultant high dissipation across the regulating device. Efficiency suffers tremendously. (Efficiencies less than 40% are typical.)

Switched mode power supplies operate at much higher levels of efficiency (generally in the order of 75% to 80%) thereby reducing significantly the energy wasted in the regulated supply. The SMPS does, however, suffer significantly in the ripple regulation it is able to maintain as opposed to a much higher degree of regulation available in series (or shunt) linear regulators.

The linear regulators obtain improved regulation by virtue of the series pass elements always conducting, as opposed to SMPS devices having their active devices operative only during a portion of the overall operating period.

This section is designed primarily to introduce the Signetics NE5560 Switched Mode Power Supply and its features; however, before discussing this particular device, NE5560, the author feels that some definitions and comparisons between linear regulators and switched mode power supplies should be stated.

REGULATION

Line Regulation:
(Sometimes referred to as static regulation) refers to the changes in the output (as a percent of nominal or actual value) as the input AC is varied slowly from its rated minimum value to its rated maximum value (i.e., from $105VAC_{RMS}$ to $125VAC_{RMS}$).

Load Regulation:
(Sometimes referred to as dynamic regulation) refers to the changes in the output (as a percent of nominal or actual value) when the load conditions are suddenly changed (i. e., no load to full load.)

NOTE
The combination of static and dynamic regulation are cumulative; care should be taken when referring to the regulation characteristics of a power supply.

Thermal Regulation:
Referred to as changes due to ambient variations or thermal drift.

TRANSIENT RESPONSE

The ability of the regulator to respond to rapid changes in either line variations, load variations, or intermittent transient input conditions. (This parameter can often be referred to as "recovery time.")

AC PARAMETERS

Voltage Limiting:
The regulator's ability to "shut down" in the event that the internal control elements fail to function properly.

Current Limiting:
Often referred to as "fold-back" where the amplifier segment of the regulator folds back the output current of the device when safe operating limits are exceeded.

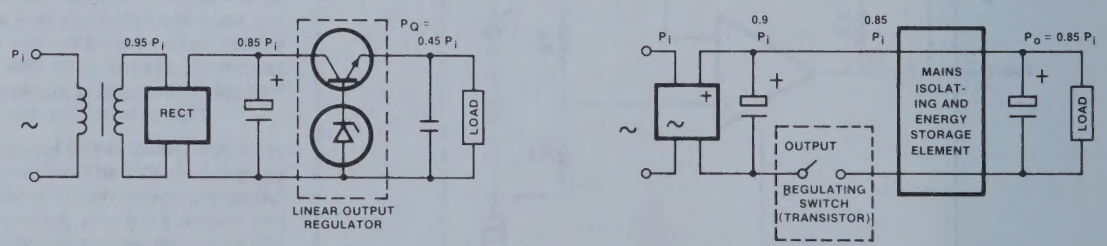
Thermal Shutdown:
The regulator's ability to shut itself down when the maximum die temperature is exceeded.

GENERAL PARAMETERS

Power Dissipation:
The maximum power the regulator can tolerate and still maintain its operation within the safe operating area of its active devices.

Efficiency:
The ratio (in percent) of the usable versus total power being dissipated in a regulated supply. (The losses can be ac as well as dc losses.)

LOSSES IN REGULATED POWER SUPPLIES



(a) CONVENTIONAL SUPPLY - 45% EFFICIENCY

(b) SWITCHED-MODE SUPPLY - 80% EFFICIENCY

Figure 4-56

EMI/RFI:
Generation of radio frequency interference signals and magnetic field disturbance especially in SMPS devices. (Transformer and choke design available which reduced both RFI & EMI to safe acceptable regions.)

The balance of this section will be dedicated to the discussion of the general operation of Switched Mode Power Supplies (SMPS) with emphasis on the Signetics NE5560 Control and Protection Module.

Switched-mode power supplies (SMPSs) have gained much popularity in recent years because of the benefits they offer. They are used now on a large scale in desk calculators, computers, as instrumentation supplies, etc., and it is confidently expected that the market for this type of supply will grow.

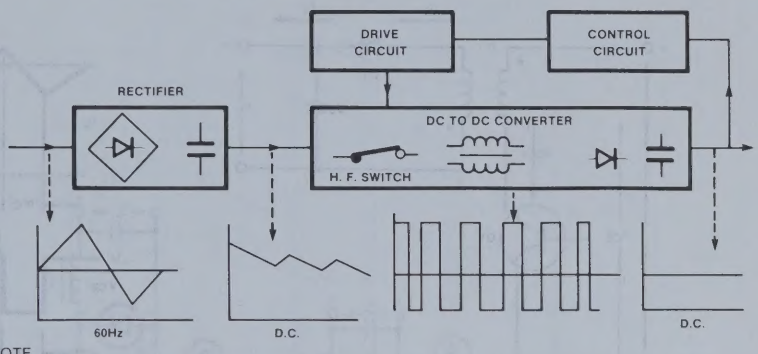
The advantages of SMPSs are low weight and small size, high efficiency, wide AC input voltage range, and low cost.

- Low weight and small size are possible because operation occurs at a frequency beyond the audible range; the inductive elements are small.
- High efficiency because, for output regulation, the power transistor is switched rapidly between saturation and cut-off and therefore has little dissipation; this eases heatsink requirements, which also contributes to weight and volume reduction. Conventional linear-regulator supplies may have efficiencies as low as 50%, or less, but efficiencies of 80% are readily achievable with SMPSs; see figure 4-56.
- Wide AC input voltage range because of the flexibility of varying the switching frequency in addition to the change in transistor duty cycle makes voltage adaptation unnecessary.
- Low overall cost, due to the reduced volume and dissipation, means that less material is required and smaller semiconductor devices suffice.

Switched-mode power supplies also have slight disadvantages in comparison with linear regulators, namely, somewhat greater circuit complexity, tendency to r.f.i. radiation, slower response to rapid load changes, and less ability to remove output ripple.

HOW SWITCHED-MODE POWER SUPPLIES OPERATE

The switched-mode power supply is a modern version of its forerunner, the electromechanical vibrator, used in the past to supply car radios. But the new concept is much more reliable because of the far greater lifetime of the transistor switch. Figure 4-57 shows the principle of the ac fed SMPS. In this system the ac voltage is rectified, smoothed, and supplied to the electronic chopper, which operates at a frequency above the audible range to prevent noise. The chopped dc voltage is applied to the primary of a transformer, and the secondary voltage is rectified and smoothed to give the required dc output. The transformer is necessary to isolate the output from the input. Output voltage is sensed by a control circuit, which adjusts the duty cycle of the switching transistor, via the drive circuit, to keep the output voltage constant irrespective of load and line voltage changes. Without the input rectifier, this system can operate from a battery of other dc source.



NOTE
Switching frequency is between 20kHz and 50kHz.

Figure 4-57

Depending on the requirements of the application, the dc-to-dc converter can be one of the three basic types: flyback converter, forward converter, or push-pull (balanced) converter.

The Flyback Converter

Figure 4-58 shows the flyback converter circuit, and the waveforms of transistor voltage, V_{CE}, and choke current, i_L, reflected to the primary (choke double-wound for line isolation). Cycle time and transistor duty cycle are denoted T and δ, respectively. While Q1 conducts, energy is accumulated in the choke magnetic field (i_L rising and D_1 reversed biased), and it is discharged into the output capacitor and the load during the flyback period, that is, while Q1 is off (i_L falling and D_1 forward biased). During Q1 conduction, C_o continues delivering energy to the load so providing smoothing action. It will be noted that only one inductive element is needed, in distinction to the converter types discussed below, which require two. As the V_{CE} waveform shows, the peak collector voltage is twice the input voltage, V_i, for δ equal to 0.5.

The Forward Converter

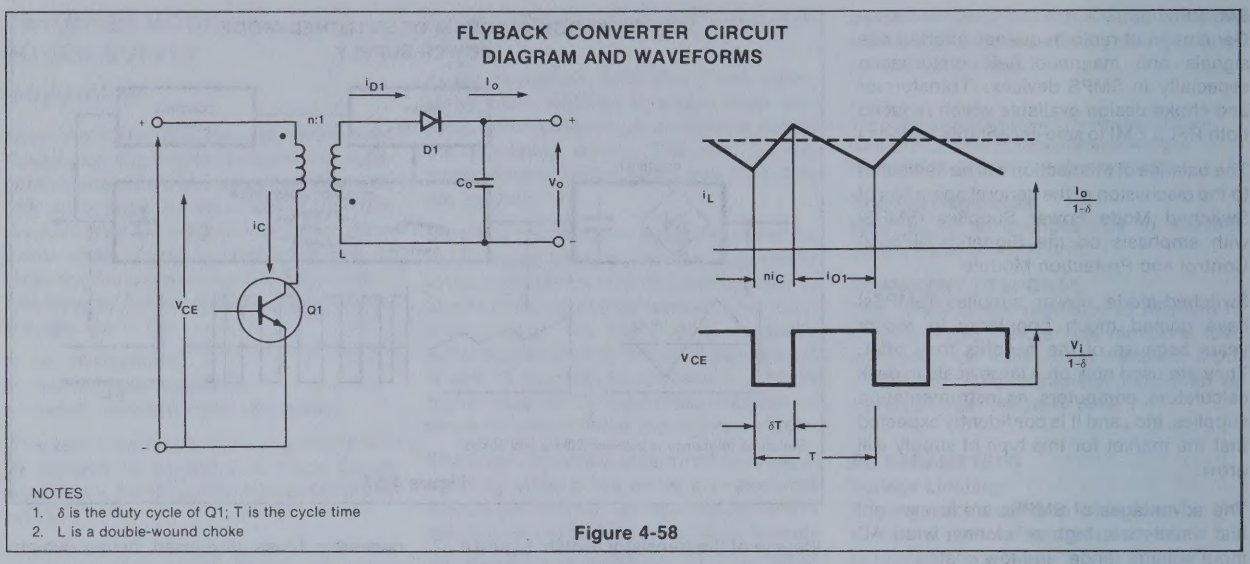
A major advantage of the forward converter, particularly for low output voltage applications, is that the high-frequency output ripple is limited by the choke in series with the output. Figure 4-59 illustrates the circuit. During the transistor-on (or forward) period, energy is simultaneously stored in the choke L_O and passed via D_1 to the load. While Q1 is off, part of the energy accumulated in L_O is transferred to the load through free-wheeling diode D_2. Output capacitor C_O smoothes the ripple due to transistor switching. After transistor turn-off, the magnetic energy built up in the transformer core is returned to the dc input via the demagnetizing winding (closely coupled with the primary) and D_3, so limiting the peak collector voltage to twice the input voltage V_i.

The Push-Pull Converter

This converter type, given in Figure 4-60, consists of two forward converters operating in push-pull. Diodes D_1 and D_2 rectify the rectangular secondary voltage generated by Q1 and Q2 being turned on during alternate half cycles. Push-pull operation doubles the frequency of the ripple current in output filter L_oC_o and so reduces the output ripple voltage. The peak transistor voltage is $2V_i$.

MAKING THE BEST CONVERTER CHOICE

There exist several versions of the three fundamental circuits described earlier.



NOTES
1. δ is the duty cycle of Q1; T is the cycle time
2. L is a double-wound choke

Figure 4-58

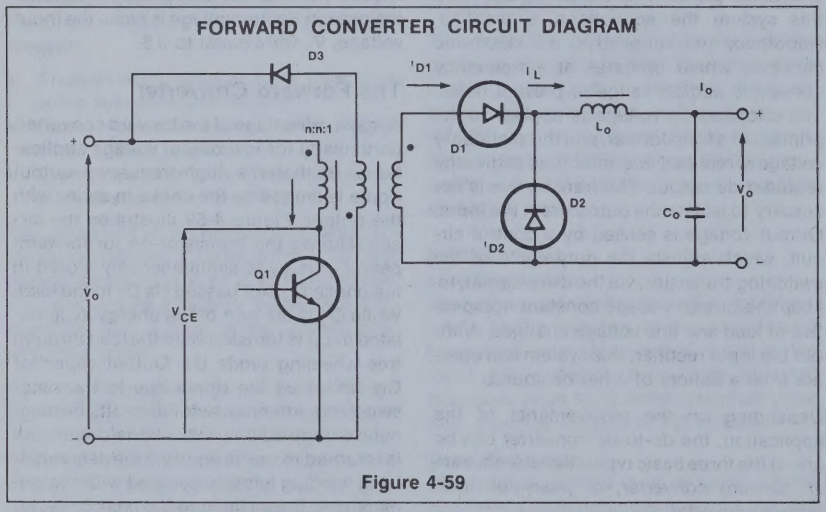


Figure 4-59

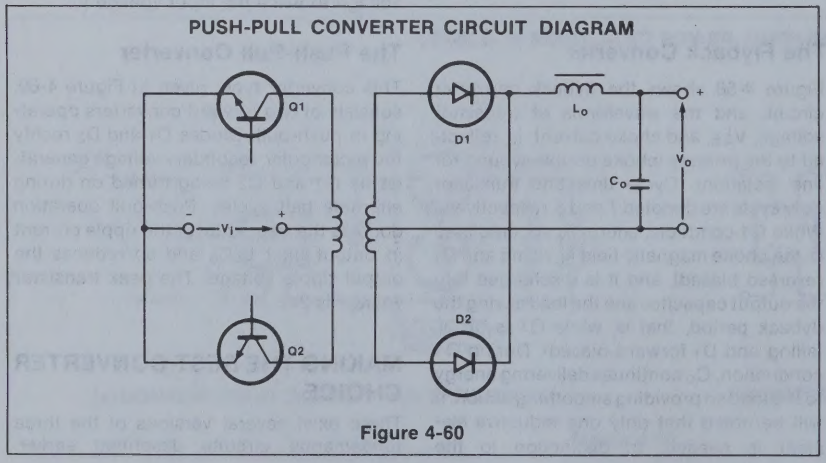


Figure 4-60

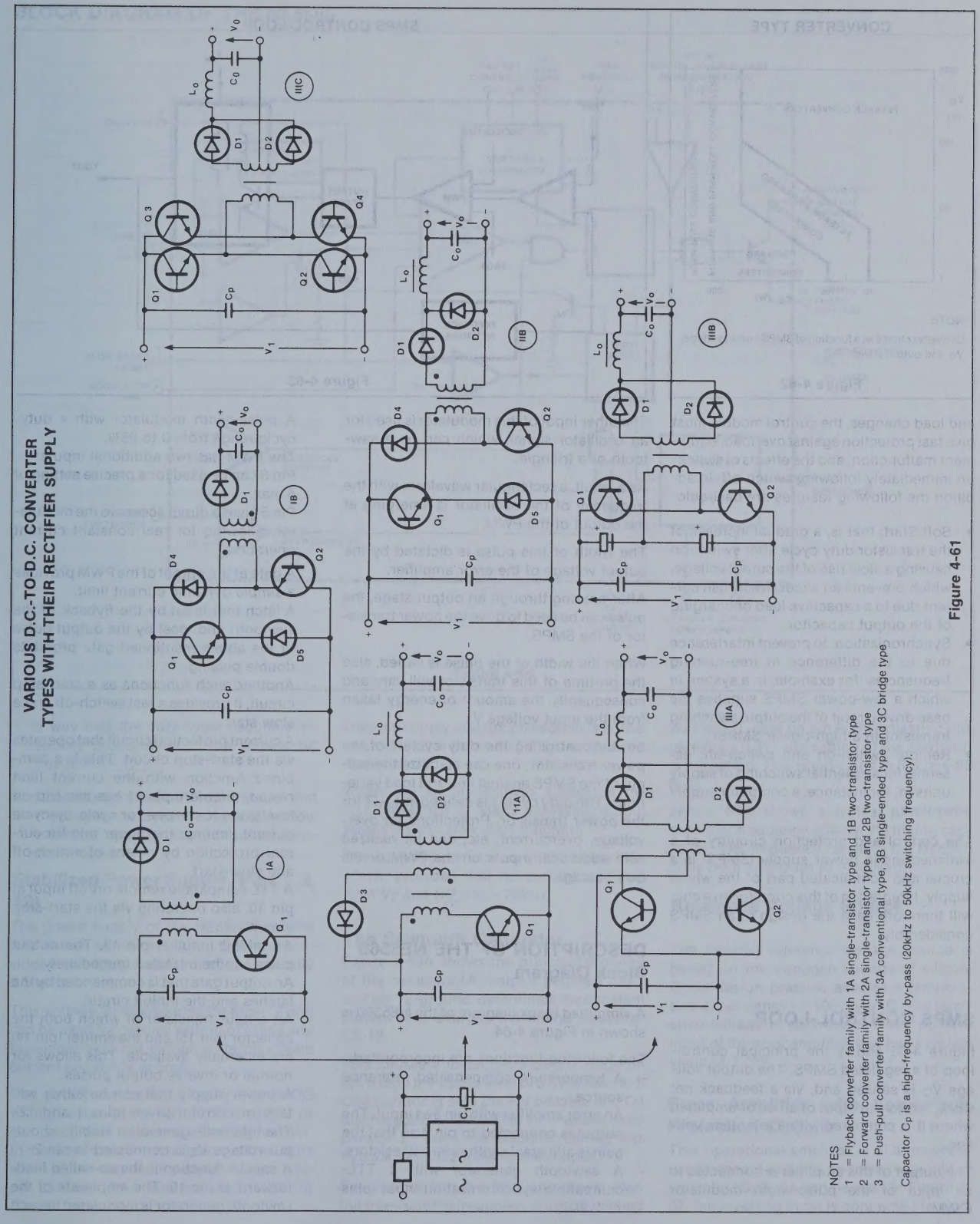
These are shown in Figure 4-61. Circuits IA, IIA and IIIA are the basic types. In the two-transistor circuits, IB and IIB, transistors Q1 and Q2 conduct simultaneously and diodes D_4 D_5 limit the peak collector voltage to the level of DC input voltage V_i. Similarly in the push-pull circuits IIIB and IIIC, the collector voltage does not exceed V_i. In circuit IIIB, Q1 and Q2 are turned on during alternate half cycles; in circuit IIIC, Q1 and Q4 are turned on in one half cycle and Q2 Q3 in the next.

Converter choice depends on application and performance requirements. The flyback converter is the simplest and least expensive; it is recommended for multi-output supplies because each output requires only one diode and one capacitor. However, smoothing may be a problem where ripple requirements are severe. The push-pull type has the most complex base drive circuit but it produces the lowest output ripple with given values of L_o and C_o.

Figure 4-62 is a general guide for the choice of converter type, based on output voltage and power. In the case of the flyback converter, it becomes more and more difficult to keep the percentage output ripple below an acceptable level as the output power increases and the output voltage decreases; for reasons of circuit economy, however, the flyback converter is the best proposition if the output power does not exceed about 10W. For output powers higher than about 1kW, the push-pull converter is preferable.

THE CONTROL AND PROTECTION MODULE

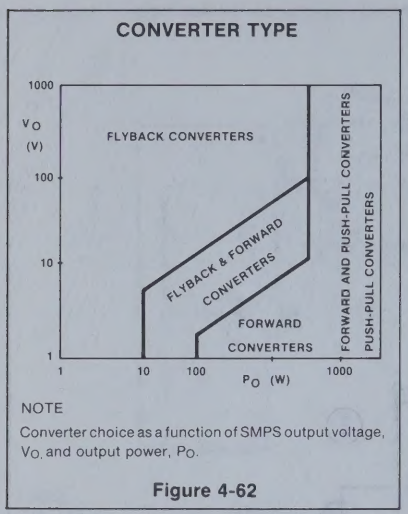
In addition to providing adequate output voltage stabilization against line voltage



NOTES
1 = Flyback converter family with 1A single-transistor type and 1B two-transistor type
2 = Forward converter family with 2A single-transistor type and 2B two-transistor type
3 = Push-pull converter family with 3A conventional type, 3B single-ended type and 3C bridge type

Capacitor C_P is a high-frequency by-pass (20kHz to 50kHz switching frequency).

Figure 4-61



NOTE
Converter choice as a function of SMPS output voltage, V_O, and output power, P_O.

Figure 4-62

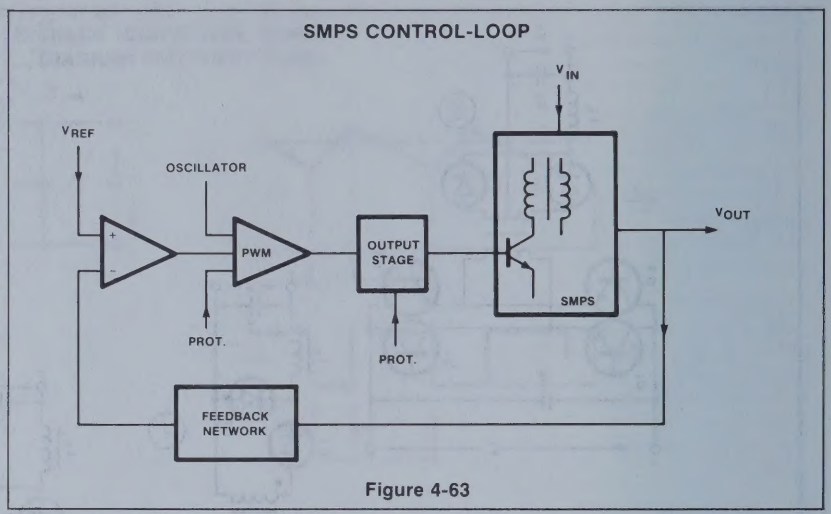


Figure 4-63

and load changes, the control module must give fast protection against overload, equipment malfunction, and the effects of switch-on immediately following switch-off. In addition the following features are desirable:

- Soft Start: that is, a gradual increase of the transistor duty cycle after switch-on causing a slow rise of the output voltage, which prevents an excessive inrush current due to a capacitive load or charging of the output capacitor.
- Synchronization: to prevent interference due to the difference in free-running frequencies (for example, in a system in which a low-power SMPS supplies the base drive circuit of the output switching transistor in a high-power SMPS).
- Remote switch-on and switch-off: essential for sequential switching of supply units in, for instance, a computer supply system.

The control and protection circuitry of a switched-mode power supply (SMPS) is a crucial and complicated part of the whole supply. Integration of this circuitry on a chip will therefore ease the design of an SMPS considerably.

SMPS CONTROL-LOOP

Figure 4-63 shows the principal control-loop of a regulated SMPS. The output voltage V_O is sensed and, via a feedback net work, fed to the input of an error amplifier, where it is compared with a reference voltage.

The output of this amplifier is connected to an input of the pulse-width modulator (PWM).

The other input of this modulator is used for an oscillator signal, which can be a sawtooth or a triangle.

As a result, a rectangular waveform with the frequency of the oscillator is emerging at the output of the PWM.

The width of this pulse is dictated by the output voltage of the error amplifier.

After passing through an output stage, the pulse can be used to drive the power transistor of the SMPS.

When the width of the pulse is varied, also the on-time of this transistor will vary and consequently the amount of energy taken from the input voltage V_i.

So, by controlling the duty cycle δ of the power transistor, one can stabilize the output of the SMPS against line and load variations. The duty cycle δ is defined as t_{on}/T for the power transistor. Protections for overvoltage, overcurrent, etc, can be realized with additional inputs on the PWM or the output stage.

DESCRIPTION OF THE NE5560

Block Diagram

A simplified block diagram of the NE5560 is shown in Figure 4-64.

The following functions are incorporated:

- A temperature compensated reference source.
- An error amplifier with pin 3 as input. The output is connected to pin 4 so that the gain is adjustable with external resistors.
- A sawtooth generator with a TTL-compatible synchronization input (pins 7, 8, 9).
- A pulse-width modulator with a duty-cycle range from 0 to 95%.
  The PWM has two additional inputs:
  Pin 6 can be used for a precise setting of δ max.
  Pin 5 gives a direct access to the modulator, allowing for real constant current operation.
- A gate at the output of the PWM provides a simple dynamic current limit.
- A latch that is set by the flyback of the sawtooth and reset by the output pulse of the above mentioned gate prohibits double pulsing.
- Another latch functions as a start-stop circuit; it provides a fast switch-off and a slow start.
- A current protection circuit that operates via the start-stop circuit. This is a combined function with the current limit circuit, therefore pin 11 has two trip-on levels; the lower one for cycle-by-cycle current limiting, the upper one for current protection by means of switch-off and slow-start.
- A TTL compatible remote on/off input at pin 10, also operating via the start-stop circuit.
- An inhibit input at pin 13. The output pulse can be inhibited immediately.
- An output gate that is commanded by the latches and the inhibit circuit.
- An output transistor of which both the collector (pin 15) and the emitter (pin 14) are externally available. This allows for normal or inverse output pulses.
- A power supply that can be either voltage or current driven (pins 1 and 12). The internally generated stabilized output voltage V_Z is connected to pin 2.
- A special function is the so-called feed-forward at pin 16. The amplitude of the sawtooth generator is modulated in such

BLOCK DIAGRAM OF THE NE5560

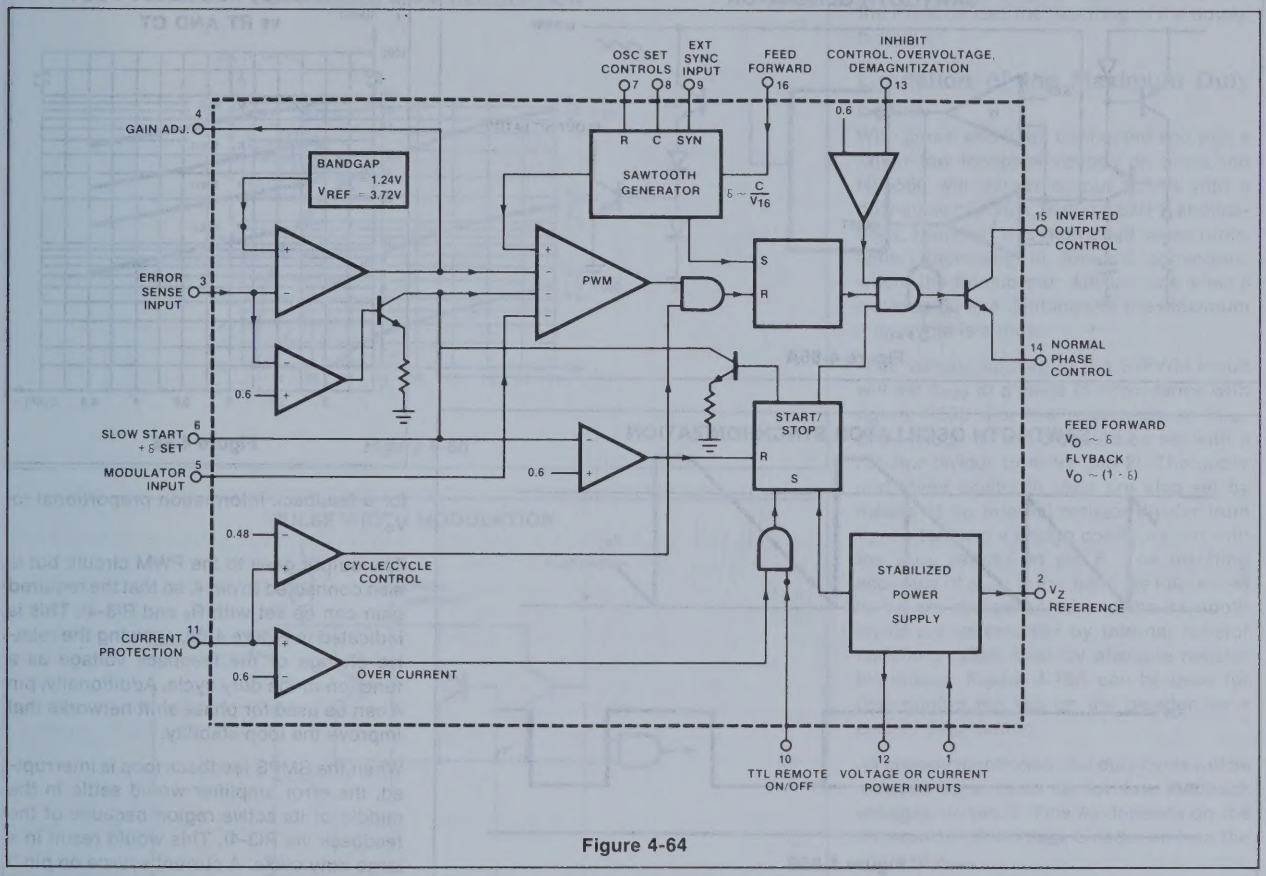


Figure 4-64

a way that the duty cycle becomes inversely proportional to the voltage on this pin: $\delta \sim \frac{C}{V16}$.

- Loop fault protection circuits assure that the duty-cycle is reduced to zero or a low value for open or short-circuited feedback loops.

Stabilized Power Supply (Pins 1, 2, 12)

The power supply of the NE5560 is of the well known series regulation type and provides a stabilized output voltage of typically 8.5 volts.

This voltage V_Z is also present at pin 2 and can be used for precise setting of δ max and to supply external circuitry. Its maximum current capability is 5mA.

The circuit can be fed directly from a DC voltage source between 10.5V and 18V or can be current driven via a limiting resistor. In the latter case, internal pinch-off resistors will limit the maximum supply voltage; typical 23V for 10mA and maximum 30V for 30mA.

The low supply voltage protection is active when V(1-12) is below 10.5V and inhibits the output pulse.

When the supply voltage surpasses the 10.5V level the IC starts delivering output pulses via the slow start function.

The current consumption at 12V is less than 10mA, provided that no current is drawn from V_Z and R(7-12) ≥ 20k Ω.

The Sawtooth Generator

Figure 4-65A shows the principal circuitry of the oscillator. A resistor between pin 7 and pin 12 (ground) determines the constant current that charges the timing capacitor C8-12.

This causes a linear increasing voltage on pin 8 until the upper level of 5.6V is reached. Comparator H sets the RS bistable and Q1 discharges C8-12 down to 1.1V, where comparator L resets the bistable. During this flyback time, Q2 inhibits the output.

Synchronization at a frequency lower than the free-running frequency is accomplished via the TTL gate on pin 9. By activating this gate (V_9 < 0.8V), the setting of the sawtooth is prevented. This is indicated in figure 4-65 B.

Figure 4-66 shows a typical plot of the oscillator frequency against the timing capacitor. The frequency range of the NE5560 goes from <50Hz up to > 100kHz.

Reference Voltage Source

The internal reference voltage source is based on the bandgap voltage of silicon. Good design practice assures a temperature dependency < ±100 ppm/°C. The reference voltage is connected to the positive input of the error amplifier and has a typical value of 3.72V.

Error Amplifier with Loop-Fault Protection Circuits

This operational amplifier is of a generally used concept and has an open loop gain of typically 60dB. As can be seen in Figure 4-67, the inverting input is connected to pin 3

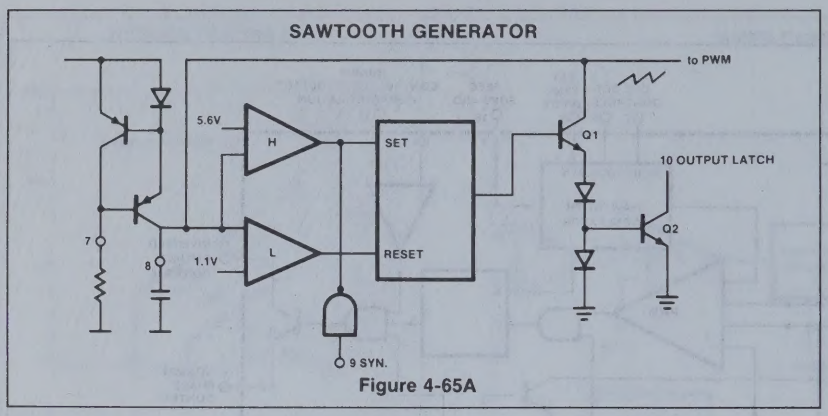


Figure 4-65A

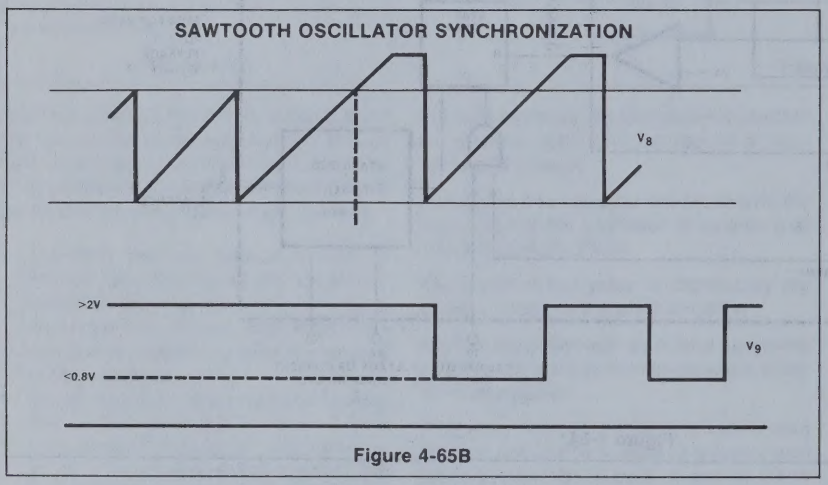


Figure 4-65B

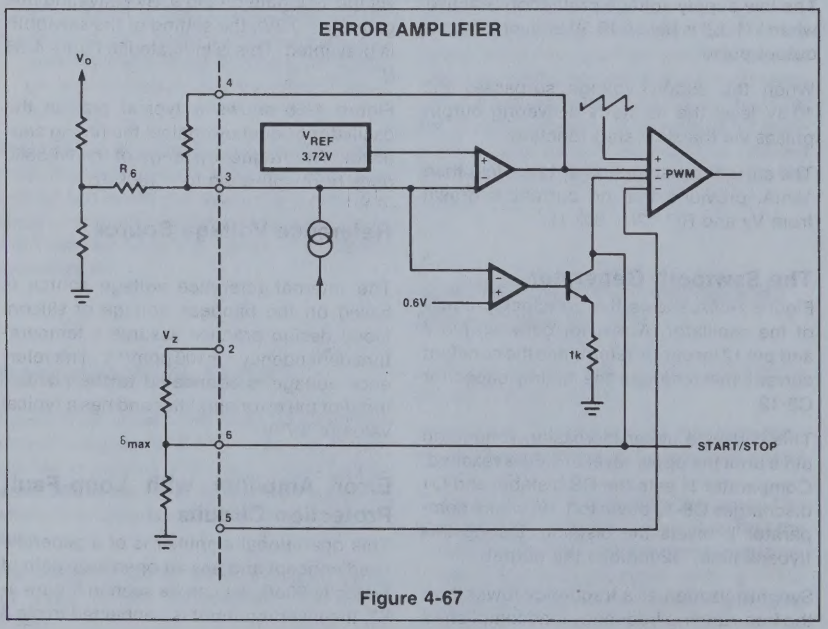


Figure 4-67

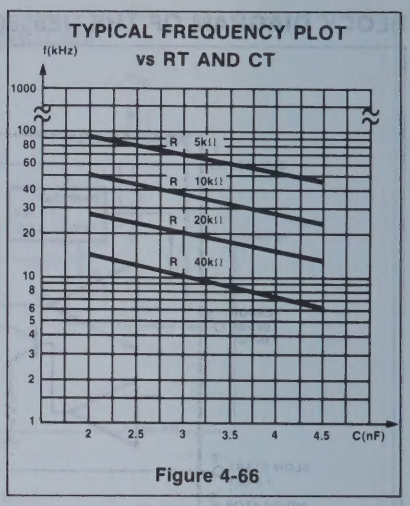


Figure 4-66

for a feedback information proportional to V_O.

The output goes to the PWM circuit, but is also connected to pin 4, so that the required gain can be set with R_S and R(3-4). This is indicated in Figure 4-68, showing the relative change of the feedback voltage as a function of the duty cycle. Additionally, pin 4 can be used for phase shift networks that improve the loop stability.

When the SMPS feedback loop is interrupted, the error amplifier would settle in the middle of its active region because of the feedback via R(3-4). This would result in a large duty cycle. A current source on pin 3 prevents this by pushing the input voltage high via the voltage drop over R(3-4). As a result, the duty cycle will become zero, provided that R(3-4) > 100k. When the feedback loop is shortcircuited, the duty cycle would jump to the adjusted maximum duty cycle. Therefore, an additional comparator is active for feedback voltages at pin 3 below 0.6V.

Now an internal resistor of typically 1k is shunted to the impedance on the δ_{max}-setting pin 6. Depending on this impedance, δ will be reduced to a value δo. This will be discussed further.

The Pulse-Width Modulator

The function of the PWM circuit is to translate a feedback voltage into a periodical pulse of which the duty cycle depends on that feedback voltage. As can be seen in Figure 4-69A, the PWM circuit in the NE5560 is a long-tailed pair in which the sawtooth on pin 8 is compared with the LOWEST voltage on either pin 4 (error amplifier), pin 5, or pin 6 (δ_{max} and slow-start). The transfer

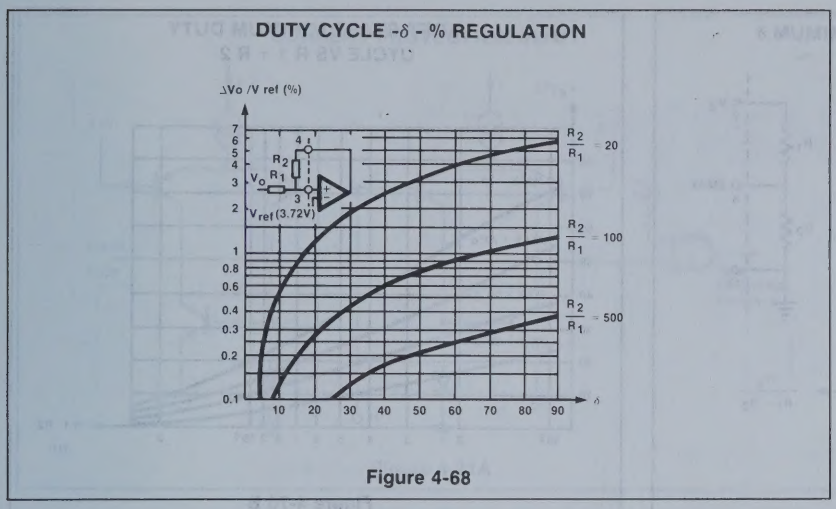


Figure 4-68

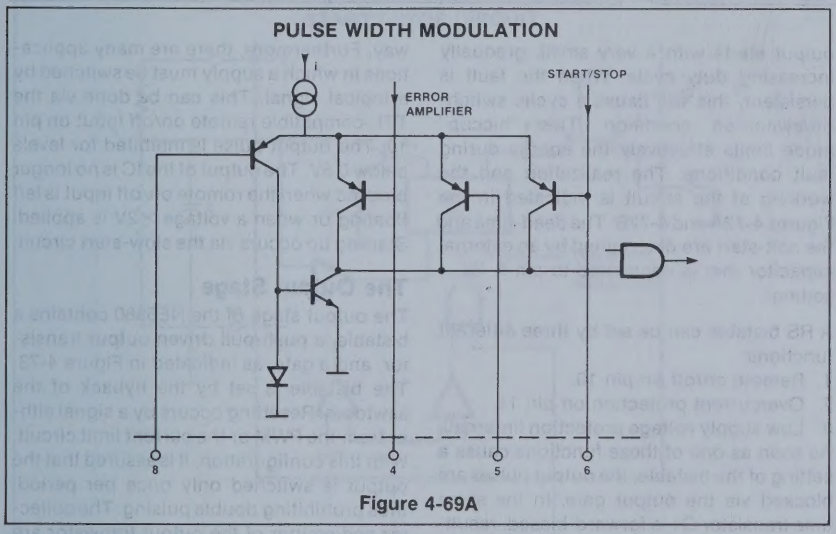


Figure 4-69A

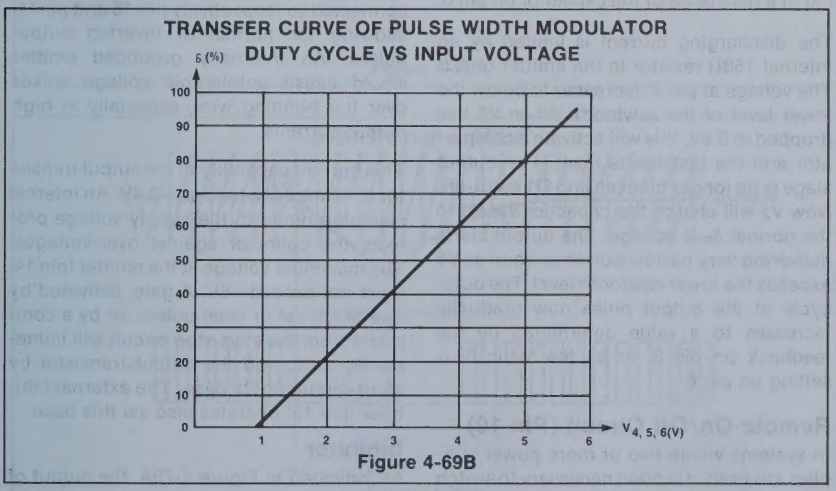


Figure 4-69B

graph is given in Figure 4-69B. The output of the PWM causes the resetting of the output bistable.

Limitation of the Maximum Duty Cycle

With pins 5 and 6 not connected and with a rather low feedback voltage on pin 3, the NE5560 will deliver output pulses with a duty cycle of ≈ 95%. In many SMPS applications, however, this high δ will cause problems. Especially in forward converters, where the transformer will saturate when δ exceeds 50%, a limitation of the maximum duty-cycle is a must.

A dc voltage applied to pin 6 (PWM input) will set δ_{max} at a value in accordance with figure 4-69B. For low tolerances on δ_{max}, this voltage on pin 6 should be set with a resistor divider from V_Z (pin 2). The upper and lower sawtooth level are also set by means of an internal resistor divider from V_Z, so forming a bridge configuration with the δ_{max} setting on pin 6. The resulting accuracy of δ_{max} is low because tolerances in V_Z are compensated and the sawtooth levels are determined by internal resistor matching rather than by absolute resistor tolerances. Figure 4-70A can be used for determining the tap on the bleeder for a certain δ_{max} setting.

As already mentioned, the duty cycle will be reduced to a value δ_o for low feedback voltages on pin 3. This δo depends on the impedance of the δ_{max} bleeder and on the value of δ_{max}.

Figure 4-70B gives a graphical representation of this. The value δo is limited to the lower and the higher side;

- It must be large enough to ensure that at maximum load and minimum input voltage the resulting feedback voltage on pin 3 exceeds 0.6V.
- It must be small enough to limit the amount of energy in the SMPS when a loop-fault occurs. In practice a value of 10-15% will be a good compromise.

Extra PWM Input (Pin 5)

The PWM has an additional inverting input: pin 5. It allows for attacking the duty cycle via the PWM circuit, independently from the feedback and the δ_{max} information. This is necessary when the SMPS must have a real constant current behavior, possibly with a fold-back characteristic. However, the realization of this feature must be done with additional external components.

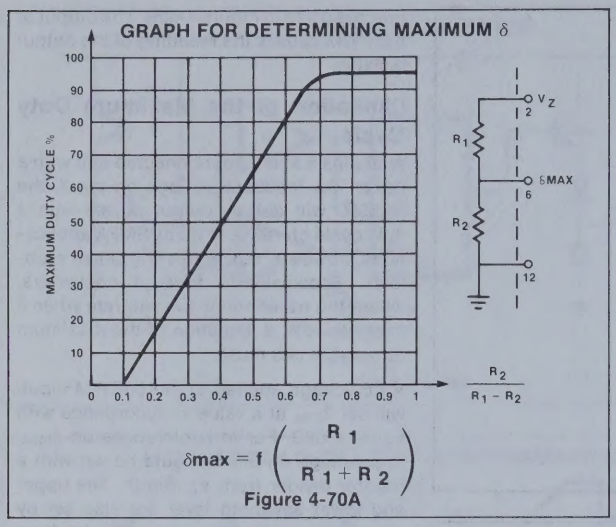


Figure 4-70A

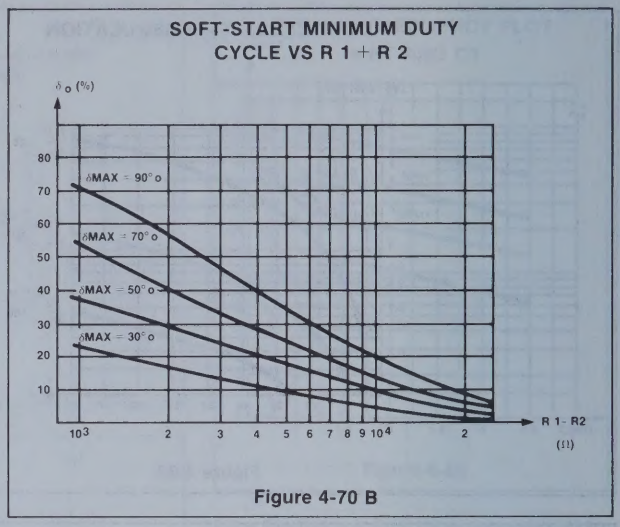


Figure 4-70 B

Dynamic Current Limit and Current Protection (Pin II)

In many applications, it is not necessary to have a real constant current output of the SMPS.

Protection of the power transistor will be the prime goal. This can be realized with the NE5560 in a simple and cheap way. A resistor (or a current transformer) in the emitter of the power transistor gives a replica of the collector current. This signal must be connected to pin 11. As can be seen in Figure 4-71A, this input has two comparators with different reference levels. The output of the comparator with the lower 0.48V reference is connected to the same gate as the output of the PWM.

When activated, it will immediately reset the output bistable, so reducing the duty cycle. The effectiveness of this so-called cycle-by-cycle current limit diminishes at low duty cycle values. When δ becomes very small, the storage time of the power transistor becomes dominant. The current will now increase again, until it surpasses the reference of the second comparator. The output of this comparator acitvates the start/stop circuit and causes an immediate inhibit of the output pulses. After a certain dead-time the circuit starts again with very narrow output pulses. The effect of this two-level current protection circuit is visualized in Figure 4-71B.

The Start/Stop Circuit

The function of this protection circuit is to stop the output pulses as soon as a fault occurs and to keep the output stopped for several periods. After this dead time, the output starts with a very small, gradually increasing duty cycle. When the fault is persistent, this will cause a cyclic switch-off/switch-on condition. This "hiccup" mode limits effectively the energy during fault conditions. The realization and the working of the circuit is indicated in the Figures 4-72A and 4-72B. The dead-time and the soft-start are determined by an external capacitor that is connected to pin 6. (δ_{max} setting).

A RS bistable can be set by three different functions:

1. Remote on/off on pin 10.
2. Overcurrent protection on pin 11.
3. Low supply voltage protection (internal).

As soon as one of these functions cause a setting of the bistable, the output pulses are blocked via the output gate. In the same time transistor Q1 is forward-biased, resulting in a discharge of the capacitor on pin 6.

The discharging current is limited by an internal 150Ω resistor in the emitter of Q1. The voltage at pin 6 decreases to below the lower level of the sawtooth. When V6 has dropped to 0.6V, this will activate a comparator and the bistable is reset. The output stage is no longer blocked and Q1 is cut-off. Now V_Z will charge the capacitor via R1 to the normal δ_{max} voltage. The output starts delivering very narrow pulses as soon as V6 exceeds the lower sawtooth level. The duty-cycle of the output pulse now gradually increases to a value determined by the feedback on pin 3, or by the static δ_{max} setting on pin 6.

Remote On/Off Circuit (Pin 10)

In systems where two or more power supplies are used, it is often necessary to switch these supplies on and off in a sequential way. Furthermore, there are many applications in which a supply must be switched by a logical signal. This can be done via the TTL-compatible remote on/off input on pin 10. The output pulse is inhibited for levels below 0.8V. The output of the IC is no longer blocked when the romote on/off input is left floating or when a voltage > 2V is applied. Starting up occurs via the slow-start circuit.

The Output Stage

The output stage of the NE5560 contains a bistable, a push-pull driven output transistor, and a gate, as indicated in Figure 4-73. The bistable is set by the flyback of the sawtooth. Resetting occurs by a signal either from the PWM or the current limit circuit. With this configuration, it is assured that the output is switched only once per period, thus prohibiting double pulsing. The collector and emitter of the output transistor are connected to respectively pin 15 and pin14, allowing for normal or inverted output pulses. An internally grounded emitter would cause untolerable voltage spikes over the bonding wire, especially at high output currents.

This current capability of the output transistor is 40mA peak for $V_{CE} \alpha$ 0.4V. An internal clamping diode to the supply voltage protects the collector against over-voltages. The maximum voltage at the emitter (pin 14) must not exceed +5V. A gate, activated by one of the set or reset pulses, or by a command from the start-stop circuit will immediately switch-off the output transistor by short-circuiting its base. The external inhibitor (pin 13) operates also via this base.

Inhibitor

As indicated in Figure 4-73A, the output of this NPN comparator will block the output

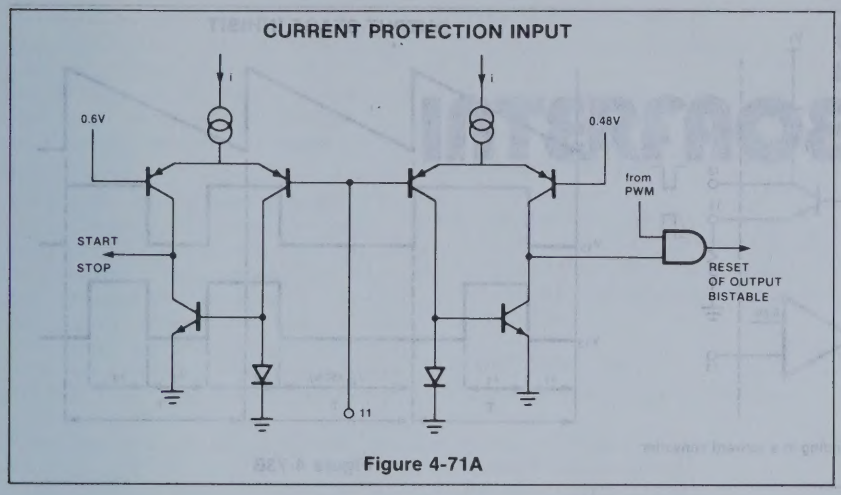


Figure 4-71A

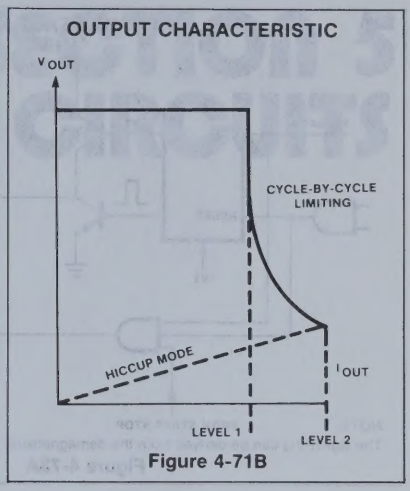


Figure 4-71B

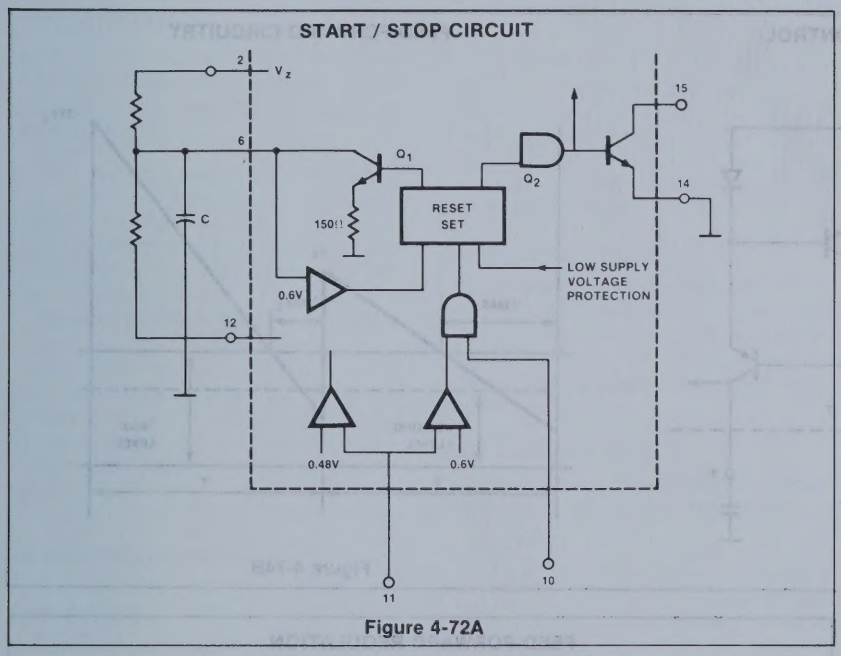


Figure 4-72A

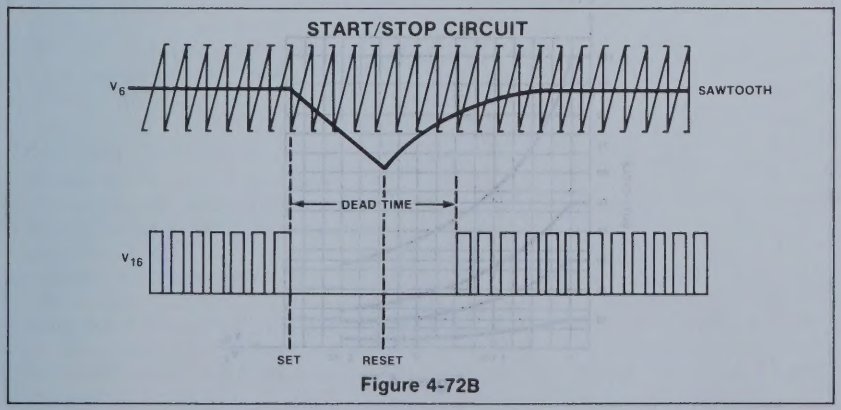


Figure 4-72B

pulse, when a voltage above 0.6V is applied to pin 13. A specific application for this function is to prevent saturation of forward converter transformers. This is indicated in Figure 4-73B.

Feed-forward (Pin 16)

The basic formula for a forward converter is

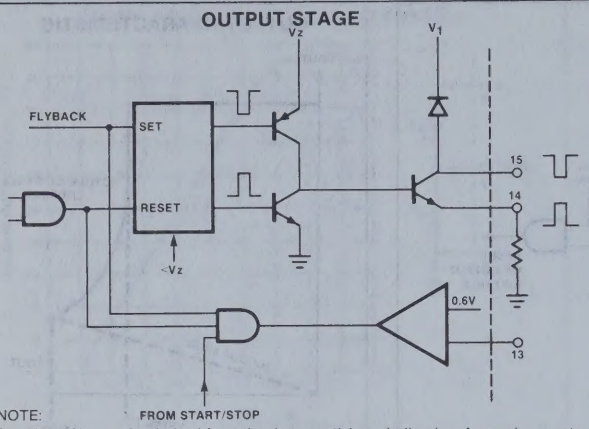
$$V_{out} = \frac{\delta V_{in}}{n} \quad (n = \text{transformer ratio})$$

This means that in order to keep V_{out} at a constant value, the duty cycle δ must be made inversely proportional to the input voltage. A preregulation (feed-forward) with the function $\delta \sim \frac{1}{V_{in}}$ can ease the feedback-loop design.

This loop now only has to regulate for load variations, which require only a low feedback gain in the normal operation area. The transformer of a forward converter must be designed in such a way that it does not saturate, even under transient conditions, where the maximum inductance is determined by $\delta_{max} \times V_{IN}$ max. A regulation of $\delta_{max} \sim \frac{1}{V_{IN}}$ will allow for a considerable reduction or simplification of the transformer. The function of $\delta \sim \frac{1}{V_{IN}}$ can be realized by using pin 16 of the NE5560.

Figure 4-74A shows the electrical realization. When the voltage at pin 16 exceeds the stablilized voltage V_Z (pin 2), it will increase the charging current for the timing capacitor on pin 8.

The operating frequency is not affected, because the upper trip level for sawtooth



NOTE:
The signal V_{13} can be derived from the demagnetizing winding in a forward converter.

Figure 4-73A

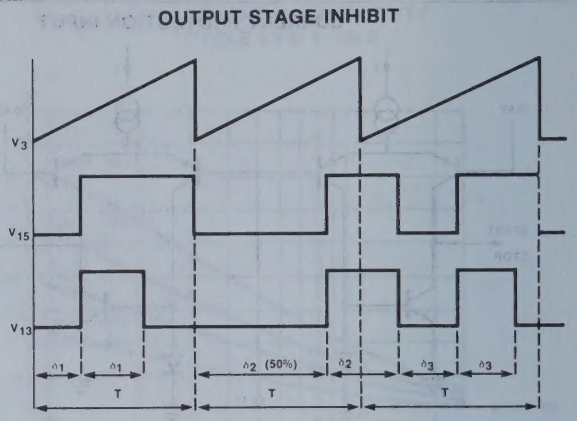


Figure 4-73B

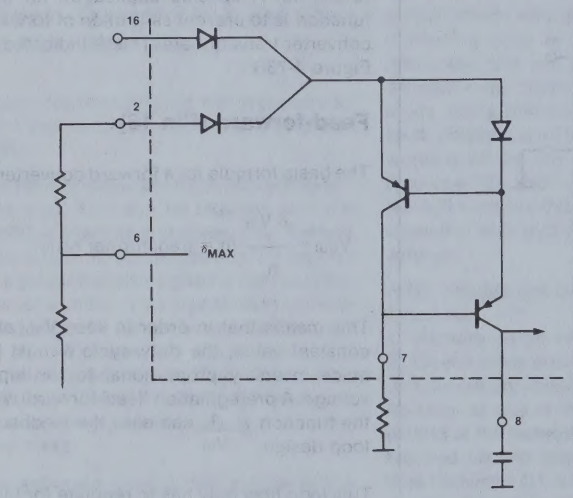


Figure 4-74A

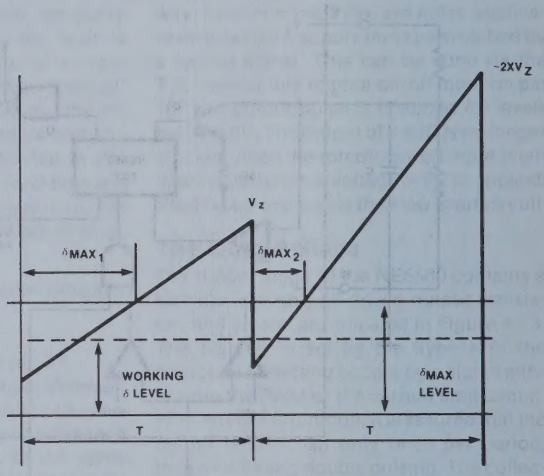


Figure 4-74B

increases also. Note that the δ_{max} voltage on pin 6 remains constant because it is set via V_Z. Figure 4-74B visualizes the effect on δ_{max} and the normal operating duty cycle δ. For V16 = 2xV_Z these duty cycles have halved. The graph for δ = f(V16) is given in Figure 4-75.

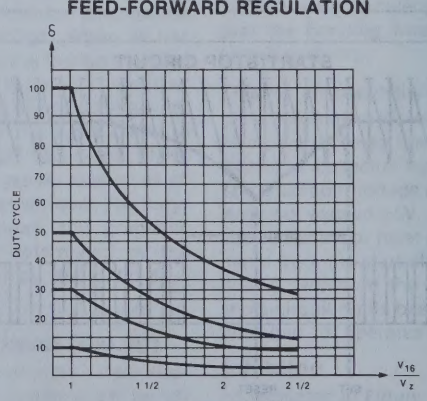
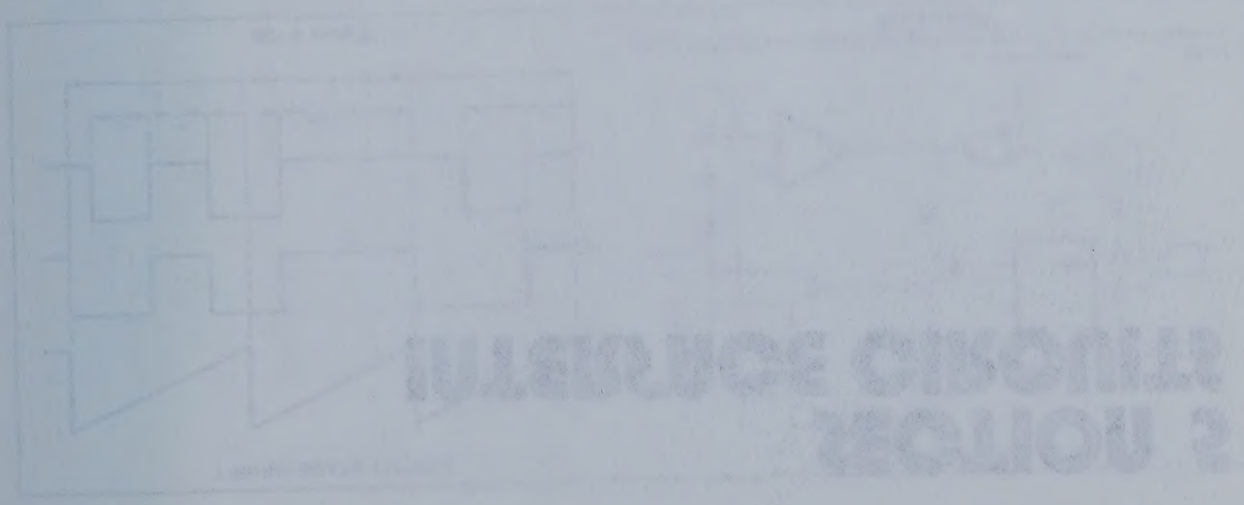


Figure 4-75

SECTION 5
INTERFACE CIRCUITS



INTRODUCTION

Large systems are comprised of many different subsystems, all of which must interface to complete the system. All types of circuits, including linear, digital and discrete are often used in the subsystems.

Interface circuits provide the necessary function of tying the parts of a system together. These circuits are usually not purely linear or digital but contain both types of circuit functions. For instance, sense amplifiers are designed for interface between low level memory outputs and bipolar levels, while differential comparators are designed for interface between analog systems and TTL/DTL systems. In general, this section will cover such devices as comparators, sense amplifiers, line drivers/receivers, and display drivers.

CONVERTERS

Digital communications, digital instruments and displays have created a demand for low cost reliable converters. Key factors in this demand are:

- The need to communicate with digital computers for processing and storage of analog signals.
- Severe limitations encountered in reliable analog data transmission over any considerable distance.
- The need for more easily readable displays.

General application areas for converters include: Data processing, data transmission, graphics and displays, audio systems, control systems and arithmetic operations.

Specific Applications

Test Systems

- Transistor tester (Force I_B and I_C)
- Resistor matching
- Programmable power supplies
- Programmable pulse generators
- Programmable current source
- Function generators (ROM drive)

Arithmetic Operations

- Analog division by a digital word
- Analog quotient of 2 digital words
- Analog product of 2 digital words—squaring
- Addition and subtraction with analog output
- Magnitude comparison of 2 digital words
- Digital quotient of 2 analog variables
- Arithmetic operations with words from different logic families

Graphics and Displays

- Polar to rectangular conversion
- CRT character generation
- Chart recorder driver
- CRT display driver

Data Transmission

- Modern transmitter
- Differential line driver
- Party line multiplexing of analog signals
- Multi-level 2-wire data transmission
- Secure communications (constant power dissipation)

Control Systems

- Reference level generator for setpoint controllers
- Positive peak detector
- Negative peak detector
- Disc drive head positioner
- Microfilm head positioner

Audio Systems

- Digital AVC and reverberation
- Music distribution
- Organ tone generator
- Audio tracking A/D
- Speech compression and expansion
- Audio digitizing and decoding

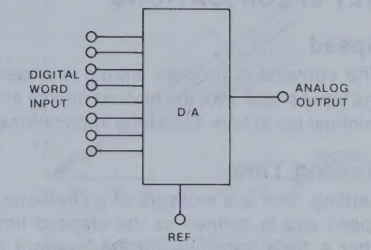
D/A CONVERTERS

D/A converters perform the function of converting a digitally coded signal input into an analog signal output (See Figure 5-1). D/A converters are useful in systems requiring analog signals derived from digital data.

DAC Building Blocks

The actual implementation of a D/A system contains four separate parts: A reference quantity; a set of binary switches to simulate binary coefficients $B_1 \ldots B_N$; a weighting network; and an output summing means.

CONVERSION OF A DIGITALLY CODED SIGNAL INPUT INTO AN ANALOG SIGNAL OUTPUT



Output = Ref. x digital word

$$\text{Output} = \text{Ref.} \times \left(\frac{B_1}{2} + \frac{B_2}{4} + \ldots + \frac{B_N}{2^N}\right)$$

Figure 5-1

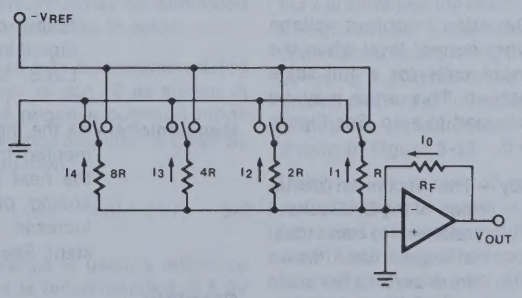
Binary-Weighted Ladder Employing Voltage Switching

The disadvantages of a binary-weighted ladder employing voltage switching include: A wide range of resistor values which are used in weighting the network; and nodal capacitances which are charged/discharged during conversion. See Figure 5-2.

R-2R Ladder Network Employing Current Switching

The advantages of this type of network include: No need for a wide range of resistor

BINARY-WEIGHTED LADDER EMPLOYING VOLTAGE SWITCHING



$$V_{OUT} = \frac{R_F}{R} V_{REF} \times \left(b_1 + \frac{b_2}{2} + \frac{b_4}{4} + \frac{b_8}{8}\right)$$

Figure 5-2

values; and current switching eliminates transients in nodal parasite capacitances. See Figure 5-3.

KEY SPECIFICATIONS

Speed

The conversion process should represent the input signal with the highest fidelity and minimal lag in time (Real time applications).

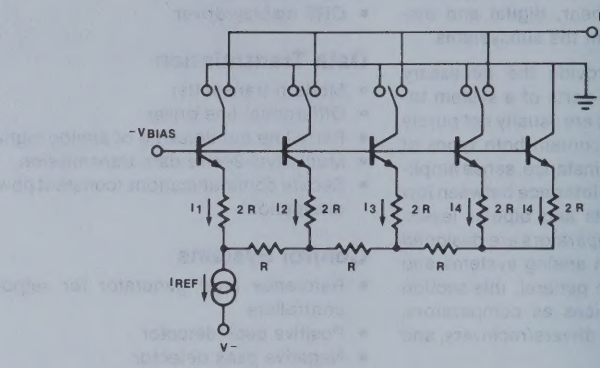
Settling Time

Settling time is a measure of a converter's speed and is defined as the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ±1/2 L.S.B. See Figure 5-4.

Errors

Offset Error —The output voltage of DAC with zero code input. Offset can and usually is trimmed to zero with an offset zero adjust potentiometer. See Figure 5-5.

R-2R LADDER NETWORK EMPLOYING CURRENT SWITCHING



$$I_{OUT} = I_{REF} \times \left(\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{} \right)$$

Figure 5-3

DAC PRODUCTS OVERVIEW

	MC1408 6-7-8	SE/NE5007/8/9	SE/NE5018/19	SE/NE5118/19	NE5020	NE5120	NE5022
Resolution	8 bit	8 bit	8 bit	8 bit	10 bit	10 bit	10 bit
Relative Accuracy	.78/ .39/ .19	.39/ .19/ .1	.19/ .1	.19/ .1	.05	.05	.05
Settling Time	300ns	60ns	2μs	200ns	4μs	500ns	4μs
Output	I	I & $\overline{I}$	V	I	V	I	±V
Features	Standard	Complementary Current Outputs	Bus Compatible input latches ref voltage	High speed current out version of NE5018	8 bit bus compatible	10 bit accuracy	±10V bipolar output

Table 5-1

Gain Error —Deviation in output voltage from correct level when the input calls for a full scale output. This error may be trimmed to zero. See Figure 5-6.

Relative Accuracy —The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full scale -1 L.S.B. See Figure 5-7.

Differential Non-Linearity — Incremental error from any ideal L.S.B. analog output change when the digital input is changed 1 L.S.B.. See Figure 5-8.

Monotonicity — As the input code is incremented from one code to the next in sequence, the analog output will either increase or remain constant. See Figure 5-9.

Stability

Stability is a measure of the independence of converter parameters with respect to variations in external conditions such as temperature and supply voltage.

Temperature Coefficient —The effects of temperature changes of the output. Specified as %F.S. change.

Supply Rejection —Ability to resist changes in the output with supply changes, specified as % full scale change.

Long Term Stability —Measure of how stable the output is over a long period of time.

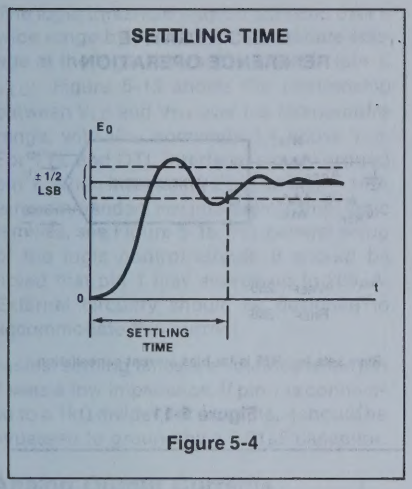
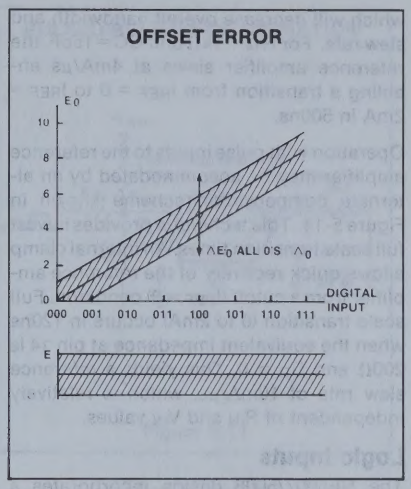


Figure 5-4



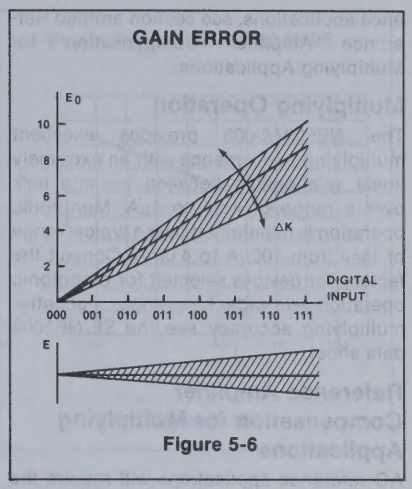


Figure 5-6

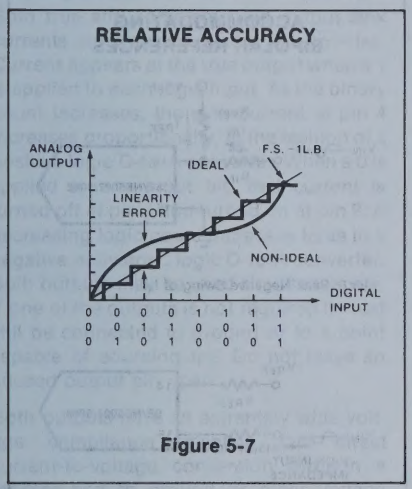


Figure 5-7

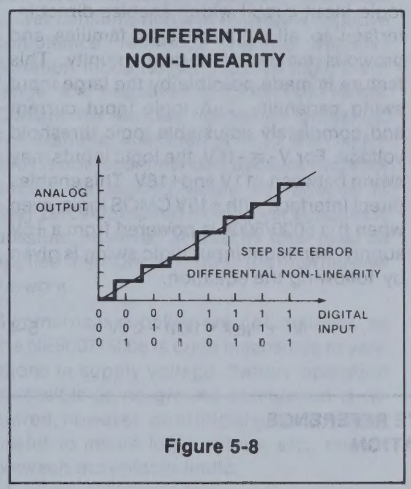

DIFFERENTIAL NON-LINEARITY
ANALOG OUTPUT
STEP SIZE ERROR
DIFFERENTIAL NON-LINEARITY
0 0 0 0 1 1 1 1
0 0 1 1 0 0 1 1
0 1 0 1 0 1 0 1
DIGITAL INPUT

Figure 5-8

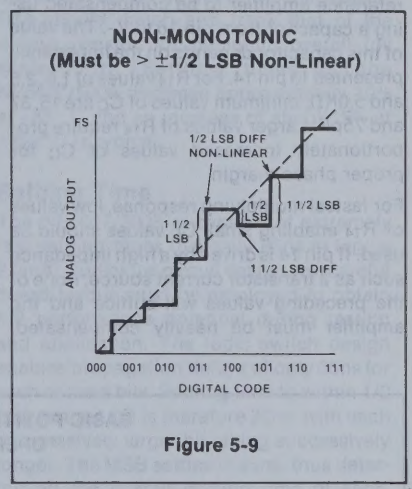


Figure 5-9

NE5007/5008 DAC

Reference Amplifier Setup

The NE5007/5008 is a multiplying D-to-A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by this equation where $I_{REF} = I_{14}$.

$$I_{FS} = \frac{255}{256} \bullet I_{REF} \qquad 5\text{-}1$$

In positive reference applications shown in Figure 5-10, an external positive reference voltage forces current through R14 into the V_{REF} (+) terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to V_{REF} (–) at pin 15, shown in Figure 5-11. Reference current flows from ground through R14 into V_{REF} (+) as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. R15 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15 as shown in Figure 5-12. The negative common mode range of the reference amplifier is given by the following equation.

$$V_{CM-} = V- + (I_{REF} \bullet 1k\Omega) + 2.5V \qquad 5\text{-}2$$

When a dc reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference R14 should be split into 2 resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a + 10.0V reference is recommended for optimum full scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in Figure 5-13.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. The recommended range for operation with a dc reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to V–. For fixed reference operation, a 0.01μF capacitor is recommended. For variable refer-

ence applications, see section entitled Reference Amplifier Compensation for Multiplying Applications.

Multiplying Operation

The NE5007/5008 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA. Consult the factory for devices selected for monotonic operation over wider I_{REF} ranges. For better multiplying accuracy see the SE/NE5009 data sheet.

Reference Amplifier Compensation for Multiplying Applications

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V-. The value of this capacitor depends on the impedance presented to pin 14. For R_{14} values of 1.0, 2.5 and 5.0KΩ, minimum values of C_C are 15, 37 and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest multiplying response, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the preceding values will suffice and the amplifier must be heavily compensated, which will decrease overall bandwidth and slew rate. For R_{14} = 1kΩ and CC = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from I_{REF} = 0 to I_{REF} = 2mA in 500ns.

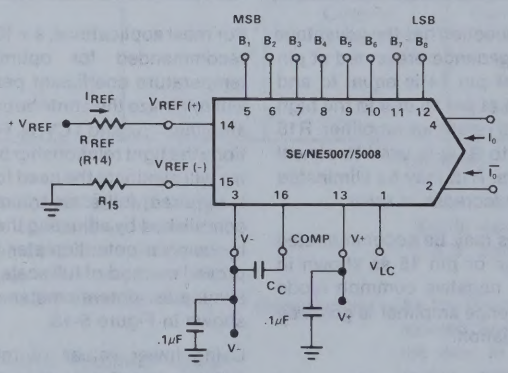
Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme shown in Figure 5-14. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16mA/μs, which is relatively independent of R_{IN} and V_{IN} values.

Logic Inputs

The NE5007/5008 design incorporates a logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V- = -15V, the logic inputs may swing between -11V and+18V. This enables direct interface with +15V CMOS logic, even when the 5000/5008 is powered from a +5V supply. Minimum input logic swing is given by following the equation.

$$V- + (I_{REF} \bullet 1k\Omega) + 2.5V \qquad 5\text{-}4$$

BASIC POSITIVE REFERENCE OPERATION

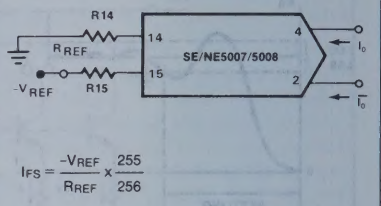


$$I_{FS} \approx +\frac{V_{REF}}{R_{REF}} \times \frac{255}{256} \quad I_O + \overline{I_O} = I_{FS} \text{ for all logic states}$$

For fixed reference, TTL operation typical values are:
V_{REF} = +10,000V, R_{REF} = 5,000Ω R15 ≈ R_{REF},
C_C = 0.01μF, V_{LC} = 0V (ground)

Figure 5-10

BASIC NEGATIVE REFERENCE OPERATION

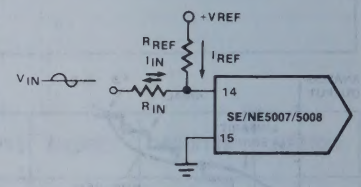


$$I_{FS} = \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

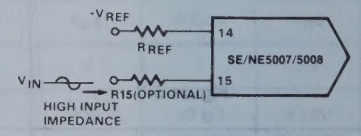
R_{REF} sets I_{FS}, R15 is for bias current cancellation.

Figure 5-11

ACCOMMODATING BIPOLAR REFERENCES



$I_{REF} \geq$ Peak Negative Swing of I_{IN}



+V_{REF} must be above Peak Positive Swing of V_{IN}

Figure 5-12

RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

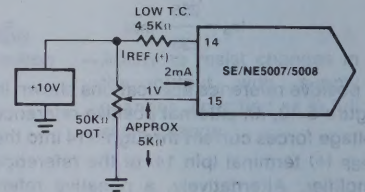


Figure 5-13

The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control (pin 1, V_{LC}). Figure 5-15 shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see Figure 5-16. For general setup of the logic control circuit, it should be noted that pin 1 may source up to 200μA. External circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

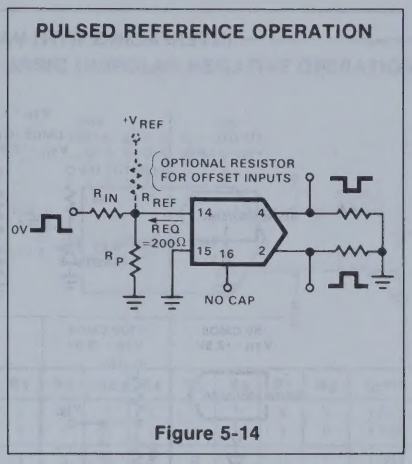


Figure 5-14

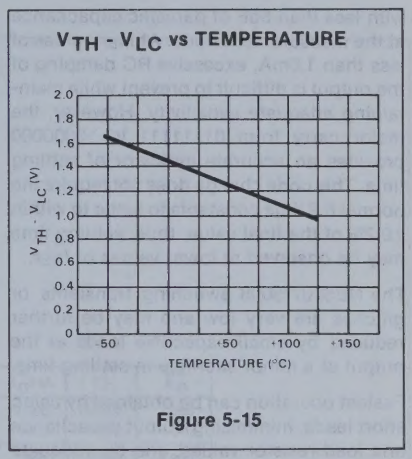


Figure 5-15

Analog Output Currents

Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FS}$. Current appears at the true output when a 1 is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a positive logic D-to-A converter. When a 0 is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases I_O as in a negative or inverted logic D-to-A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}. Do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V- and is independent of the positive supply. Negative compliance is given by equation 5-5.

$$V- + (I_{REF} \bullet 1k\Omega) + 2.5V \qquad 5\text{-}5$$

Note that lower values of I_{REF} will allow a greater output compliance.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as balanced bridge A/D circuits as well as driving center-tapped coils and transformers.

Power Supplies

The NE5007/5008 operate over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of $\pm$5V or less, $I_{REF} \leq$ 1mA is recommended.

Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range. Consult the various figures for guidance. For example, operation at -4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible; however, at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the NE5007/5008 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.

Power consumption may be calculated by this equation.

$$P_D = (I+)(V+) + (I+)(V-) + (2I_{REF})(V-) \qquad 5\text{-}6$$

A useful feature of the NE5007/5008 design is that supply current is constant and independent of input logic states. This is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

Temperature Performance

The linearity and monotonicity specifications of the NE5007/5008 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is low, typically $\pm$10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

Full scale output drift performance will be best with +10.0V references, as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift. Settling times of the NE5007/5008 decrease approximately 10% at -55° C and an increase of about 15% at +125°C is typical.

Settling Time

The NE5007/5008 is capable of extremely fast settling times (typically 85ns at I_{REF} = 2.0mA). Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 85ns, thus determining the overall settling time of 85ns. Settling to 6-bit accuracy requires about 65 to 70ns. The output capacitance of the 5007/5008 including the package is approximately 15pF. Therefore the output RC time constant dominates settling time if RL > 500Ω.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

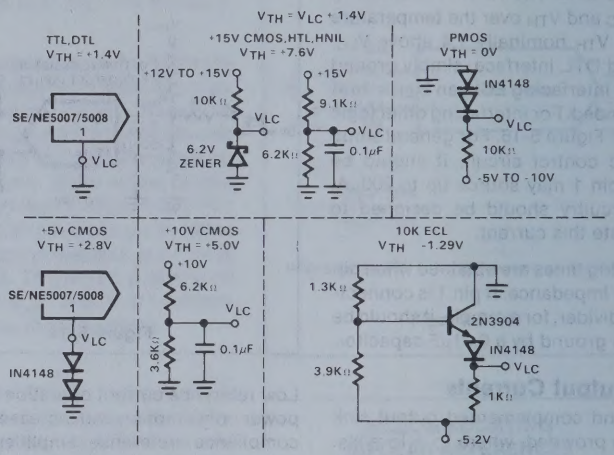
Measurement of settling time requires the ability to accurately resolve $\pm$4μA. Therefore a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Figure 5-17 uses a cascode design to permit driving a 1kΩ load

with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value; thus, settling time may be observed at lower values of I_{REF}.

The NE5007/5008 switching transients or glitches are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is dependent of input logic states. 0.1μF capacitors at the supply pins provide full transient performance.

INTERFACING WITH VARIOUS LOGIC FAMILIES



NOTE

Do not exceed negative logic input range of DAC

Figure 5-16

SETTLING TIME MEASUREMENT

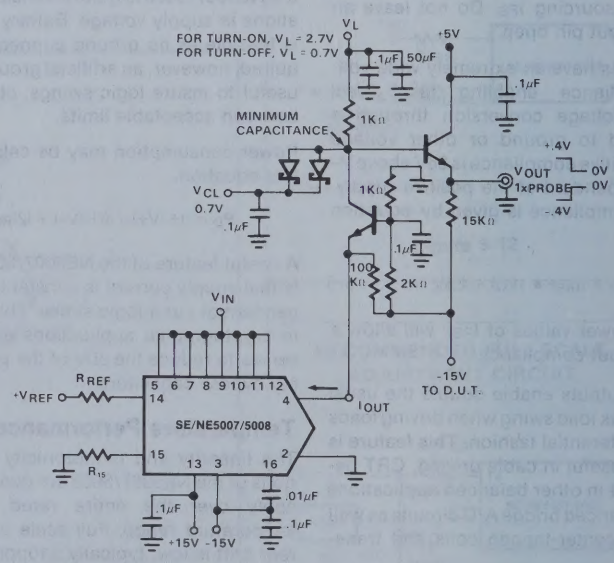
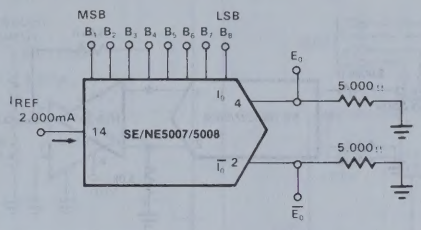


Figure 5-17

TYPICAL APPLICATIONS

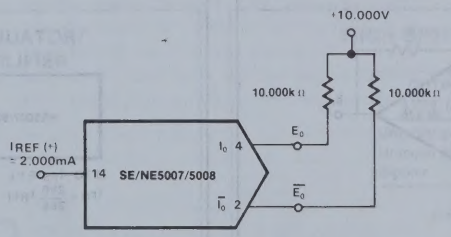
BASIC UNIPOLAR NEGATIVE OPERATION



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
Full scale	1	1	1	1	1	1	1	1	1.992	000	-9.960	.000
Full scale - LSB	1	1	1	1	1	1	1	0	1.984	.008	-9.920	-.040
Half scale + LSB	1	0	0	0	0	0	0	1	1.008	.984	-5.040	-4.920
Half scale	1	0	0	0	0	0	0	0	1.000	.992	-5.000	-4.960
Half scale - LSB	0	1	1	1	1	1	1	1	.992	1.000	-4.960	-5.000
Zero scale + LSB	0	0	0	0	0	0	0	1	.008	1.984	-.040	-9.920
Zero scale	0	0	0	0	0	0	0	0	.000	1.992	.000	-9.960

Figure 5-18

BASIC BIPOLAR OUTPUT OPERATION

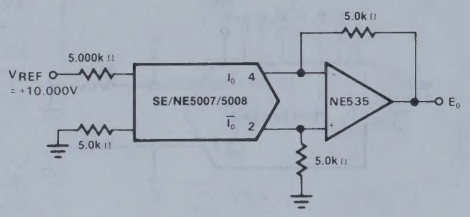


	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O	$\overline{E_O}$
POS full scale	1	1	1	1	1	1	1	1	-9.920	+10.000
POS full scale - LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero scale + LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero scale - LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg full scale + LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg full scale	0	0	0	0	0	0	0	0	+10.000	-9.920

Figure 5-19

TYPICAL APPLICATIONS (Cont'd)

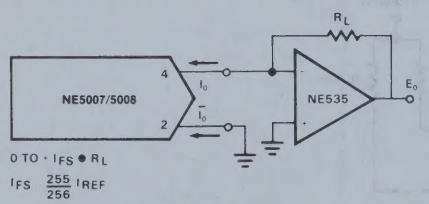
SYMMETRICAL OFFSET BINARY OPERATION



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O
POS full scale	1	1	1	1	1	1	1	1	+9.920
POS full scale - LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero scale	1	0	0	0	0	0	0	0	+0.040
(–) Zero scale	0	1	1	1	1	1	1	1	-0.040
Neg full scale + LSB	0	0	0	0	0	0	0	1	-9.840
Neg full scale	0	0	0	0	0	0	0	0	-9.920

Figure 5-20

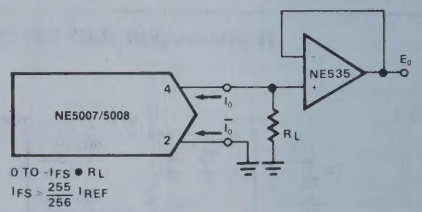
POSITIVE LOW IMPEDANCE OUTPUT OPERATION



For complementary output (operation as negative logic DAC), connect inverting input of OP-amp to I_O (pin 2), connect $\overline{I_O}$ (pin 4) to ground.

Figure 5-21

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



For complementary output (operation as a negative logic DAC), connect non-inverting input of OP-amp to I_O (pin 2); connect I_O (pin 4) to ground.

Figure 5-22

LOW COST 8-BIT 1 MICROSECOND A-TO-D CONVERTER

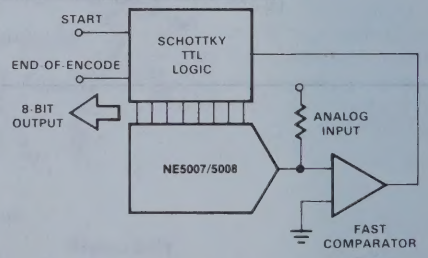
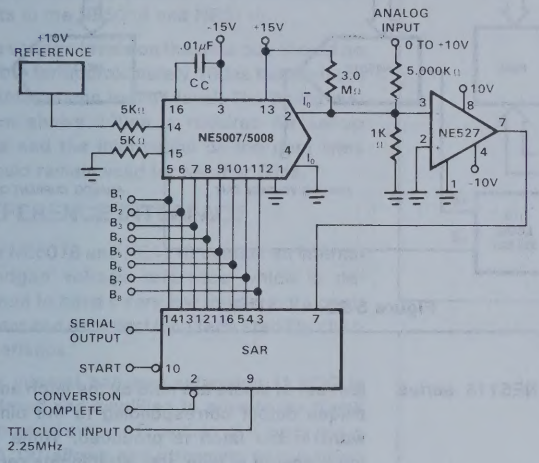


Figure 5-23

3 IC LOW COST A-TO-D CONVERTER

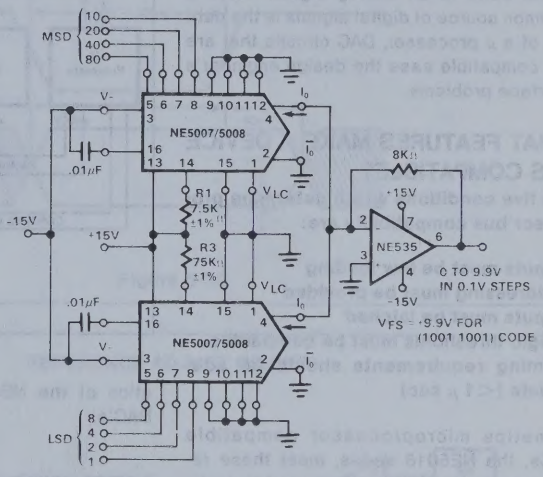


NOTE

Connect "start" to "conversion complete" for continuous conversions.

Figure 5-24

LOW COST 2-DIGIT BCD DAC

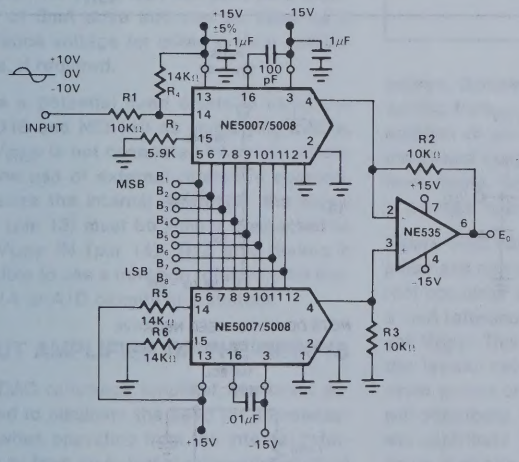


NOTE

Output is directly proportional to positive power supply.

Figure 5-25

DC-COUPLED DIGITAL ATTENUATOR/ PROGRAMMABLE GAIN AMPLIFIER



Bipolar input offset binary output } Performs 2 quadrant multiplications—AC input controls output polarity.

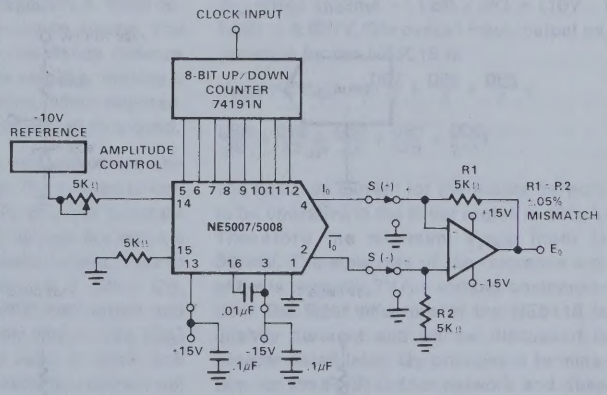
NOTES

1. R1 = R2 = R3
2. R4 = R5
3. E_O DC to 20KHz = ±5V
4. E_O DC to 10KHz = ±10V

Figure 5-26

HIGH SPEED WAVEFORM GENERATOR

OUTPUT TYPE (EO)	SWITCH S(+)	CONDITIONS S(-)
Unipolar positive	+	GND
Unipolar negative	GND	-
Bipolar	+	-



NOTES

1. Bipolar output is symmetrical around zero, adjustable peak to peak amplitude.
2. For triangle wave, count up to full, reverse and count down.
3. For positive-going sawtooth, count up to full; clear, repeat.
4. For negative-going sawtooth, count down, clear, repeat.
5. For other waveforms, use a ROM programmed with the desired function.

Figure 5-27

MICROPROCESSOR COMPATIBLE DACS

DAC products are designed to convert a digital code to an analog signal. Since a common source of digital signals is the data bus of a μ processor, DAC circuits that are bus compatible ease the design engineer's interface problems.

WHAT FEATURES MAKE A DEVICE BUS COMPATIBLE?

The five conditions which determine processor bus compatibility are:

- **Inputs must be low loading**
- **Addressing must be provided**
- **Inputs must be latched**
- **Logic thresholds must be compatible**
- **Timing requirements should be adequate ($<1\ \mu$ sec)**

Signetics microprocessor compatible DACs, the NE5018 series, meet these requirements. In addition, they provide an internal reference source. The NE5018 provides a scaled voltage output, eliminating the need for an external op amp. The NE5118 is identical to the NE5018, except it provides the user with a current output. Figure 5-28 shows a typical microprocessor system with analog I/O using the NE5018 to provide a programmable voltage and an NE5118 to provide a programmable current.

The following discussions detail the operation of the NE5018 and NE5118 series DAC's.

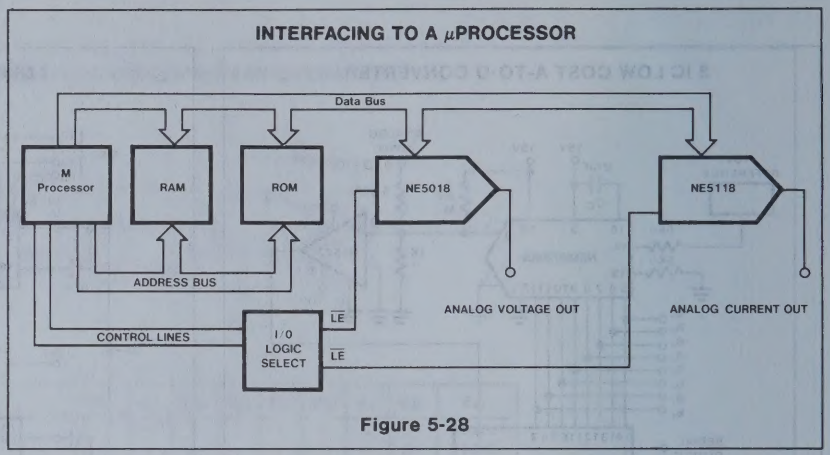


Figure 5-28

LATCH CIRCUIT

The latch circuits of the NE5018 and NE5118 are identical. Both the data inputs and latch enable ($\overline{LE}$) input feature ultra-low loading for ease of interfacing. The eight bit-data latch, controlled by the latch enable input, is static and level sensitive. When ($\overline{LE}$) is low, all the latches become transparent and the output changes as the bit pattern changes on the data bus. When the latch enable returns to its high state, the last set of inputs are held by the latch and a unique output corresponding to the binary word in the latch is produced. While the latch enable is high, the latch inputs represent a high impedance load on the data bus and changes on the data bus have no effect on the DAC output.

The digital logic input for the NE5018 and NE5118 series DAC's utilize a differential input logic system with a threshold level of +1.4 volts with respect to the voltage level on the digital ground pin (Pin 1). Figure 5-29 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

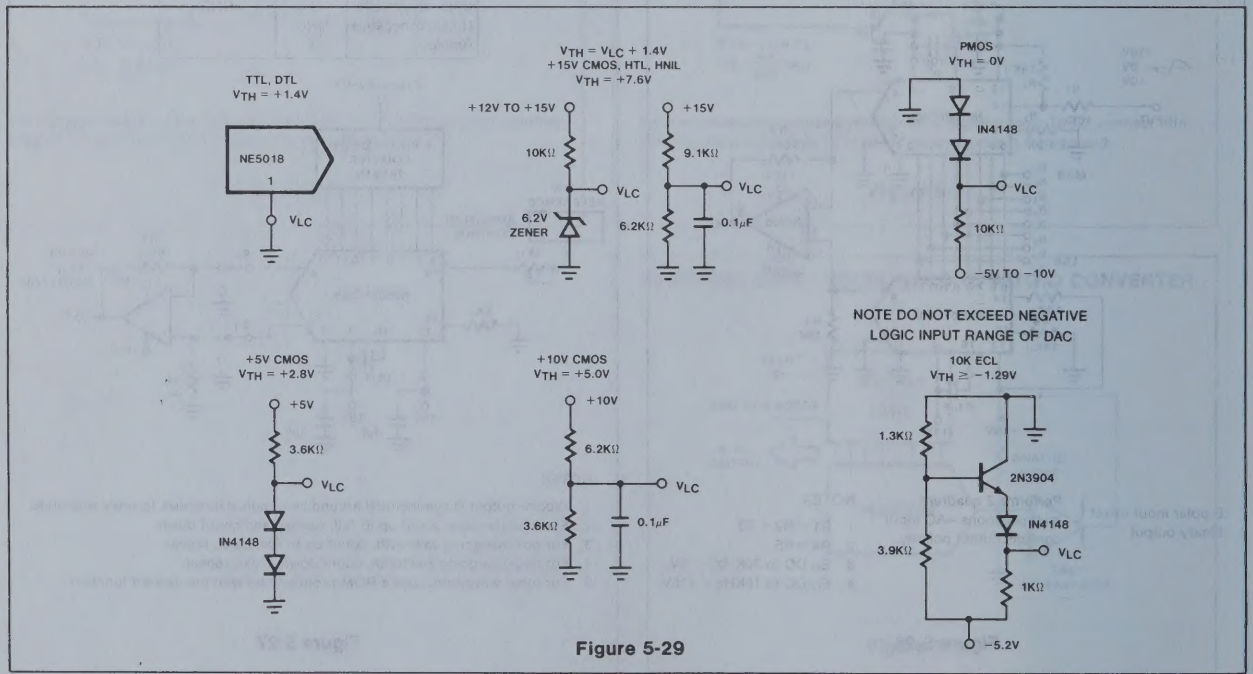


Figure 5-29

To be compatible with microprocessors, the DAC should respond in as short a period as possible to insure full utilization of the μP and I/O data bus lines. Figure 5-30 gives the typical timing requirements of the latch circuits in the NE5018 and NE5118.

The voltage levels on the data bus should be stable for approximately 150ns before latch enable returns to high level. The timing diagram shows 100ns is required for set-up time and the information on the data lines should remain valid for another 50ns.

LATCH ENABLE ($\overline{LE}$) TIMING DIAGRAM for the NE5018 and NE5118

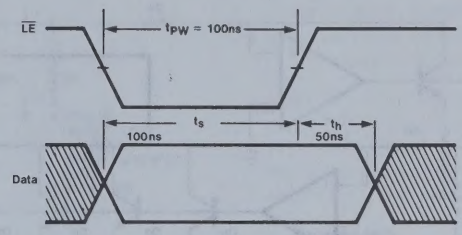


Figure 5-30

REFERENCE ADJUST CIRCUIT

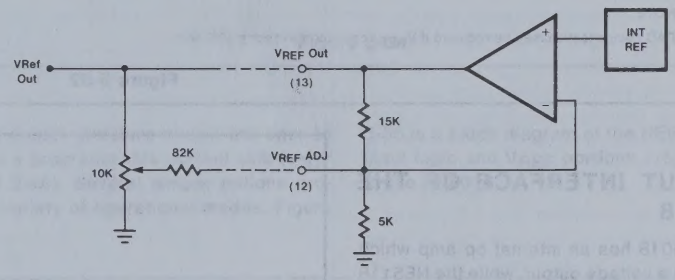


Figure 5-31

REFERENCE INTERFACE

The NE5018 and NE5118 contain an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5 volt reference output. Providing a V_{REF} (ADJ) (pin 12) allows easy trimming of the reference output (pin 13). Use of a 10K pot and series resistor, as shown in figure 5-31, adjusts the gain of the buffer amplifier therefore varying the output reference voltage level.

This network can then be used as a full scale output adjust. A variation in the V_{REF} OUT of ~.8V, results in a corresponding 1.6V variation in the full scale output. This is more than adequate since the untrimmed V_{REF} OUT is typically within 200mv of the nominal 5 volts. The V_{REF} OUT will provide a maximum of 5mA drive and can be used as a reference voltage for other system components, if required.

Since a potential need exists in using the NE5018 and NE5118 as multiplying DAC's, the V_{REF} is not connected internally, allowing the use of external reference sources. To utilize the internal reference, the V_{REF} OUT (pin 13) must be jumper connected to the V_{REF} IN (pin 14). This also makes it possible to use a common reference for other D/A or A/D circuits in a system.

INPUT AMPLIFIER OF THE NE5018

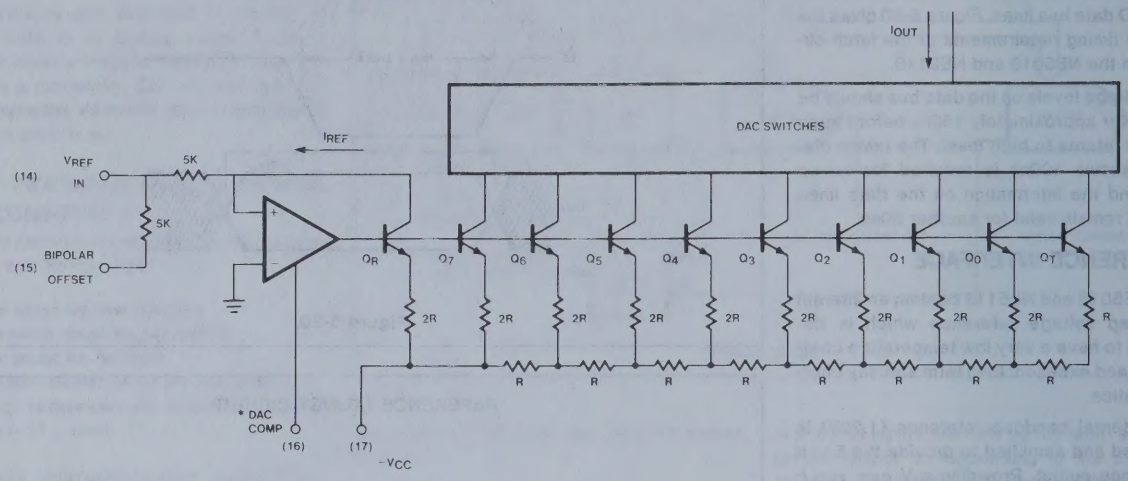
The DAC reference amplifier has been designed to eliminate the need for compensation when operating from the internal reference or from an external reference which is buffered by an op amp or low impedance source. Compensation is required, when operating from a high impedance source. The addition of an external resistance reduces the phase margin of the amplifier making it less stable. Compensation, when required, is a single capacitor from pin 16 to ground.

Figure 5-32 details the input reference amplifier and current ladder. The voltage to current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5 volt V_{REF}. This current sets the input bias to the ladder network. Data bit 7 (DB_7) Q_7, when turned on, will mirror this current and will contribute 1mA to the output. DB_6 (Q_6) will contribute ½ of that value or .5mA, and so on. If all bits are on, the output current will be 2mA - 1 LSB. The full scale V_{OUT} will be ($I_{OUT}R_S$) or (2mA - 1 LSB x 5K) = (10V - 1 LSB) = 9.961V. The overall input/output expression for the NE5018 is:

$$V_{OUT} = 2V_{REF} \times \left(\frac{DB7}{2} + \frac{DB6}{4} + \frac{DB5}{8} + \frac{DB4}{16} + \frac{DB3}{32} + \frac{DB2}{64} + \frac{DB1}{128} + \frac{DB0}{256}\right)$$

The minimum current for the ladder network to be operative in the linear region is 100μA. Therefore the minimum V_{REF} input is 500mV. The slew rate of the reference amplifier is typically .7V/μs without compensation. The input structure of the NE5118 is slightly different and will be discussed in greater detail later. Q_T provides a termination for the R-2R ladder network and does not contribute to I_{OUT}.

R - 2R LADDER NETWORK DEVELOPS A SCALED REFERENCE CURRENT VALUE INTO THE DAC SWITCHING NETWORK



NOTE

DAC compensation may be required if V_{REF} resistance exceeds 10K ohm.

Figure 5-32

OUTPUT INTERFACE OF THE NE5018

The NE5018 has an internal op amp which provides a voltage output, while the NE5118 is a current output device. The NE5018 output op amp is a two stage design with feedforward compensation. Having a slew rate 10V/μs, it provides a voltage output from 0 to 10V (±.2%) typically within 2 μs (the time allowed for the output voltage to settle to within ½ LSB). Compensation must be provided externally as shown in figure 5-33.

The addition of the optional diode between the summing node (Pin 20) and ground prevents the DAC current switches from driving the op amp into saturation during large signal transitions which would increase the settling time.

Zero adjust circuits such as the one shown in figure 6 may also be connected to the summing node to provide a means to zero the output when all zeros are present on the input. Not all applications require a zero adjust circuit since the untrimmed zero scale is typically less than 5mV. Excess stray capacitance at the sum node of the output op amp may necessitate the use of a feedback capacitor from V_{OUT} to the sum node (C_{FF}) to insure stability of the op amp. Typical values of C_{FF} range from 15 to 50pF. The rated load of the op amp is ~ 2Kohm. For stability, the load capacitance should be minimized (50pF max).

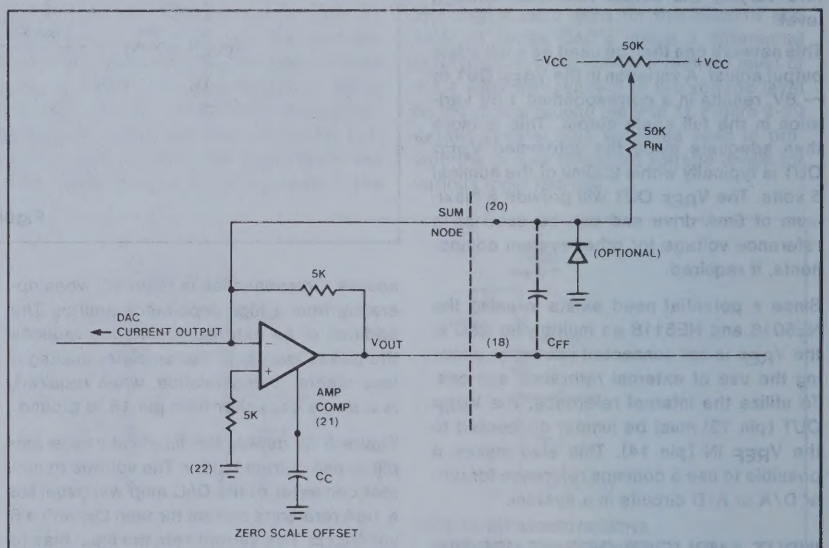


Figure 5-33

MODES OF OPERATION OF THE NE5018

The NE5018 has two basic modes of operation: unipolar and bipolar. When operating in the unipolar mode the output range is 0 to +10 volts. To change from unipolar to bipolar operation the bi-polar offset pin is connected to the summing node. This provides the 5 volt offset required for this mode of operation. The output now will have a range from −5 to +5 volts. Figure 5-34 details the connection of the NE5018 in the bi-polar mode of operation.

With the bi-polar offset pin (15) connected to the sum node pin (20), it forms a unity gain inverter with an input of $+V_{REF}$. The bi-polar offset develops an I_{REF} current across the internal 5K resistor. This current is then fed to the sum node of the output amplifier where it is summed with the current output of the DAC ladder network. Assume for the moment that the current output of the ladder network is 0mA. With a V_{REF} equal to +5 volts, I_{REF} is 1mA and the output of the op amp is converted to −5V. If the DAC switches are now set to full scale, the current from the DAC ladder is 2mA. This is summed against the 1mA I_{REF} and causes the output of the op amp to swing from −5V to +5 volts.

$(I_{DAC} - I_{REF})$ 5K = (2mA - 1mA) 5K = +5 volts

Since the bi-polar offset resistor is monolithic, tracking with the 5K feedback resistor of the output amplifier is excellent.

Note that the bi-polar offset pin could not be used when using the DAC in a multiplier application since the V_{OUT} would reflect an inverted input signal.

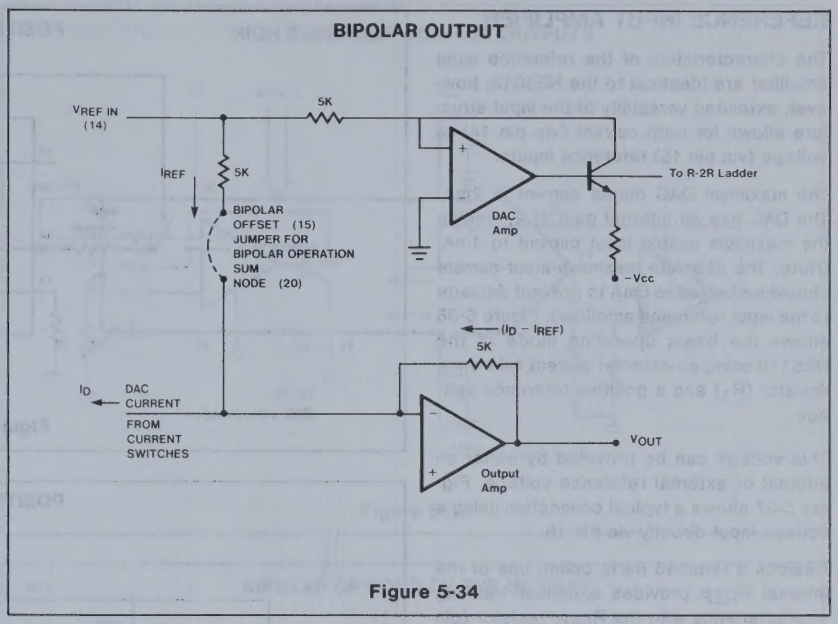
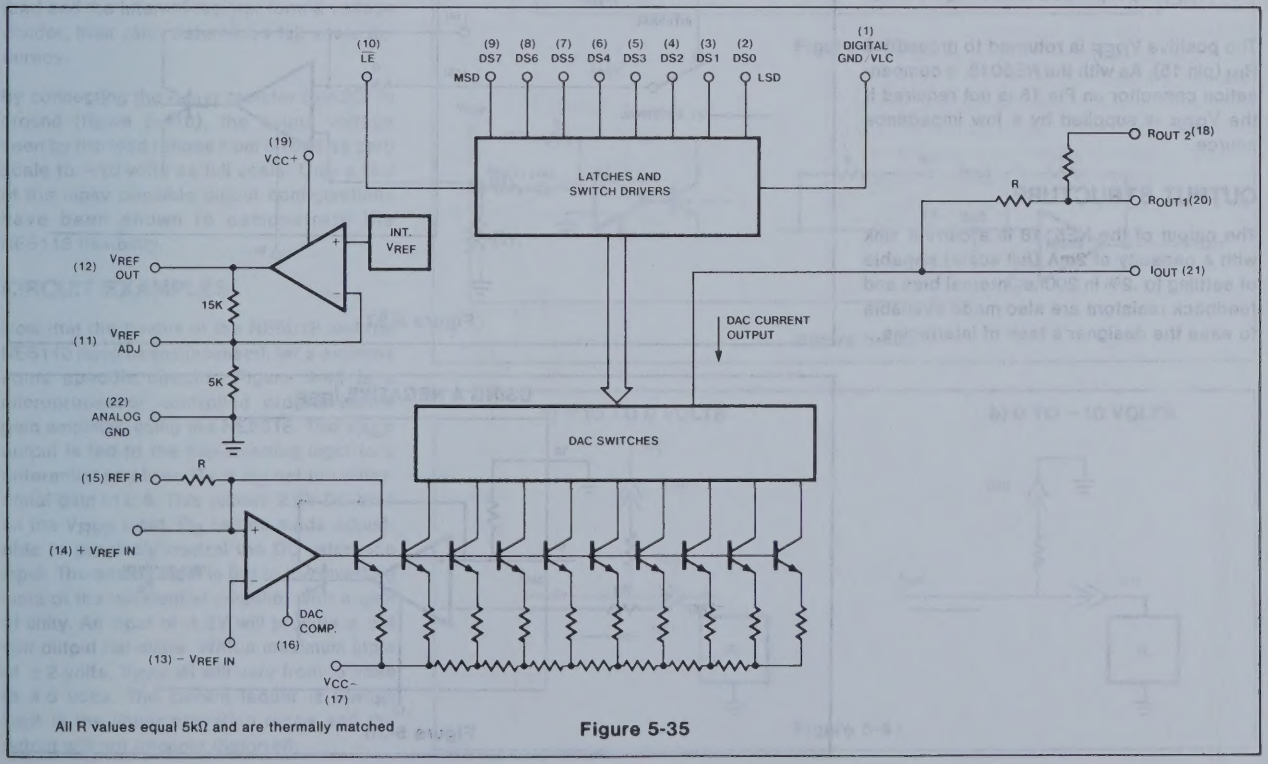


Figure 5-34

NOTES ON THE NE5118 CURRENT OUTPUT DAC

The basic operation of the NE5118 current output DAC is the same as the NE5018. The current output structure allows the user to provide a programmable current sink (I_{OUT} max of 2mA). Several jumper options provide a variety of operational modes. Figure 5-35 is a block diagram of the NE5118. The input logic and V_{REF} portions are identical to the NE5018.

BLOCK DIAGRAM



All R values equal 5kΩ and are thermally matched

Figure 5-35

REFERENCE INPUT AMPLIFIER

The characteristics of the reference input amplifier are identical to the NE5018; however, extended versatility of the input structure allows for both current (via pin 14) or voltage (via pin 15) reference inputs.

The maximum DAC output current is 2mA. The DAC has an internal gain of 2, limiting the maximum usable input current to 1mA. (Note: The absolute maximum input current should be limited to 5mA to prevent damage to the input reference amplifier). Figure 5-36 shows the basic operating mode of the NE5118 using an external current reference resistor (R_1) and a positive reference voltage.

This voltage can be provided by either an internal or external reference voltage. Figure 5-37 shows a typical connection using a voltage input directly via pin 15.

Besides a reduced parts count, use of the internal R_{REF} provides excellent tracking characteristics with the R_{OUT} resistor (pin 20) when developing a high slew rate voltage output. The negative V_{REF} input must be returned to ground directly or through R_2. R_2 is optional and is used to cancel minor errors developed by the input bias currents of the reference amplifier ($R_2 = R_1$). A negative voltage can be the reference by using the $-V_{REF}$ input pin as shown in figure 5-38.

The positive V_{REF} is returned to ground via R_{IN} (pin 15). As with the NE5018, a compensation capacitor on Pin 16 is not required if the V_{REF} is supplied by a low impedance source.

OUTPUT STRUCTURE

The output of the NE5118 is a current sink with a capacity of 2mA (full scale) capable of settling to .2% in 200ns. Internal bias and feedback resistors are also made available to ease the designer's task of interfacing.

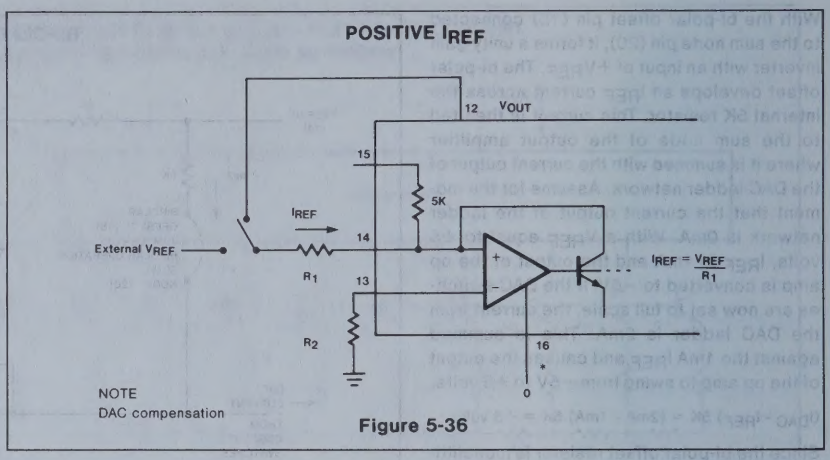


Figure 5-36

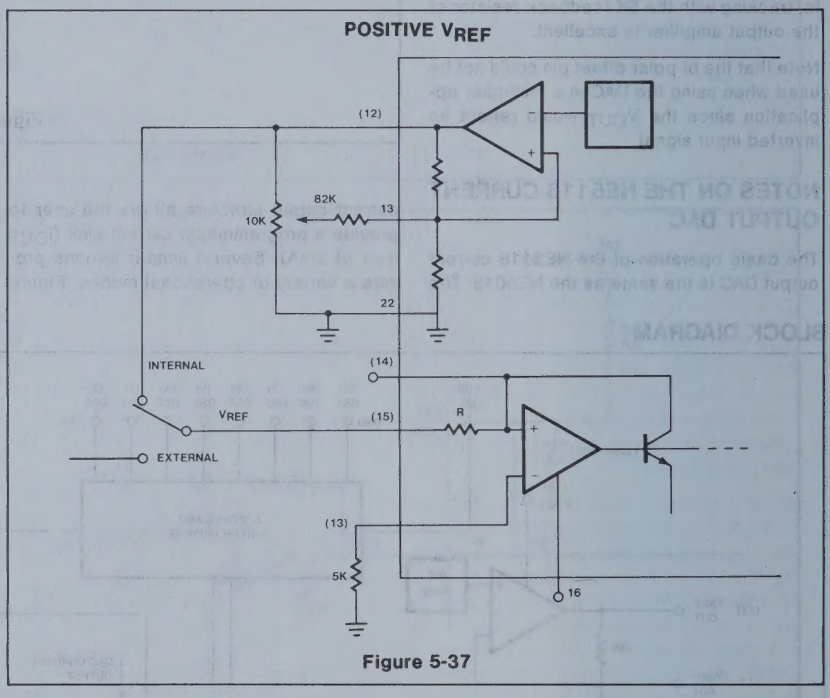


Figure 5-37

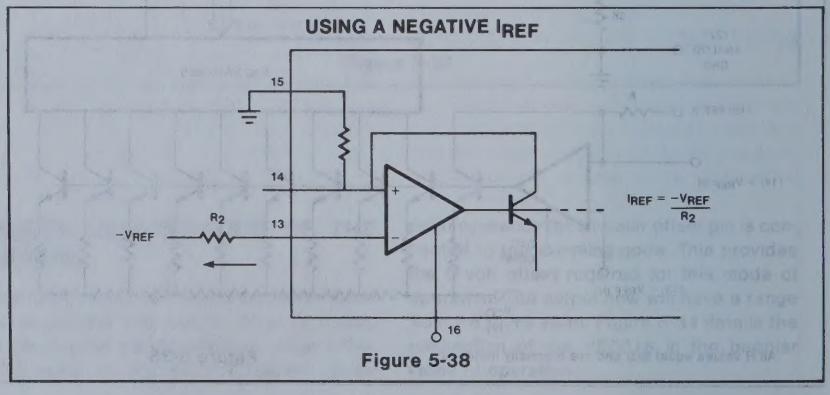


Figure 5-38

Figure 5-39 shows the NE5118 using a current to voltage converter on the output to provide a high slew rate voltage output. Using the NE538 as shown can provide 60V/μs slew rate output. The diode on the inverting node of the op amp improves the response time by preventing saturation of the op amp during large signal transitions. The feedback resistor (R_{OUT1} pin 20) is provided internally; this provides excellent thermal tracking characteristics with the R_{REF} on the input.

Bi-polar operation can be accomplished by connecting the $V_{REF\ OUT}$ (Pin 12) to the R_{OUT} resistor (Pin 20) (Figure 5-40a). The principal is the same as the NE 5018 bipolar operation. The internal resistors exhibit excellent thermal tracking characteristics.

An alternate method of bipolar output operation is shown in Figure 5-40b. The R_{REF} and R_{OUT}, set up a current to voltage converter while two (2) external resistors provide a bipolar offset. R_{EXT_1} and R_{EXT_2} should have similar thermal tracking characteristics.

The NE5118 can provide a voltage output directly when driving a high impedance load as shown in figure 5-41a. With a full scale current of 2mA, pin 20 tied to +10V and a digital input of zero, the high impedance load will see +10V. For a full scale digital input, the load will see 0 volts. Since the load and the internal resistor form a voltage divider, their ratio determines full scale accuracy.

By connecting the R_{OUT} resistor (pin 20) to ground (figure 5-41b), the output voltage seen by the load ranges from 0 volts as zero scale to −10 volts as full scale. Only a few of the many possible output configurations have been shown to demonstrate the NE5118 flexibility.

CIRCUIT EXAMPLES

Now that the basics of the NE5018 and the NE5118 have been discussed, let's examine some specific circuits. Figure 5-42 is a microprocessor controlled programmable gain amplifier, using the NE5018. The V_{REF} output is fed to the non-inverting input to a differential amplifier. $R_1 + R_2$ set the differential gain to 0.5. This places 2.5V DC bias on the V_{REF} input. R_2 can be made adjustable to precisely control the DC reference input. The analog input is fed to the inverting input of the differential amplifier with a gain of unity. An input of ±2V will provide a ±4 volt output full scale. With a maximum input of ±2 volts, V_{REF} IN will vary from .5 volts to 4.5 volts. The current ladder is always kept in the linear operating range and the output will not become distorted.

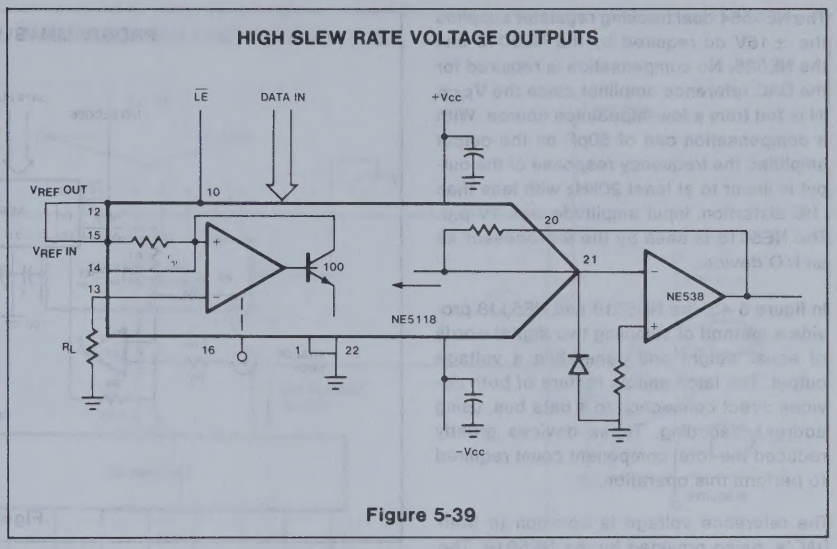


Figure 5-39

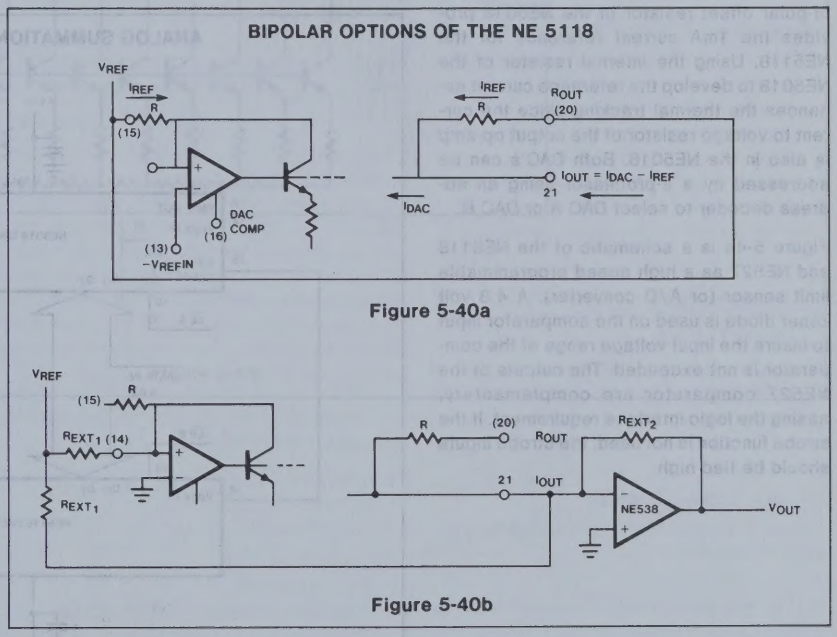


Figure 5-40a

Figure 5-40b

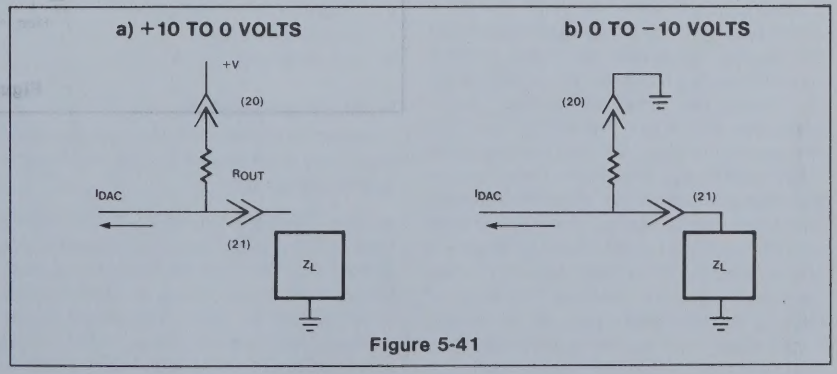


Figure 5-41

The NE5554 dual tracking regulator supplies the ±15V dc required by the NE5018 and the NE535. No compensation is required for the DAC reference amplifier since the V_{REF} IN is fed from a low impedance source. With a compensation cap of 30pF on the output amplifier, the frequency response of the output is linear to at least 20kHz with less than .1% distortion. Input amplitude was 1V p.p. The NE5018 is seen by the μ-processor as an I/O device.

In figure 5-43, the NE5018 and NE5118 provide a method of summing two digital words of equal weight and generating a voltage output. The latch enable feature of both devices direct connection to a data bus, using address decoding. These devices greatly reduced the total component count required to perform this operation.

The reference voltage is common to both DAC's, being provided by the NE5018. The bi-polar offset resistor of the NE5018 provides the 1mA current reference for the NE5118. Using the internal resistor of the NE5018 to develop the reference current enhances the thermal tracking since the current to voltage resistor of the output op amp is also in the NE5018. Both DAC's can be addressed by a μ-processor using an address decoder to select DAC A or DAC B.

Figure 5-44 is a schematic of the NE5118 and NE527 as a high speed programmable limit sensor (or A/D converter). A 4.8 volt zener diode is used on the comparator input to insure the input voltage range of the comparator is not exceeded. The outputs of the NE527 comparator are complementary, easing the logic interface requirement. If the strobe function is not used, the strobe inputs should be tied high.

PROGRAMMABLE GAIN AMPLIFIER

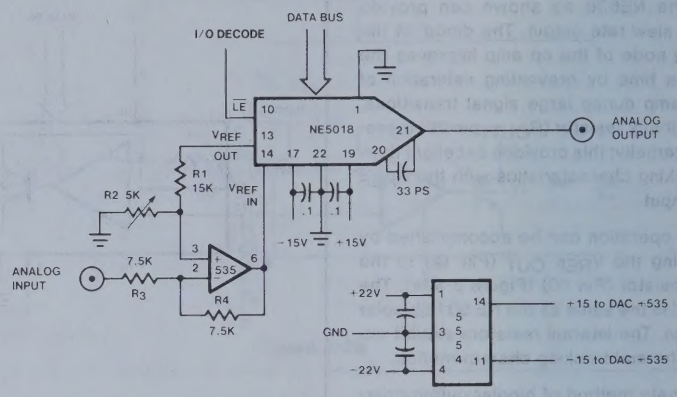


Figure 5-42

ANALOG SUMMATION WITH DIGITAL INPUTS

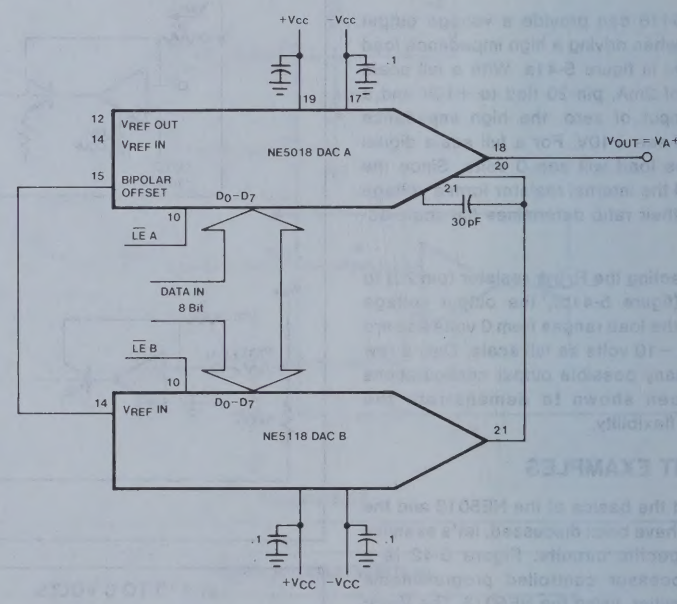


Figure 5-43

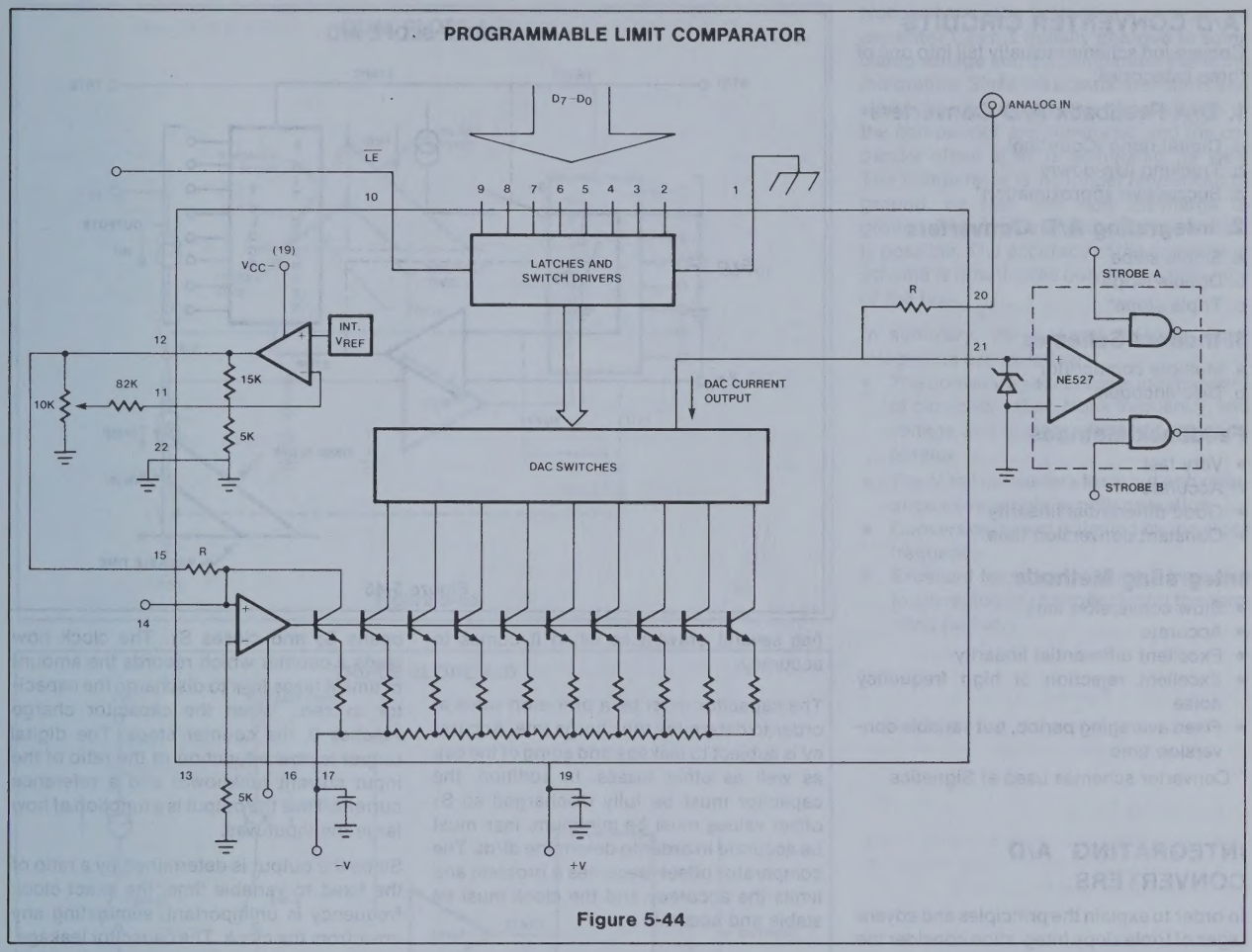

PROGRAMMABLE LIMIT COMPARATOR
D7-D0
ANALOG IN
LE
10
9 8 7 6 5 4 3 2
1
(19)
VCC
LATCHES AND SWITCH DRIVERS
R
20
STROBE A
12
INT. VREF
82K
11
15K
10K
21
NE527
DAC CURRENT OUTPUT
5K
22
DAC SWITCHES
STROBE B
15
R
14
13
5K
16
17
19
-V
+V

Figure 5-44

A/D CONVERTER CIRCUITS

Conversion schemes usually fall into one of three categories:

1. D/A Feedback A/D Converters

a. Digital ramp (Counting)
b. Tracking (Up-down)
c. Successive approximation*

2. Integrating A/D Converters

a. Single slope
b. Double slope
c. Triple slope*

3. Indirect Schemes

a. Multiple comparator
b. Disc encoders

Feedback Methods

- Very fast
- Accurate
- Good differential linearity
- Constant conversion time

Integrating Methods

- Slow conversion time
- Accurate
- Excellent differential linearity
- Excellent rejection of high frequency noise
- Fixed averaging period, but variable conversion time

* Converter schemes used at Signetics

INTEGRATING A/D CONVERTERS

In order to explain the principles and advantages of triple slope integration consider the following integrating techniques.

Single Slope System

Figure 5-45 shows a circuit using a single slope integration.

V_{IN} is the analog signal which is to be converted to a digital output. Initially, S_1 is closed, S_2 is open, and the 8 bit counter is set to zero. When a start pulse is applied to the counter, S_1 opens, S_2 closes and the counter starts counting. Notice that when S_2 closes, the reference current source starts charging C_{EXT}. The voltage on C_{EXT} increases at a linear rate until the charge on C_{EXT} reaches V_{IN}. At that time, the comparator changes state which stops the counter, opens S_2 and closes S_1. The counter now contains a digital value which is related to the amplitude of the input signal. The capacitor charges at a fixed rate. The length of time is variable dependent on the analog input value. This system is very simple to build and only requires a single supply but

SINGLE SLOPE A/D

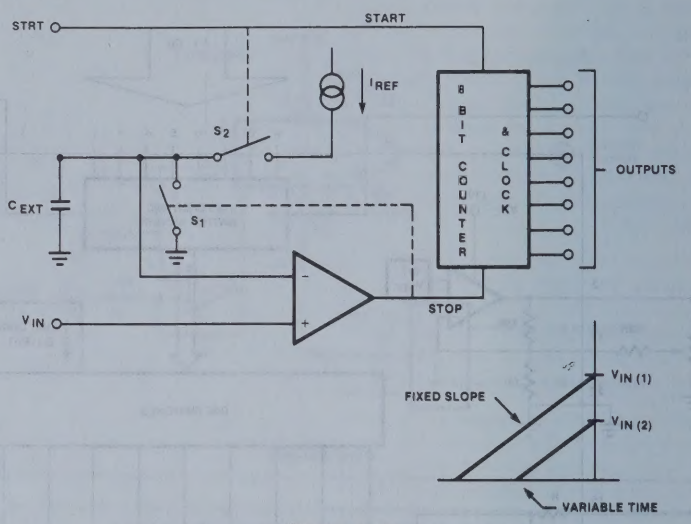


Figure 5-45

has several drawbacks when it comes to accuracy.

The capacitor must be a precision value in order to determine the charge rate. Accuracy is subject to leakage and aging of the cap as well as other losses. In addition, the capacitor must be fully discharged so S_1 offset values must be minimum. I_{REF} must be accurate in order to determine di/dt. The comparator offset becomes a problem and limits the accuracy and the clock must be stable and accurate.

In summary, the single slope system possesses the following:

ADVANTAGES

- Simple to build
- Single supply

DISADVANTAGES

- Poor accuracy
- Capacitor (leakage, losses, aging)
- Clock (stability, accuracy)
- Capacitor switch offset
- Comparator offset
- I_{REF} accuracy

Dual Slope System

To improve accuracy, the dual slope technique was developed. Figure 5-46 shows a dual slope system.

Initially, C_{EXT} is discharged and the counter is at 0. The analog input is converted to a current (I_{IN}). When the start pulse is applied, the clock and control circuit closes S_2 for a fixed period of time. The input signal charges C_{EXT} to some value. At the end of this fixed charge period, the control circuit opens S_2 and closes S_1. The clock now feeds a counter which records the amount of time it takes I_{REF} to discharge the capacitor to zero. When the capacitor charge reaches 0, the counter stops. The digital output is now a function of the ratio of the input current (unknown) and a reference current. Thus the output is a function of how large the input was.

Since the output is determined by a ratio of the fixed to variable time, the exact clock frequency is unimportant, eliminating any error from the clock. The capacitor leakage, aging, and other losses are no longer a factor because the effects are constant and cancel in a ratio based system.

The comparator and capacitor offsets are still a problem and dual supplies are now required since C_{EXT} must discharge to below ground.

In summary, the dual slope system possesses the following:

ADVANTAGES

- Eliminates errors due to errors in clock and capacitor aging

DISADVANTAGES

- Accuracy limited by capacitor and comparator offsets
- Dual supplies required

Triple Slope System

The triple slope method, shown in Figure 5-47, eliminates the capacitor and comparator offset effects on accuracy.

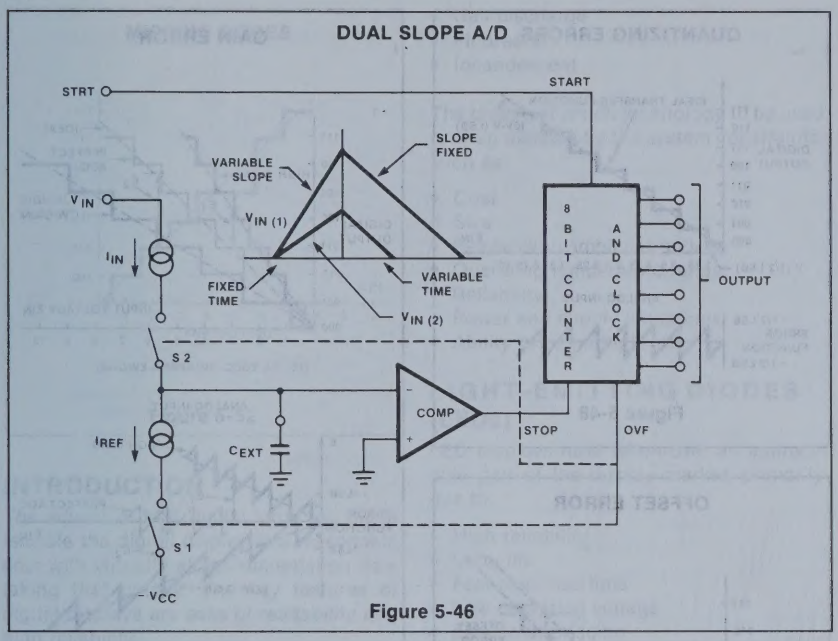


Figure 5-46

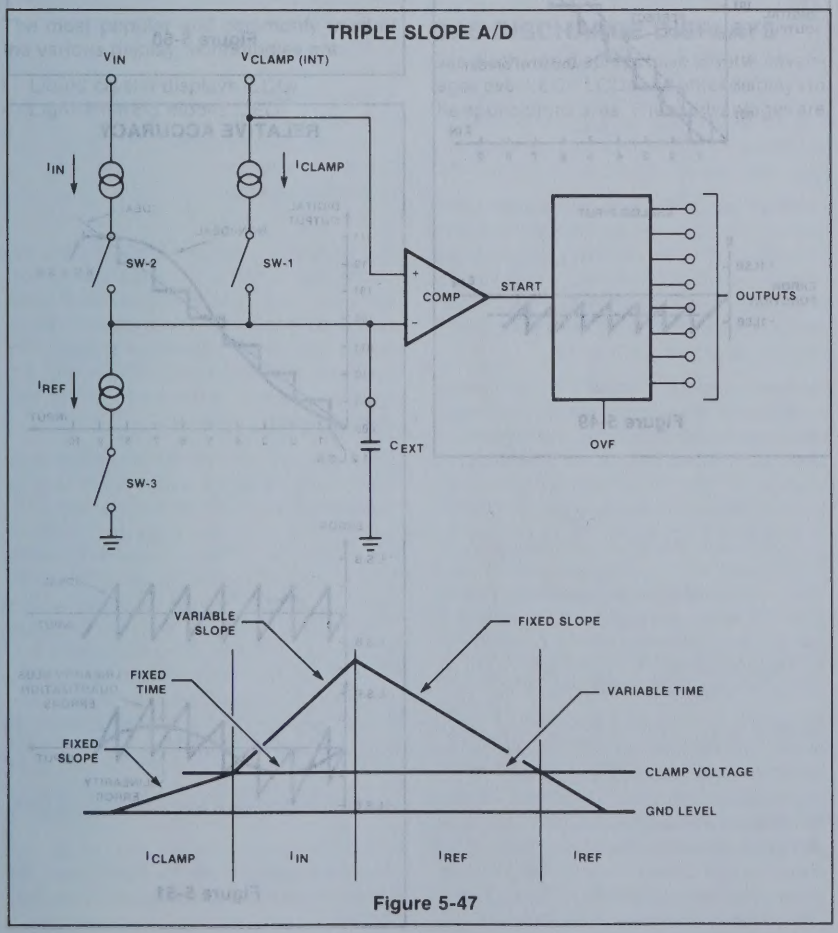


Figure 5-47

Notice that in the triple slope method, the capacitor C_{EXT} is initially charged to some clamp voltage and the comparator starts the integration. Since the comparator starts and stops the conversion, the offset effects of the comparator are eliminated and the capacitor offset error is eliminated as well. The comparator is no longer referenced to ground, so I_{REF} can now discharge to ground. This means single supply operation is possible. The accuracy of the conversion scheme is now limited only by the accuracy of the I_{REF}.

In summary, the features of triple slope integration are as follow:

- The conversion accuracy is independent of capacitor value, clock frequency, and voltage and current offsets of the comparator
- The V to I converters for input and reference allow single supply operation.
- Conversion speed is limited by the clock frequency
- Excellent for noise rejection. This is due to averaging of changes during the sampling period.

5

CONSIDERATIONS FOR A/D CONVERTERS

- Analog input signal range and resolution required
- Linearity requirement and stability
- Conversion speed required
- Monotonicity requirement: Can missing codes be tolerated?
- Character of input signal: Is it noisy, sampled, filtered, slowly varying?
- Transfer characteristics (Type of coding)

A/D CONVERTER TERMS

Resolution

Resolution is the input change required to increment the output between the two adjacent codes. This term also refers to the number of bits in the output word and; hence, the number of discrete output codes the input analog signal can be broken into. Expressed in "bits" resolution.

Transfer Characteristic

The Transfer Characteristic is the relationship of the output digital word (code) to the input analog signal, i.e., Binary, BCD.

Conversion Speed

The Conversion Speed is the speed at which an ADC can make repetitive data conversions.

Quantizing Error

Quantizing Error is an inherent error in the conversion process due to finite resolution (discrete output). See Figure 5-48.

Offset Error

An Offset Error is shown in Figure 5-49.

Gain Error

A Gain Error is shown in Figure 5-50.

Relative Accuracy

Relative Accuracy is the deviation of an actual bit transition from the ideal transition value at any level over the range of the ADC (% F.S.). See Figure 5-51.

Hysteresis Error

A Hysteresis Error is the code transition voltage dependence relative to the direction from which the transition is approached.

Monotonicity

Monotonicity is when the output code either increases or remains the same for increasing analog input signals. The opposite is true in the reverse direction.

Missing Codes

A Missing Code is a code combination that is skipped. See Figure 5-52.

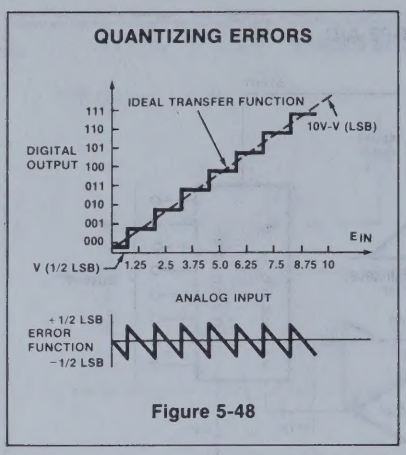


Figure 5-48

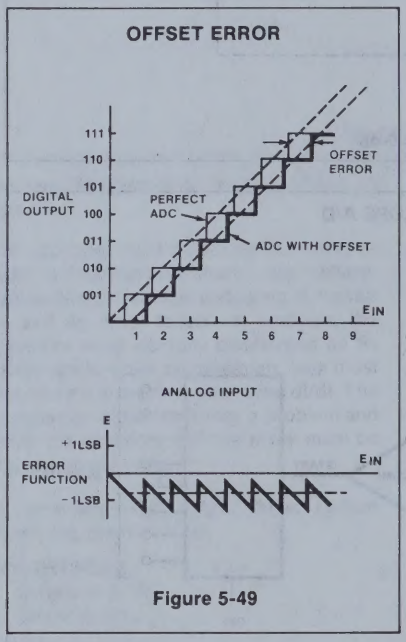


Figure 5-49

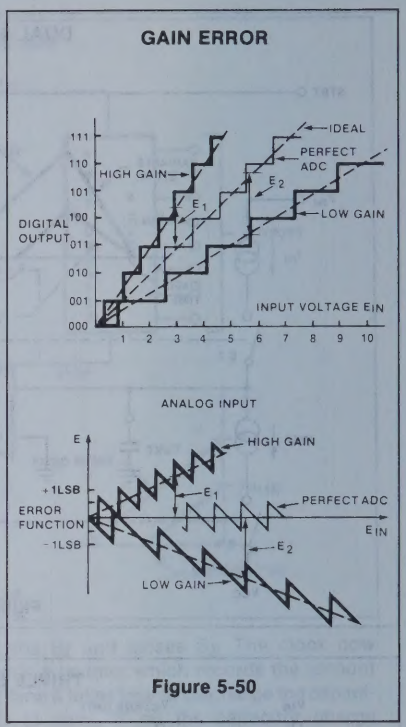


Figure 5-50

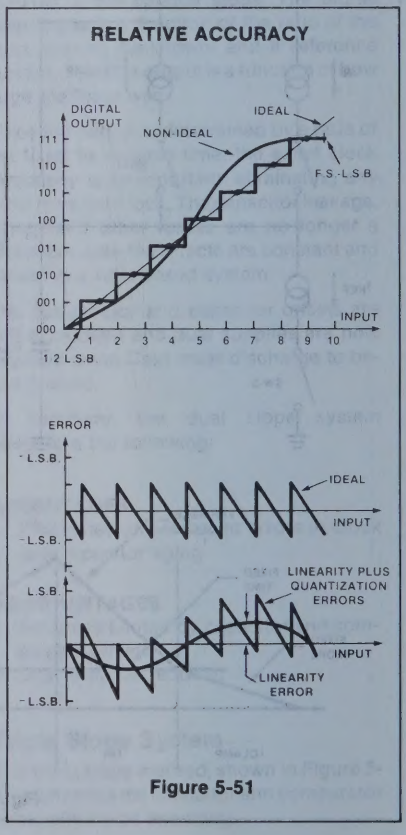


Figure 5-51

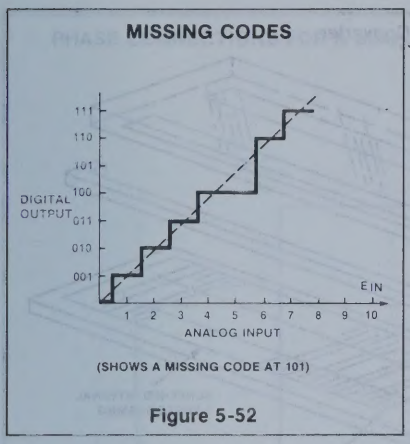


Figure 5-52

INTRODUCTION

The advent of MSI digital logic has made feasible the digital display at a reasonable cost with virtually all instrumentation now taking that course. The key features of digital displays are ease of readability and high reliability.

The most popular and commonly used of the various display technologies are:

- Liquid crystal displays (LCD)
- Light-emitting diodes (LED)
- Gas-discharge
- Fluorescent
- Incandescent

The choice of which technology to be used is often dictated by the system constraints, such as:

- Cost
- Size
- Readability (ambient light)
- Operating temperature range
- Reliability
- Power and supply limitations
- Ability to be multiplexed

LIGHT-EMITTING DIODES (LEDs)

LED displays have taken over an appreciable part of the display market, primarily due to:

- High reliability
- Long life
- Fast response time
- Low operating voltage
- Ease in interfacing

GAS DISCHARGE DISPLAYS

Gas discharge displays have several advantages over LEDs, LCDs and other displays in the applications area. These advantages are generally in products where performance, rather than cost, is of prime importance. These advantages include:

- Larger digits
- Increased readability in bright, ambient light
- High reliability
- Operation in wide temperature extremes

Applications for Gas Discharge Displays

Automotive Industry

- Operating temperature range (-40°F to +120°F)
- LCDs—Freeze at lower temperature
- LEDs—Poor efficiencies at high temperature

Avionics

- Visibility
- LCDs—Difficult to multiplex (poor response)
  Poor operating temperature range
  Need direct light
- LEDs—Poor visibility in bright light

Games

- Size and brightness
- LCDs—Poor viewing angle
- LEDs—Not bright enough

5

NE580 BARGRAPH DRIVER

Although the gas discharge bargraph is not a new type of display device, it has not been widely used so far, partly because of cost of the associated drive circuitry it required.

Signetics Corporation has developed a single IC(NE580) which comprises most of the electronics necessary to interface an analog voltage level to a bargraph display. This will dramatically reduce the cost of using bargraph displays, thus opening a new wide range of possible applications for them.

Because the bargraph display has not found wide applications yet, the principles of operation and drive requirements may not be fully understood.

A gas discharge bargraph display is a device where the cathodes form the visible part of the display. The cathodes are in the form of short bars, or segments, and are arranged in a column to give the effect of a thermometer when lit. The cathodes are printed in conductive ink on a substrate, which is usually blackened to enhance contrast. The anode is a continuous transparent bar printed behind the front glass. The front glass and the substrate are sandwiched together, the space between them being filled with neon gas. This is shown in Figure 5-53.

Glow transfer principle

When an electrical pulse of sufficient magnitude is applied between the anode and any cathode segment, ionization of the gas takes place and a visible glow is produced in the region of the cathode. Once ionization has taken place, charged particles around the glowing cathode diffuse outwards to the adjacent cathode and put it into a state where it will now require a lower firing voltage for ionization to occur.

In Figure 5-53 it can be seen that there is a "keep alive" anode and cathode at the bottom end of the tube, normally hidden from view. This cathode is *permanently* ignited and acts as a source of charged particles for the tub. These particles leak across to the first cathode segment and lower its firing voltage.

After the first cathode has been ignited, it will supply charged particles to the next segment, and so on. By successively firing segments, a continous bar of lighted segments can be made to glow from one end of the tube to the other. This procedure is known as "glow transfer", and it is the principle on which the bargraph display operates.

Phase connections

Bargraph displays can be 3-phase, 5-phase or 6-phase in operation. Let's take a look at what this means.

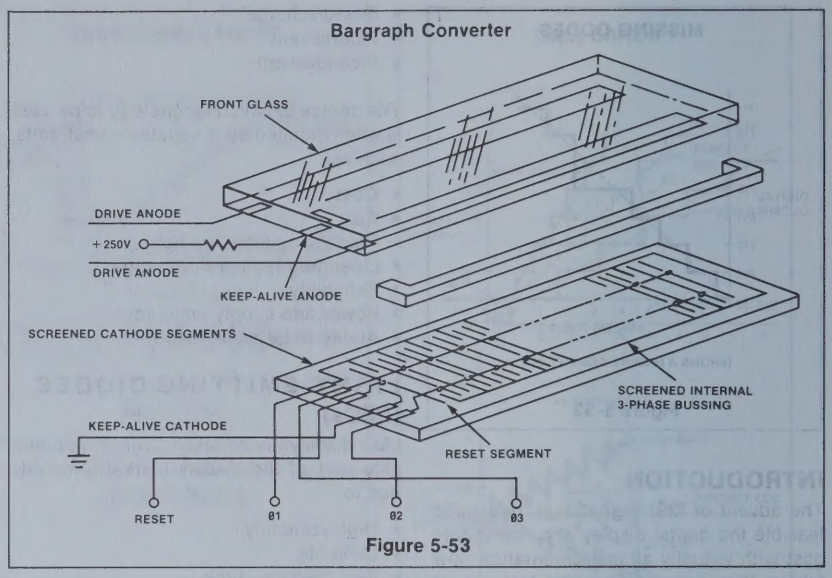


Figure 5-53

If we consider a 200 segment bargraph, then, to fire each segment in turn it would be necessary to have 200 outputs from the drive circuitry, thus making it very complex and extremely expensive. For this reason it is necessary to connect the segments in a bus arrangement, as shown in Figure 5-54.

In the simple 9-segment, 3-phase bargraph shown in Figure 5-54, each segment in turn is connected to an alternate bus. Assume now that segment 1 has received a transfer of charged particles from the "keep alive" cathode, so that when a pulse is applied to phase 1, segment 1 will ignite.

However, segments 4 and 7 will not ignite, even though they are connected to phase 1, because segments 2, 3, 5, and 6 have not been ignited and, hence, there has been no transfer of charged particles to segments 4 and 7. The pulse is then applied successively to phases 2 and 3, so igniting segments 2 and 3.

The pulse is repeated now across phases 1, 2, and 3 which first ignited segments 4, 5, and 6, then finally segments 7, 8, and 9. This is the application of the "glow transfer" principle discussed previously.

In practice, the pulses are applied to the phase connections by rotating a counter which is synchronized to a clock. If the clock speed is too slow, the person viewing the display will see the segments going on and off alternately. However, if the clock speed is maintained above a certain minimum frequency (typically, 70Hz) then a "flicker-free" display will be obtained.

APPLICATIONS

Bargraphs can be used for displays in many applications. A few examples are:

1. Process control
2. Automobiles
3. Panel meters
4. Depth indicators
5. Aircraft cockpit displays
6. Level indicators
7. Analog indicators

The bargraph display does not have the mechanical hysterisis of a standard meter movement and therefore has a much faster response. If required, the response can be slowed by filtering the input signals. The hysterisis thus becomes an option of the designer without restrictions of the mechanical meter movement.

They are not as delicate as mechanical meters and have the added advantage of maintaining accuracy in any viewing position (i.e. not affected by gravity, acceleration, jarring, etc). These features make this type display attractive for portable equipment. The 250V supply presents only a minor problem due to the size, price and availability of 12 to 250V converters currently available. Because the display appears as a continuous bar of light, slowly varying signal inputs are easier to interpret than a digital display.

NE580 BARGRAPH CONVERTER

The block diagram of the NE580 and the timing diagram are shown in Figures 5-55 and 5-56.

PHASE CONNECTIONS FOR A SIMPLE 9-SEGMENT, 3-PHASE BARGRAPH

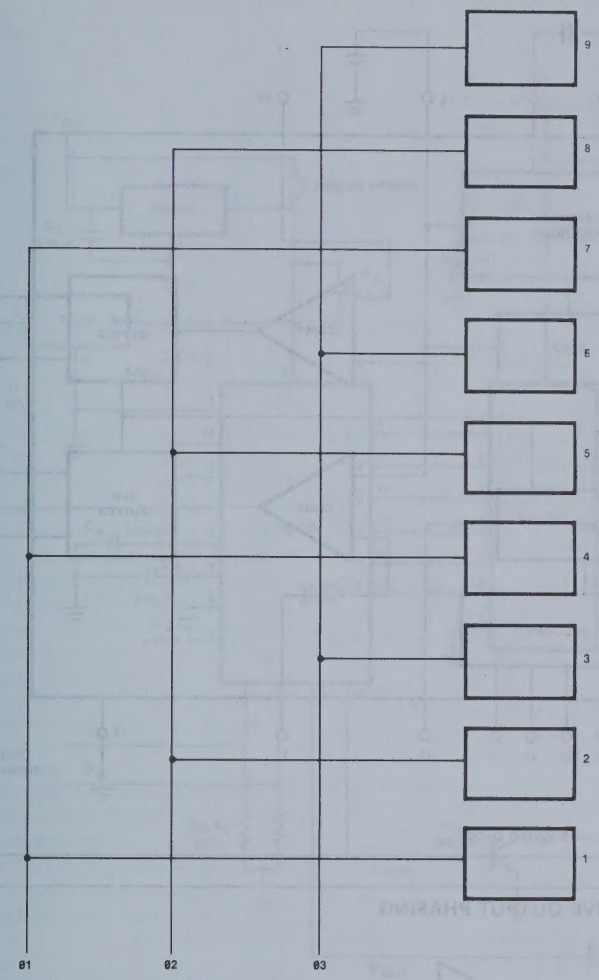


Figure 5-54

The internal clock drives a counter and ramp generator and the frequency of the clock is set with a single external capacitor. The counter addresses a ROM which is used to control the phase decoder. The phase decoder generates the required cathode pulses. A single external pin (pin 3) sets the phase decoder for 5 phase (pin 3 Low) or 6 phase (pin 3 High) operation. An external hold capacitor and an external ramp capacitor are the only other external component requirements of the NE580.

The clock also gates a constant current source to charge the ramp capacitor with a staircase waveform of equal increment steps. Each step corresponds to a cathode phase pulse. There are two steps per segment so the comparison of the analog input voltage (s) with respect to the ramp is made at the mid point of each segment.

The counter inhibits the current source and discharges the ramp after 200 cathode counts.

The ramp current is controlled by the voltage at the V_{REF} input.

The anode voltage to the display is on for a portion of the time that corresponds to the input voltage as described by the equation:

$$V_{IN} = V_{REF} \times \frac{T_{AN}}{\#\text{ (Elements)}} \qquad (5\text{-}7)$$

where T_{AN} is the number of cathode phases for which the anode is on.

Thus for a 200 element device:

$$V_{IN} = V_{REF} \times \frac{T_A}{200} \qquad (5\text{-}8)$$

The NE580 is not a high voltage device; therefore external high voltage drivers are used. Figure 5-57 shows a complete circuit required for driving a Burroughs 5 phase 200 element Bargraph (BG12205-2).

The NE580 requires a 5 volt logic level supply. The 78HV05 provides the regulated 5 volts. A jumper option is provided for use if 5 volts is already available. IC_2 is a 3 terminal 2.5V regulator (78L02) used to provide a stable reference signal to the NE580. The reference signal level can be adjusted by R_1.

Capacitor C_4 (pin 4 of the NE580) is a timing set capacitor. This sets the internal clock frequency of the NE580 and determines the cathode pulse width. The frequency of the internal oscillator of the NE580 can be approximated by the following equation:

$$f(KHZ) = \frac{.555}{C(\mu Fd)}$$

Where F is the Frequency (in KHZ) and C is the timing capacitor (in μFd), each cathode pulse width is equivalent to 2 clock periods.

To generate the 70μsec cathode pulses required by the bargraph, a capacitor value of .019μFd. should be used. Using a standard .022μF capacitor will set the clock frequency to = 25 KHZ. There are 200 phase outputs or 400 clock pulses per frame. The frame frequency is then $\frac{F(clock)}{400}$ or 62.5 frames/sec.

This is well above the eye flicker rate.

Capacitor C_5 is the ramp control element. The constant current source in the ramp generator circuit of the NE580 is dependent on the operating frequency. At 25KHZ, the current is typically 80μA. C_5 should be as large as possible to minimize the effects of leakage. A typical valve for the ramp control element is .47μFd. A Mylar or other low leakage type capacitor should be used.

Capacitor C_6 is a sample and hold element required by the NE580. This should also be a low leakage type capacitor. Grounding pin 3 of the NE580 programs the internal phase decoder for a 5 phase output.

The analog input voltages at Ain and Bin can have an input range of 0 volts to V_{REF} (maximum voltage range is -0.3V to +7 volts).

BLOCK DIAGRAM

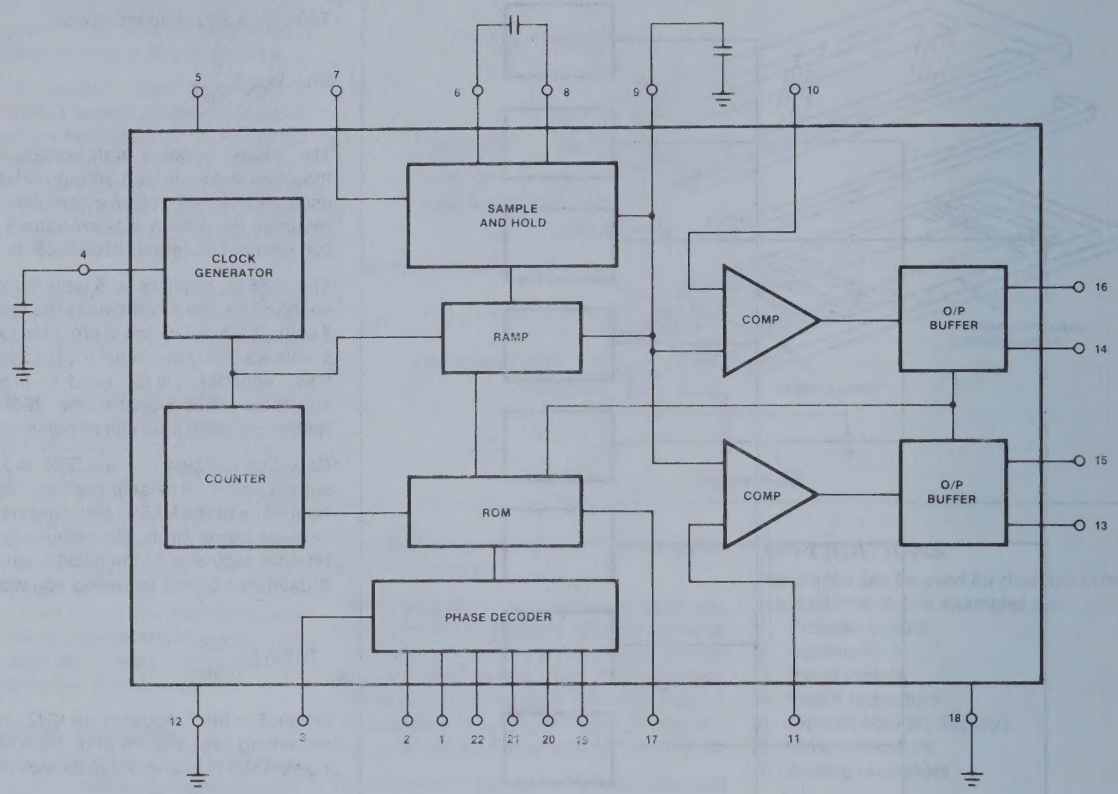


Figure 5-55

RELATIVE OUTPUT PHASING

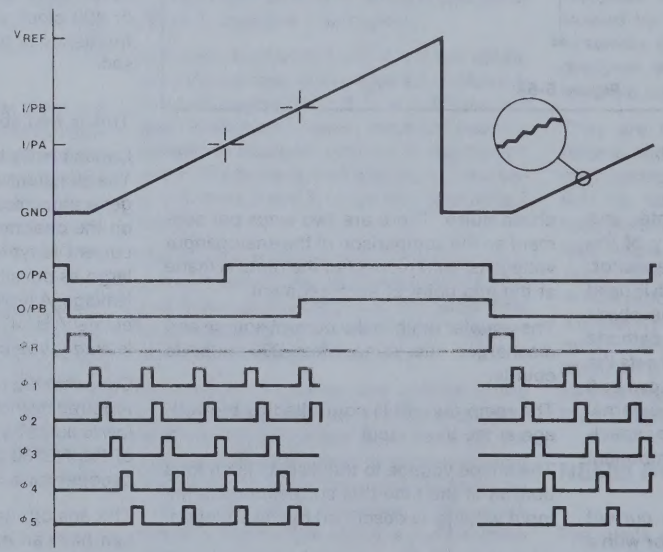


Figure 5-56

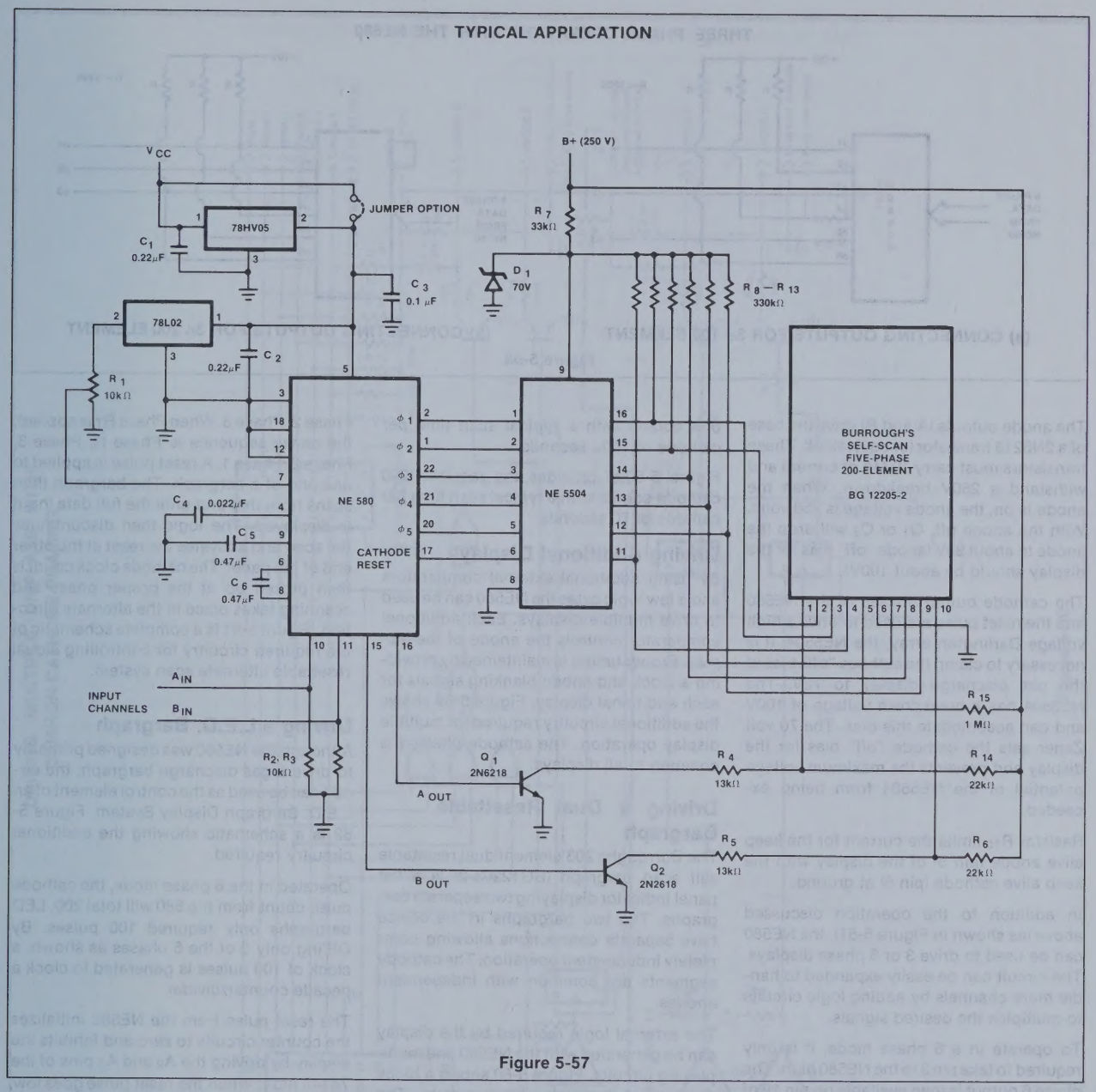

TYPICAL APPLICATION
V CC
78HV05
JUMPER OPTION
C 1 0.22μF
C 3 0.1 μF
78L02
C 2 0.22μF
R 1 10kΩ
B+ (250 V)
R 7 33kΩ
D 1 70V
R 8 – R 13 330kΩ
NE 580
NE 5504
CATHODE RESET
BURROUGH'S SELF-SCAN FIVE-PHASE 200-ELEMENT
BG 12205-2
C 4 0.022μF
C 5 0.47μF
C 6 0.47μF
INPUT CHANNELS
A IN
B IN
R2, R3 10kΩ
Q 1 2N6218
A OUT
R 4 13kΩ
R 14 22kΩ
R 15 1 MΩ
R 5 13kΩ
R 6 22kΩ
Q2 2N2618
B OUT

Figure 5-57

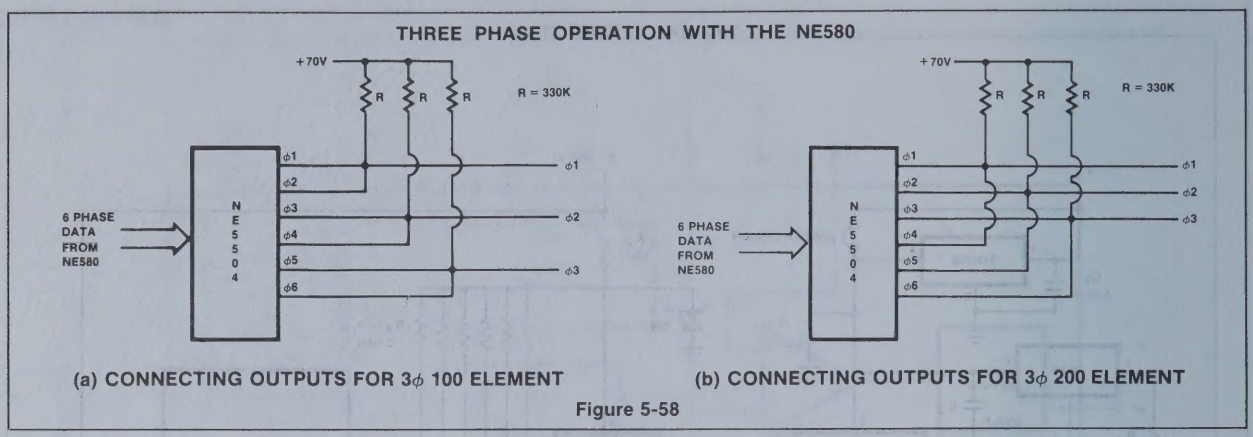


Figure 5-58

The anode outputs (A and B) drive the base of a 2N6218 transistor (or equivalent). These transistors must carry 10 MA of current and withstand a 250V breakdown. When the anode is on, the anode voltage is 250 volts. With the anode off, Q_1 or Q_2 will drop the anode to about 95V (anode "off" bias for the display should be about 100V).

The cathode output phases of the NE580 and the reset pulse are used to drive a high voltage Darlington array, the NE5504. It is necessary to clamp the cathode "off" bias of the gas discharge display to 72V. The NE5504 has a breakdown voltage of 100V and can accomodate this bias. The 70 volt Zener sets the cathode "off" bias for the display and prevents the maximum voltage potential of the NE5504 from being exceeded.

Resistor R_{15} limits the current for the keep alive anode (pin 5) of the display with the keep alive cathode (pin 6) at ground.

In addition to the operation discussed above (as shown in Figure 5-57), the NE580 can be used to drive 3 or 6 phase displays. The circuit can be easily expanded to handle more channels by adding logic circuits to multiplex the desired signals.

To operate in a 6 phase mode, it is only required to take pin 3 to the NE580 high. The phase 6 output is then available on pin 19 of the NE580.

Driving 3 Phase Displays

3 phase gas discharge displays are available as 100 or 200 element indicators (providing 1% or 0.5% resolution respectively).

The NE580 is operated as a 6 phase display driver (Pin 3 tied High) and the high voltage drive circuit is rewired to provide the proper phase outputs. Figure 5-58(a) shows the wiring scheme for a 100 element 3 phase display and provides the required 100 cathode counts with a typical scan time per cathode of 140μ seconds.

Figure 5-59(b) provides the required 200 cathode counts with a typical scan time per cathode of 70 seconds.

Driving Additional Displays

By using additional external comparators and a few logic gates the NE580 can be used to drive multiple displays. Each additional comparator controls the anode of the display. Proper timing is maintained by providing a clock and anode blanking signals for each additional display. Figure 5-59 shows the additional circuitry required for multiple display operation. The cathode phasing is common to all displays.

Driving a Dual Resettable Bargraph

The Burroughs 203 element dual resettable self scan bargraph (BG12203-2) is a flat panel indicator displaying two separate bargraphs. The two bargraphs in the device have separate connections allowing completely independent operation. The cathode segments are common with independent anodes.

The external logic required by the display can be generated with the NE580 and multiplexing circuits. Figure 5-60 shows a block diagram of the logic drive system. The NE580 has anode controls for 2 inputs and associated logic to generate the phase data to drive the display. External comparators are used to compare the additional analog input signals with the NE580 generated ramp. The anode output signals are multiplexed in sync with the appropriate cathode pulses.

The logic circuit must generate 2 reset pulses (R_T and R_B) and 201 clock pulses in a 3-phase arrangement. With phase R_B applied the phase sequence is Phase R, Phase 1, Phase 2, Phase 3. When Phase R_T is applied, the phase sequence is Phase R, Phase 3, Phase 2, Phase 1. A reset pulse is applied to one end of a bargraph. The bargraph then scans from that end until the full data input is displayed. The logic then discontinues the scan and activates the reset at the other end of the panel. The cathode clock count is then picked up at the proper phase and scanning takes place in the alternate direction. Figure 5-61 is a complete schematic of the required circuitry for controlling a dual resettable alternate scan system.

Driving a L.E.D. Bargraph

Although the NE580 was designed primarily to drive a gas discharge bargraph, the circuit can be used as the control element of an L.E.D. Bargraph Display System. Figure 5-62 is a schematic showing the additional circuitry required.

Operated in the 6 phase mode, the cathode pulse count from the 580 will total 200. LED bargraphs only required 100 pulses. By OR'ing only 3 of the 6 phases as shown, a clock of 100 pulses is generated to clock a decade counter/divider.

The reset pulse from the NE580 initializes the counter circuits to zero and inhibits the display by driving the A_2 and A_3 pins of the 74145 high. When the reset pulse goes low, the BCD/Decade decoder will enable cathode A of the Bargraph. The clock pulses will step the counter through illuminating each anode of the bargraph sequentially until the counter reaches ten. The counter will then output a carry incrementing the ripple counter (74LS93) and the Decade/Decoder will enable the next cathode group of the display. During this sequence, the A out signal of the NE580 is low and will remain low until the NE580 ramp voltage exceeds the analog input voltage. When this occurs, the A out goes high and inhibits all outputs

DRIVING MULTIPLE DISPLAYS WITH COMMON CATHODE PHASING

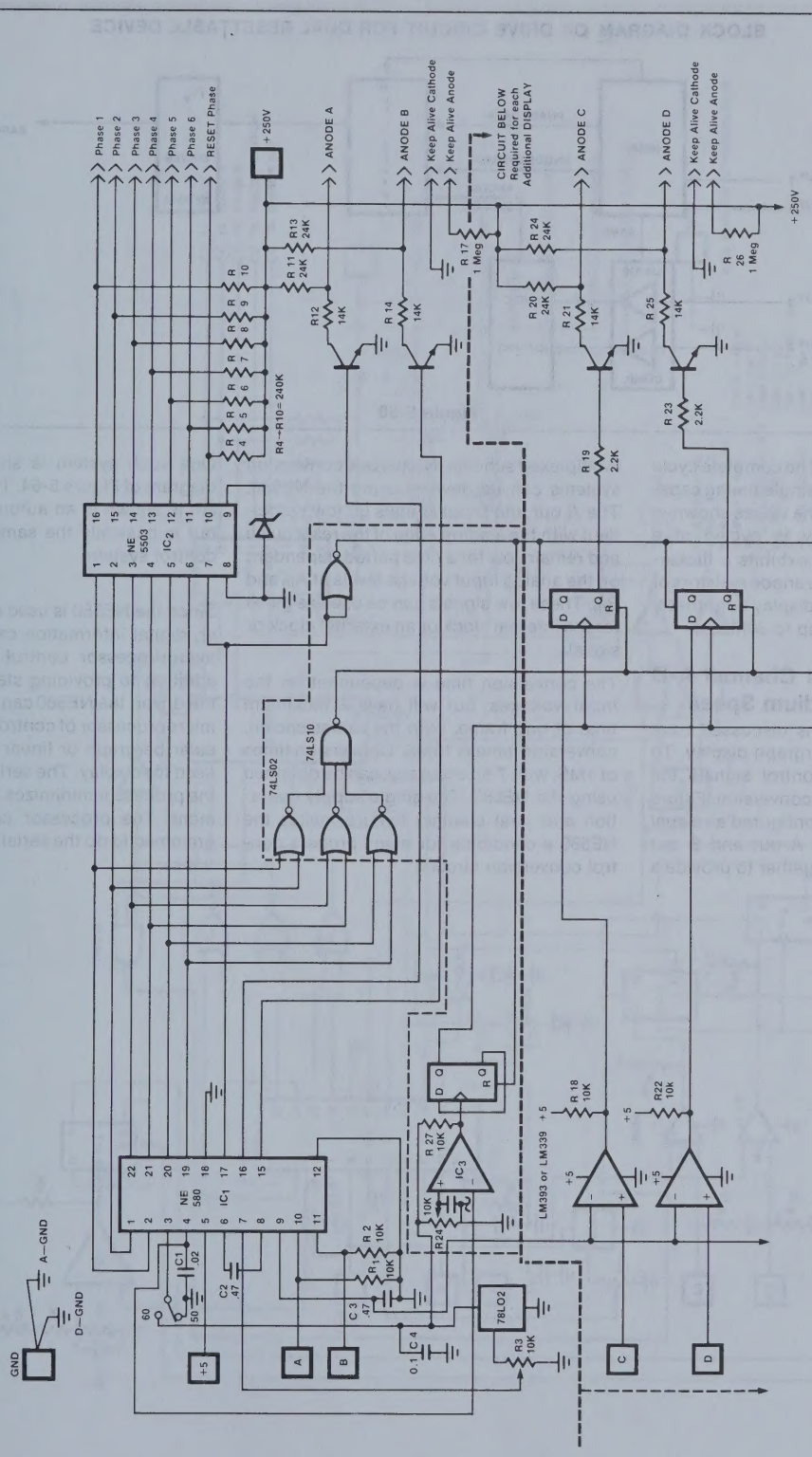


Figure 5-59

BLOCK DIAGRAM OF DRIVE CIRCUIT FOR DUAL RESETTABLE DEVICE

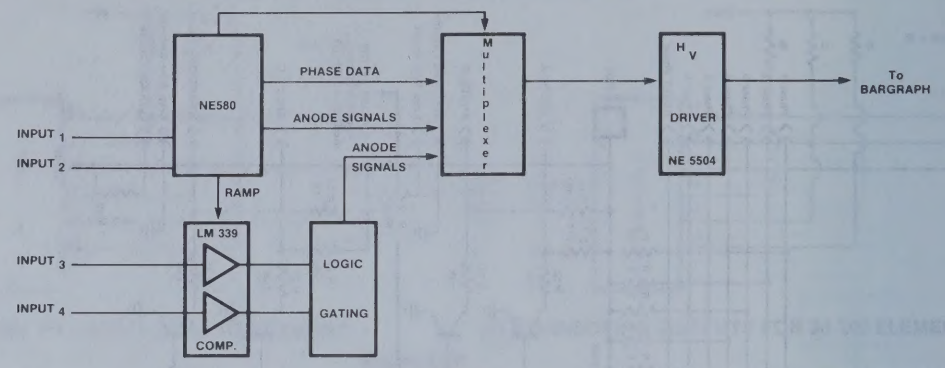


Figure 5-60

of the Decade Decoder. The complete cycle time is controlled by the single timing capacitor x the NE580. With the values shown in Figure 5-62 the display is cycled at a 70Hz and the Bargraph exhibits a flicker-free column of lights. The anode resistors of the bargraph control the display brightness. The 74145 can provide up to 80MA.

Single Supply Dual Channel A-D Converter With Medium Speed

Thus far, all applications discussed have been used to drive a bargraph display. To generate the display control signals the NE580 had to do an A-D conversion. Figure 5-63 shows the NE580 configured as a dual channel A/D converter. A out and B out signals can be OR'ed together to provide a multiplexed scheme. Numerous conversion systems can be devised using the NE580. The A out and B out signals go low coincident with the leading edge of the reset pulse and remain low for a time period dependent on the analog input voltage levels at A_{in} and B_{in}. These low signals can be used as gates for the internal clock or an external clock or signal.

The conversion time is dependent on the input voltages, but will have a maximum time of one frame. With the values shown, conversion time is 16MS. Conversion times of 1MS, with 7 bit accuracy, can be obtained using the NE580. The single supply operation and dual channel feature makes the NE580 a candidate for many process control conversion circuits.

One such system is shown in the block diagram of Figure 5-64. This particular system is shown in an automotive application, but is basically the same for any process control system.

Since the NE580 is used as an A/D converter, digital information can be gated into a microprocessor control system. Thus, in addition to providing status indications to the driver, the NE580 can provide inputs to a microprocessor of control applications. Circular bargraph or linear bargraphs can be used for display. The serial output format to the processor minimizes the wiring requirement. The processor can easily be programmed to do the serial to parallel conversions.

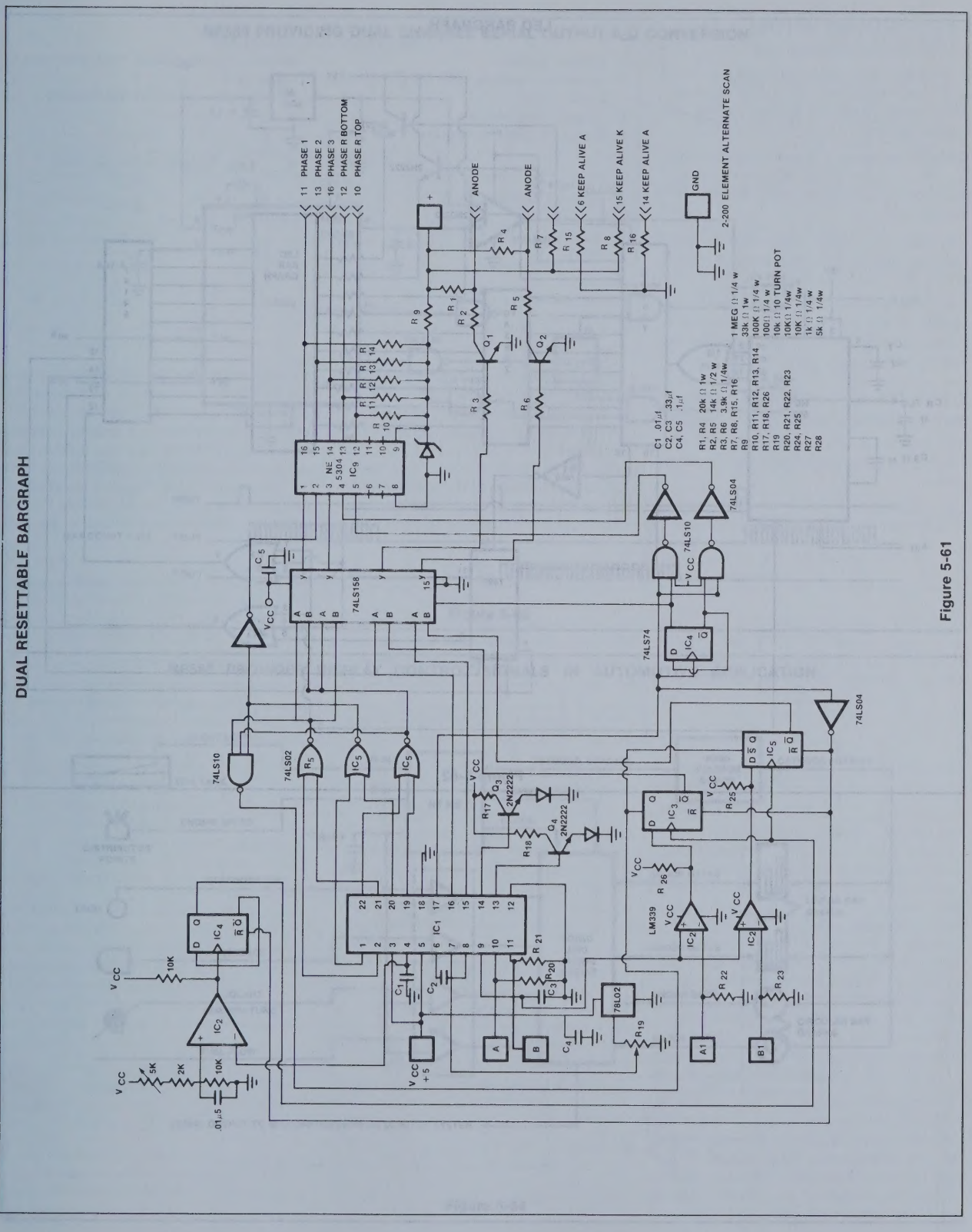

DUAL RESETTABLE BARGRAPH
11 PHASE 1
13 PHASE 2
16 PHASE 3
12 PHASE R BOTTOM
10 PHASE R TOP
ANODE
ANODE
6 KEEP ALIVE A
15 KEEP ALIVE K
14 KEEP ALIVE A
GND
2-200 ELEMENT ALTERNATE SCAN
1 MEG Ω 1/4 w
33k Ω 1w
100K Ω 1/4 w
100Ω 1/4 w
10k Ω 10 TURN POT
10KΩ 1/4w
10K Ω 1/4w
1k Ω 1/4 w
5k Ω 1/4w
C1 .01μf
C2, C3 .33μf
C4, C5 .1μf
R1, R4 20k Ω 1w
R2, R5 14k Ω 1/2 w
R3, R6 3.9k Ω 1/4w
R7, R8, R15, R16
R9
R10, R11, R12, R13, R14
R17, R18, R26
R19
R20, R21, R22, R23
R24, R25
R27
R28
74LS04
74LS10
74LS74
74LS158
74LS02
74LS04
LM339
78L02
NE 5304
2N2222
2N2222
V CC
+5
A
B
A1
B1

Figure 5-61

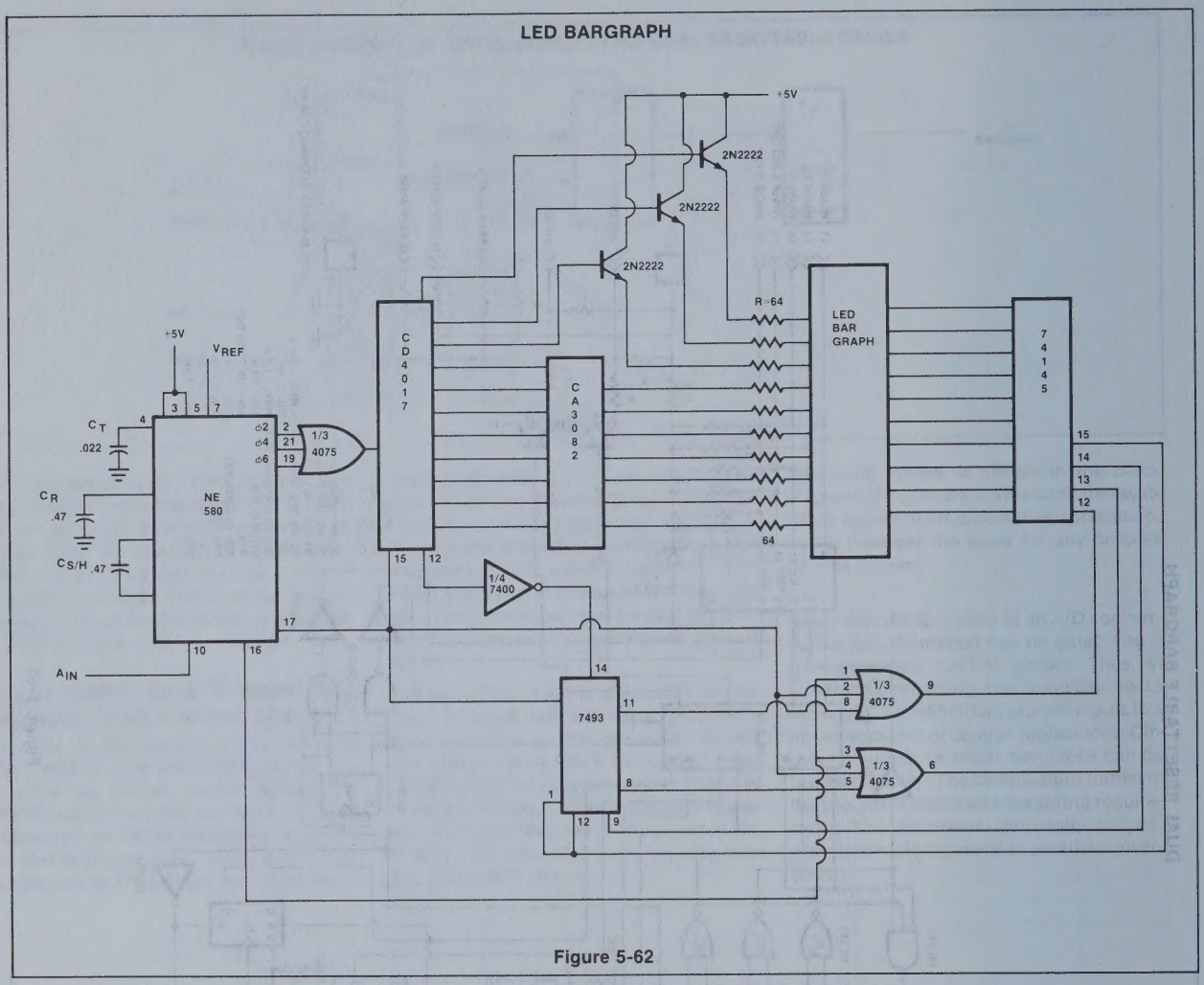

LED BARGRAPH
+5V
2N2222
2N2222
2N2222
R=64
LED
BAR
GRAPH
CD4017
CA3082
7415
+5V
VREF
CT
.022
CR
.47
CS/H .47
NE
580
1/3
4075
1/4
7400
7493
1/3
4075
1/3
4075
AIN
64

Figure 5-62

NE580 PROVIDING DUAL CHANNEL SERIAL OUTPUT A/D CONVERSION

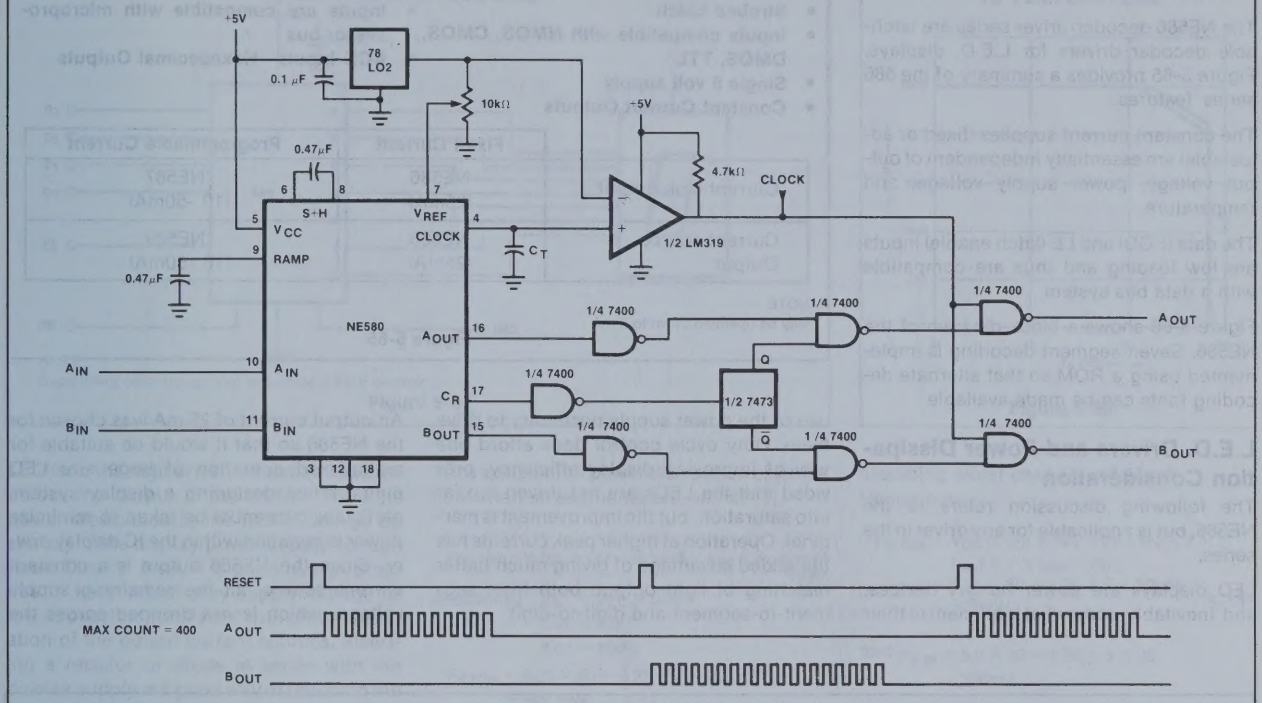


Figure 5-63

NE580 PROVIDES DISPLAY CONTROL SIGNALS IN AUTOMOTIVE APPLICATION

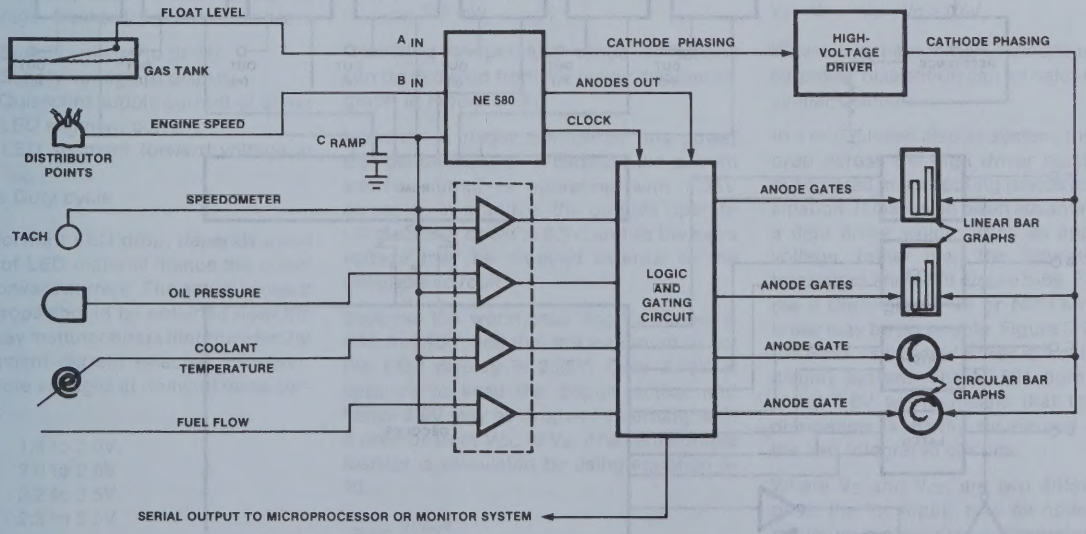


Figure 5-64

LED DECODER DRIVER

NE586/587/588/589

The NE586 decoder/driver series are latchable decoder drivers for L.E.D. displays. Figure 5-65 provides a summary of the 586 series' features.

The constant current supplies (fixed or adjustable) are essentially independent of output voltage, power supply voltage, and temperature.

The data (BCD) and $\overline{LE}$ (latch enable) inputs are low loading and thus are compatible with a data bus system.

Figure 5-66 shows a block diagram of the NE586. Seven segment decoding is implemented using a ROM so that alternate decoding fonts can be made available.

NE 586/587/588/589 LED DRIVERS

- **Strobed Latch**
- **Inputs compatible with NMOS, CMOS, DMOS, TTL**
- **Single 5 volt supply**
- **Constant Current Outputs**
- **Inputs are compatible with microprocessor bus**
- **BCD Inputs—Hexadecimal Outputs**

	Fixed Current	Programmable Current
Current sink output	NE586 (25mA)	*NE587 (10 -50mA)
Current source Output	NE588 (25mA)	*NE589 (10 -50mA)

NOTE
May be operated down to 5 mA

Figure 5-65

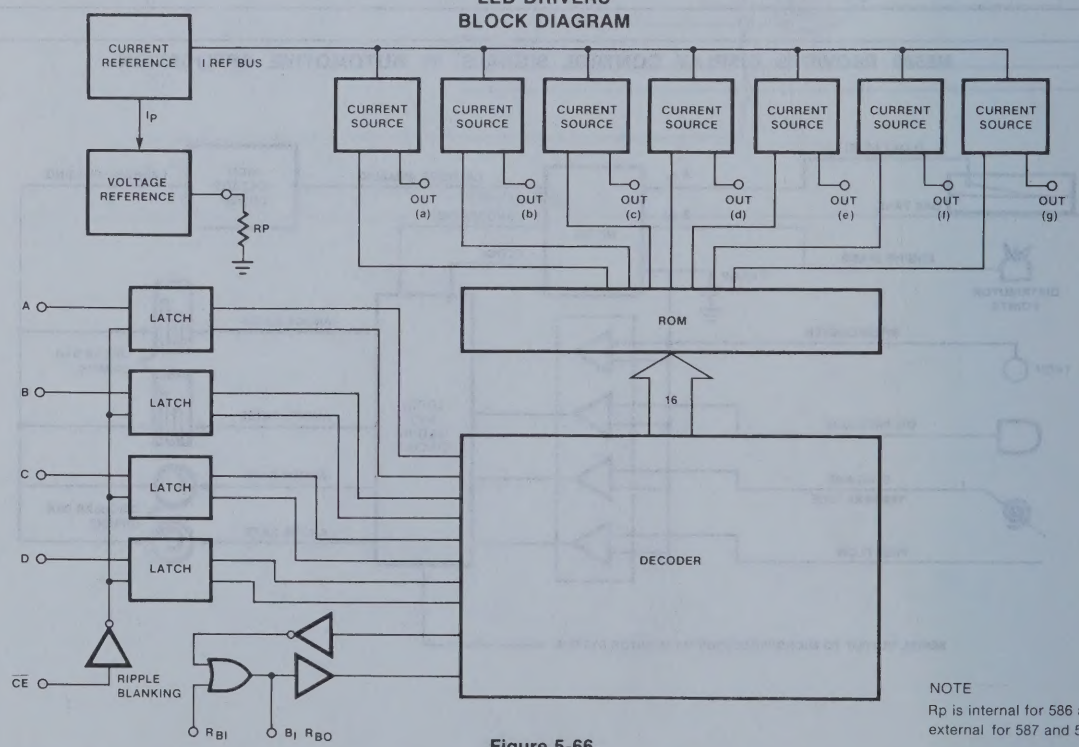
L.E.D. Drivers and Power Dissipation Consideration

The following discussion refers to the NE586, but is applicable for any driver in the series.

LED displays are power hungry devices, and, inevitably, somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

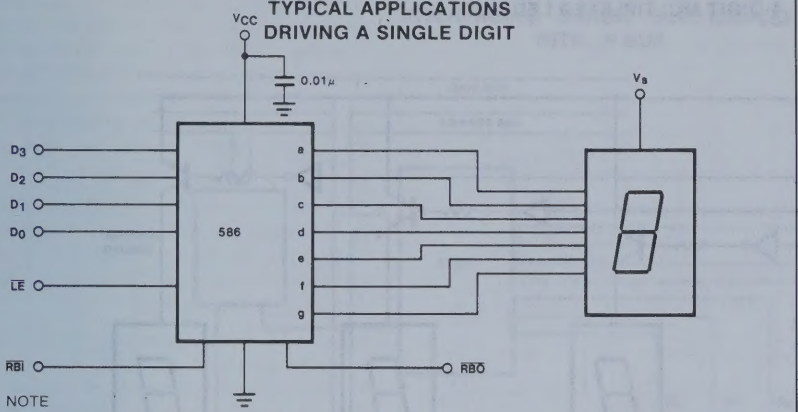
An output current of 25 mA was chosen for the NE586 so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the NE586 output is a constant current source, all the remaining supply voltage, which is not dropped across the

NE 586/587/588/589
LED DRIVERS
BLOCK DIAGRAM



NOTE
Rp is internal for 586 and 588 external for 587 and 589.

Figure 5-66



NOTE
Decoupling capacitor on V_{CC} should be 0.01μF ceramic

Figure 5-67

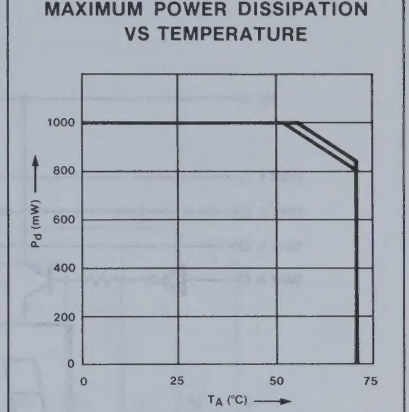


Figure 5-68

LED (and the digit driver, if used) will appear across the output of the NE586. Thus the power dissipation in the NE586 will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation within the NE586 may be calculated as follows. Referring to Figure 5-67, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

- V_{CC}' Supply voltage to driver
- V_S' Supply voltage to display
- I_{CC}' Quiescent supply current of driver
- I_{SEG}' LED segment current
- V_F' LED segment forward voltage at I_{seg}
- K_{DC}'% Duty cycle

V_F', the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturers literature for the peak segment current selected. However, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

These voltages are all for single diode displays. Some early red displays had 2 series LEDs per segment, hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

$$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC} \text{ mW} \quad (5\text{-}9)$$

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$

$$P_{d\,max} = 5.25 \times 50 + 3.25 \times 7 \times 30 \text{ mW}$$
$$= 945 \text{ mW}$$

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{d\,av} = 5.0 \times 30 + 3.00 \times 5 \times 25 \text{ mW}$$
$$= 525 \text{ mW}$$

Operating temperature range limitations can be deduced from the power dissipation graph in Figure 5-68.

However, a major portion of this power dissipation ($P_{d\,max}$) is because the current source output is operating with 3.25V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_F for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by using equation 5-10.

$$R_S = \frac{V_{DROP}}{I_{seg} \times \#\text{ of seg}} \quad (5\text{-}10)$$

or $R_S = \dfrac{2.0}{7 \times I_{seg}} \simeq 10\Omega$ (1/2 W rating)

assuming worst case I_{seg} of 30mA
Hence now:

$$P_{d\,max} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times I_{seg} \times K_{DC}$$
$$= 5.25 \times 50 + 1.25 \times 7 \times 30\text{mW}$$
$$= 525\text{mW} \quad (5\text{-}11)$$

and $P_{d\,av} = 5.0 \times 30 + 1.25 \times 5 \times 25$
$= 306\text{mW}$

If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$V_S - V_F - nV_d$, $V_D \simeq 0.8V$

Where n is the number of diodes used, and so power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in Figure 5-69. For example a Darlington PNP or NPN emitter follower may be preferable. Figure 5-70 shows the N591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the

4-DIGIT MULTIPLEXED LED DISPLAY

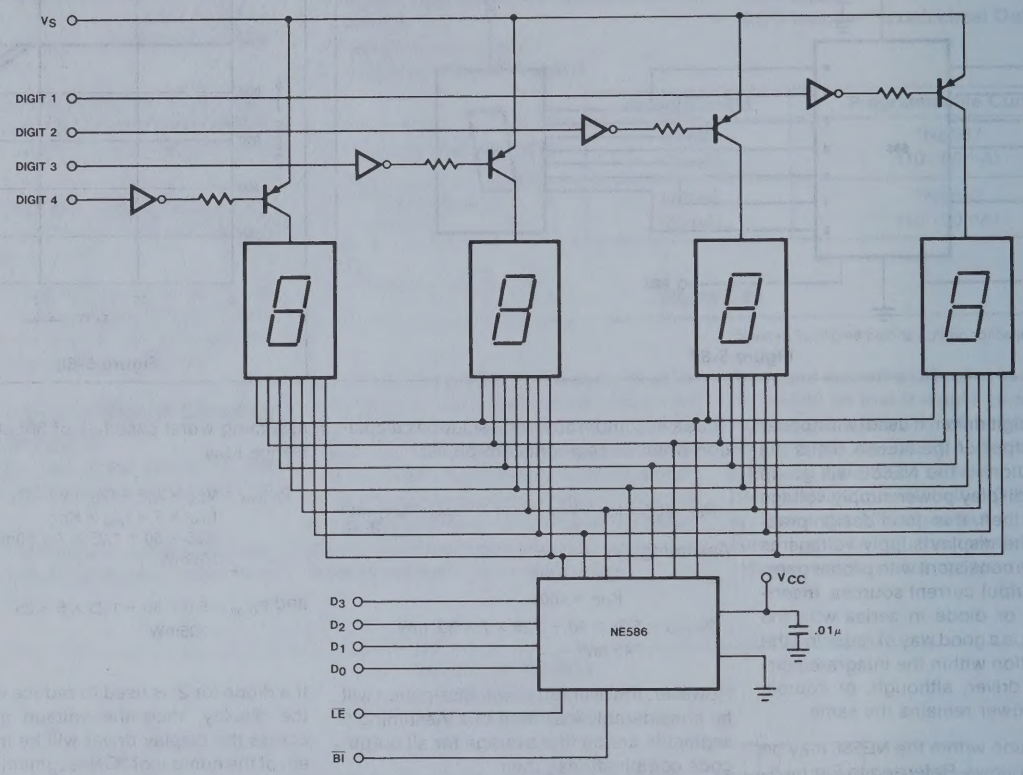


Figure 5-69

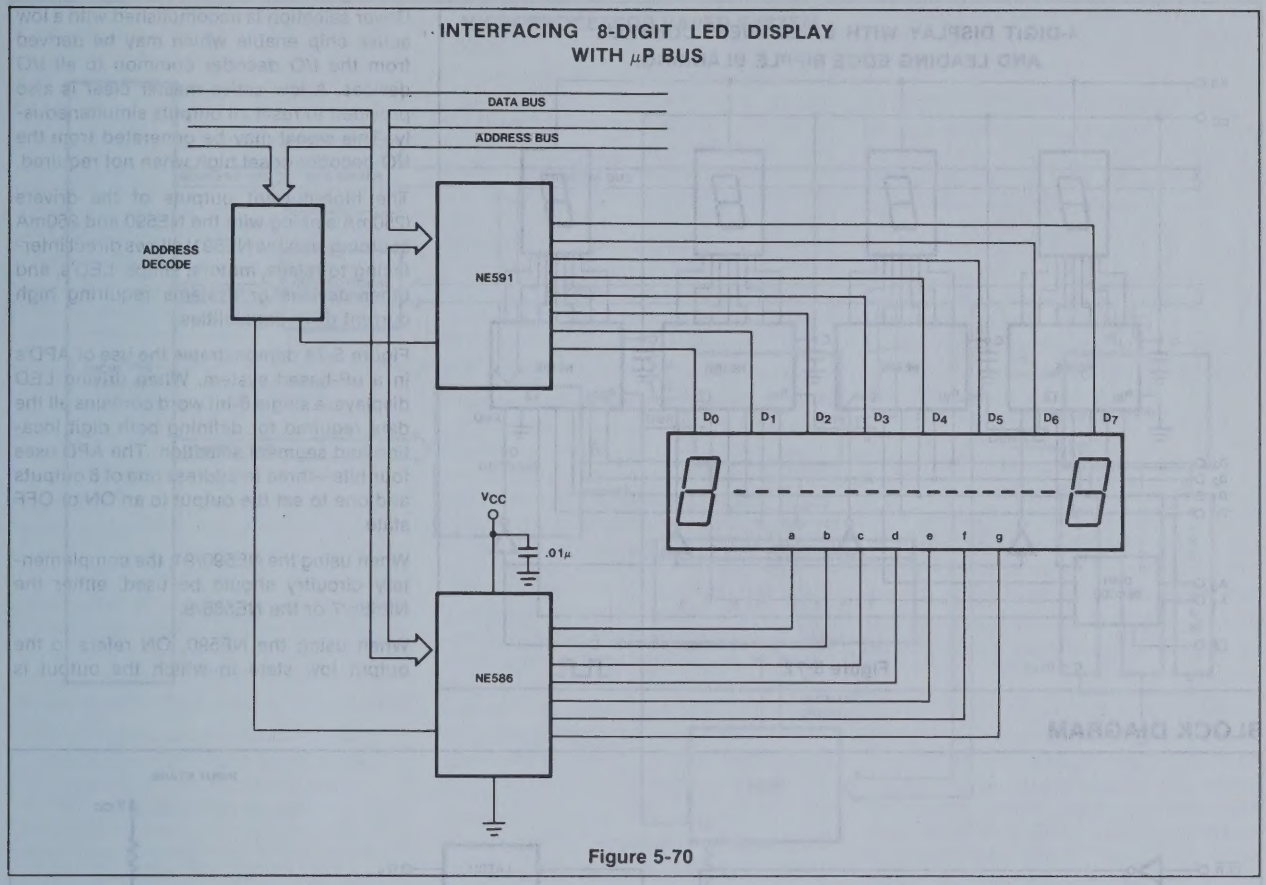


Figure 5-70

system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4. 5V rms works well in most LED display systems. Waveforms are shown in Figure 5-71.

The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With

$V_S = 4.9V$ pk.
$V_F = 2.0V$

The duty cycle is approximately 60%.

V_S in this example was derived by the circuit shown in Figure 5-71. Remember that the forward voltage drop of the rectifying diode must be subtracted to arrive at the exact peakof the V_S voltage.

Figure 5-72 shows other typical application schemes for multiplexing LED displays.

ADDRESSABLE PERIPHERAL DRIVERS SUPPORT μP-BASED SYSTEMS

The Signetics NE590 and NE591 addressable peripheral drivers (APDs) greatly facilitate interfacing a variety of support circuits to microprocessor based systems.

The APDs are designed to eliminate the need for many of the buffers, latches, TTL ICs, and discrete transistors currently needed to drive peripheral devices.

Figure 5-73 shows that each driver includes a set of input latches, a 1-of-8 demultiplexer, and a set of high current drive outputs together with the assorted chip enable and clear logic.

The low loading inputs of these drivers (typically $I_{IL} = 15\mu A$ and $I_{IH} = 1\mu A$) allow direct interfacing to the μP-bus. Eight addressable latches, which are addressed by a three bit binary code and (set/reset) by a single binary bit, allow storage of each output condition (ON/OFF), allowing the μP to continue processing after the APD has been addressed.

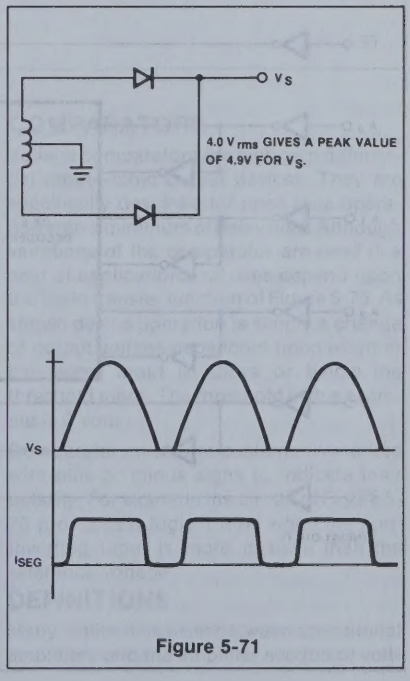


Figure 5-71

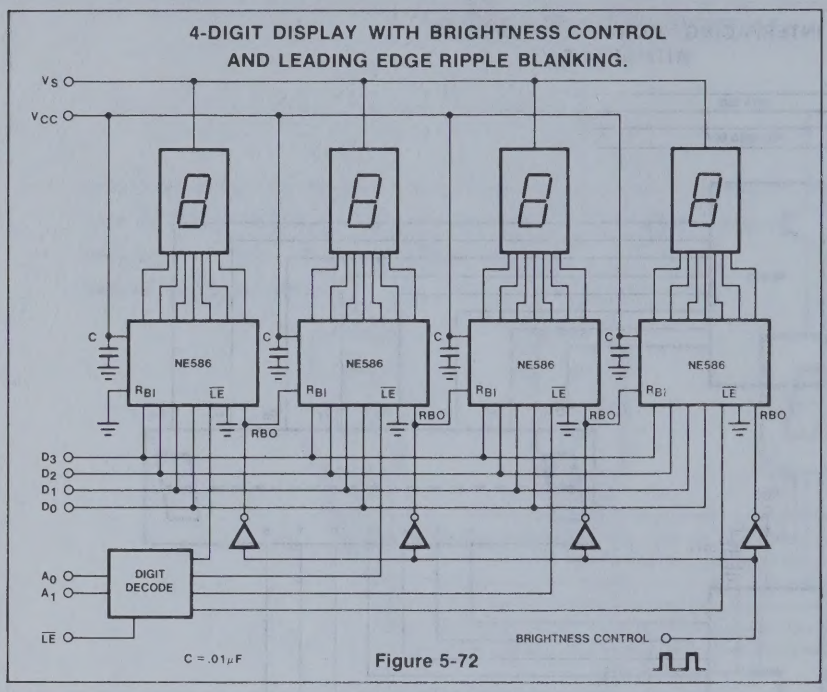


Figure 5-72

Driver selection is accomplished with a low active chip enable which may be derived from the I/O decoder common to all I/O devices. A low active master clear is also provided to reset all outputs simultaneously. This signal may be generated from the I/O decoder or set high when not required.

The high-current outputs of the drivers (250mA sinking with the NE590 and 250mA sourcing with the NE591) allows direct interfacing to relays, motors, lamps, LED's, and other devices or systems requiring high current drive capabilities.

Figure 5-74 demonstrates the use of APD's in a uP-based system. When driving LED displays, a single 8-bit word contains all the data required for defining both digit location and segment selection. The APD uses four bits—three to address one of 8 outputs and one to set the output to an ON or OFF state.

When using the NE590/91, the complementary circuitry should be used, either the NE586/7 or the NE588/9.

When using the NE590, ON refers to the output low state in which the output is

BLOCK DIAGRAM

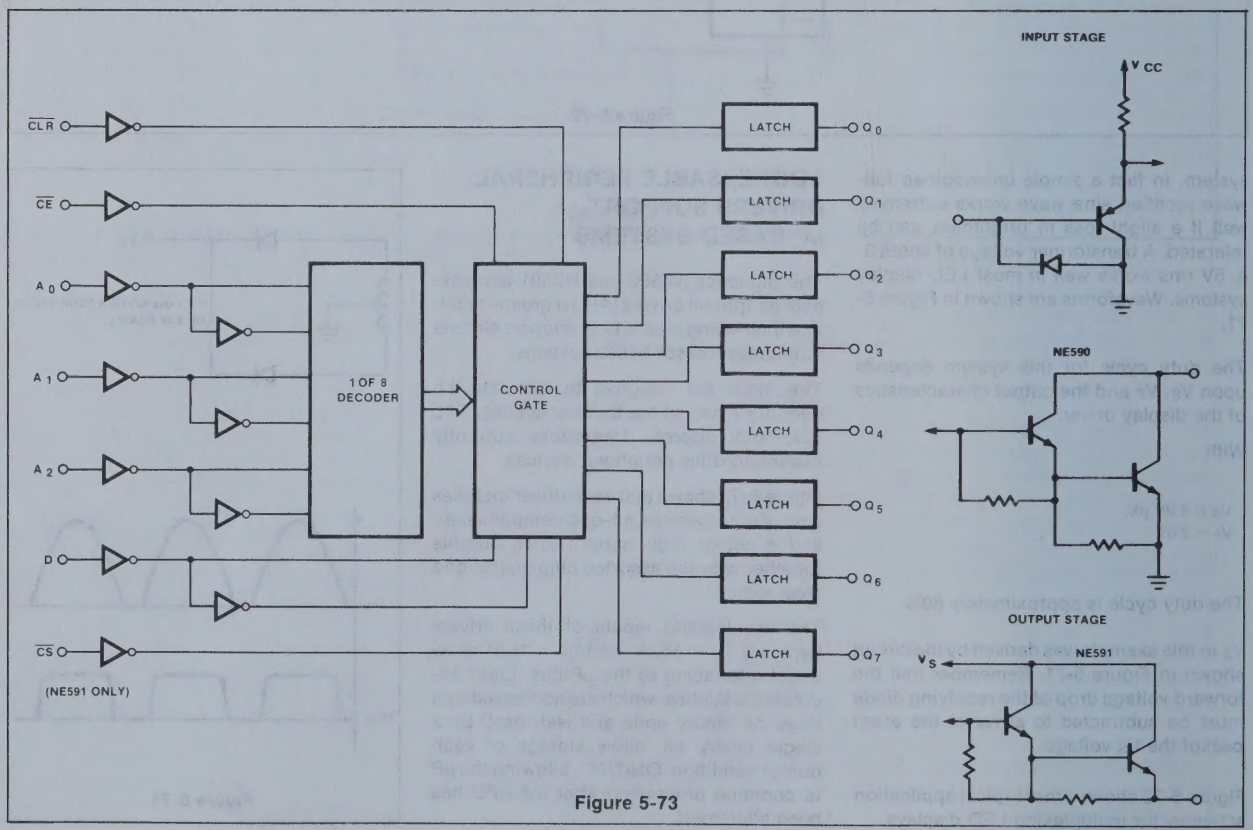


Figure 5-73

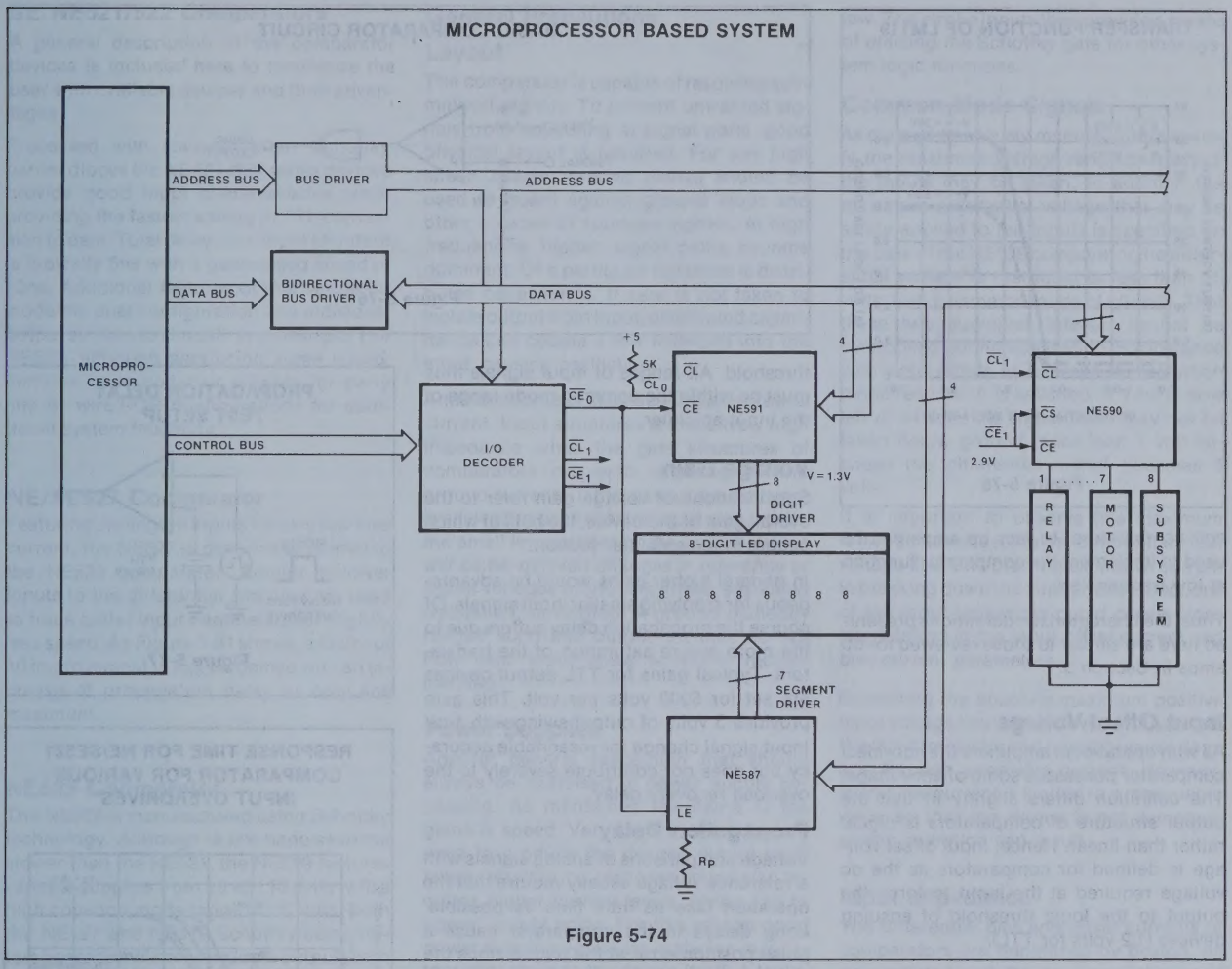


Figure 5-74

capable of sinking a maximum of 250mA. The clear ($\overline{CL}$) pin may be tied high and would normally not be required in this application.

The four remaining data bits are required by the NE589 which supplies segment data. These four BCD data bits are converted into seven-segment data used for driving the anodes of the LED's. Data is strobed into the latches by the LATCH ENABLE INPUT at the same time that information is being supplied to the NE590. Since the NE589 provides a constant current source, uniform brightness is obtained from each segment in the display. The NE589 is capable of supplying up to 50 mA/segment. Segment currents are set by a single programming resistor.

Figure 5-74 shows several devices connected to the NE591: a relay, a motor, and a D-C subsystem. Each device is selected in the same manner as the LED digits; that is, three bits are used to select the output and one bit is used to turn the output ON or OFF.

An output may be cleared in one of two ways:

1) By direct selection and clearing of the individual latch,
   or
2) By clearing all outputs through the use of the clear input.

The latter method does not require addressing.

The examples shown in Figure 5-74 clearly demonstrate the advantages that can be derived from using the NE590 and NE591 APDs in microprocessor-based systems. These devices provide easy interfacing and minimize the number of interfacing components; they also provide the logic interface to the microprocessor and the switch function and high-current drive required by the peripheral units.

COMPARATORS

Voltage comparators are high gain differential input—logic output devices. They are specifically designed for open loop operation with a minimum of delay time. Although variations of the comparator are used in a host of applications, all uses depend upon the basic transfer function of Figure 5-75. As shown device operation is simply a change of output voltage dependent upon whether the signal input is above or below the threshold input. The threshold in this example is 0 volts.

Comparator inputs are customarily marked with plus or minus signs to indicate their polarity. For example the circuit of Figure 5-76 produces a logic 1 level when the non-inverting input is more positive than the reference voltage.

DEFINITIONS

Many similarities exist between operational amplifiers and the amplifier section of volt-

TRANSFER FUNCTION OF LM119

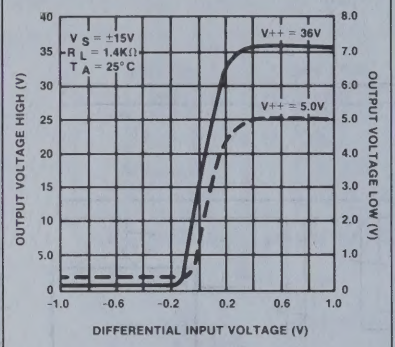


Figure 5-75

age comparators. In fact op amps can be used to implement the comparator function at low frequencies.

Thus, the characteristic definitions presented here are similar to those reviewed for op amps in Section 3.

Input Offset Voltage

As with operational amplifiers the non-ideal comparator possesses some offset voltage. The definition differs slightly in that the output structure of comparators is digital rather than linear. Hence, input offset voltage is defined for comparators as the dc voltage required at the input to force the output to the logic threshold of ensuing devices (1.2 volts for TTL).

Input Offset Current

Imbalances of input bias current arise from small variances of the junction geometry of the differential input amplifier. As for op amps, the imbalance is referred to as input offset current.

Bias Current

As with op amps the input structure of comparators is usually a differential bipolar stage. Hence, the average input current required defines bias current.

Common Mode Range

When specifying voltage comparators one of the key parameters is common mode range, which is defined as the range of voltages over which both inputs can be varied simultaneously without abnormal output voltage transitions. This parameter must be kept uppermost in the designer's mind because the reference and signal voltages become common mode signals at threshold. All ranges of input signals thus must be within the common mode range of the input amplifier.

BASIC COMPARATOR CIRCUIT

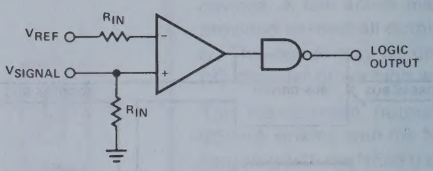


Figure 5-76

Voltage Gain

Specifications of voltage gain refer to the overall gain of the device, the bulk of which occurs in the amplifier section.

In general higher gains would be advantageous for resolving smaller input signals. Of course the propagation delay suffers due to the more severe saturation of the transistors. Typical gains for TTL output devices are set for 5000 volts per volt. This gain provides 5 volts of output swing with 1mV input signal change for reasonable accuracy but does not contribute severely to the overload recovery delay.

Propagation Delay

Voltage comparisons of analog signals with a reference voltage usually require that the operation take as little time as possible. Long delays in the comparator cause a pulse position error at the output since the analog signal in the meantime has changed value. At low frequencies the delay is of small consequence but at higher frequencies, transit time becomes intolerable. Design of voltage comparator devices includes as a prime goal, the minimizing of transit times.

Propagation delay testing is done under worst case conditions. The recovery from saturation varies depending upon the initial state of the amplifier and the overdrive. Worst case conditions begin applying a 100mV signal on the reference terminal. With no signal applied the amplifier is in saturation in one direction. A step input pulse on the signal line of 100mV $\pm$ V_{OS} will bring the amplifier to a threshold level. Propagation delay at this point is undefined since the output has not switched.

To attain output switching a small overdrive is necessary. Propagation delay is tested in a configuration such as Figure 5-77. The input is a step function of 100mV plus a specified excess or overdrive signal. This causes the amplifier to be exercised from saturation in one direction to saturation in the other for worst case propagation delay. Note that larger overdrive improves delay time as can be seen in Figure 5-78. An overdrive of 5mV causes 12ns delay, whereas a 100mV overdrive improves transit time to only 6ns.

PROPAGATION DELAY TEST SETUP

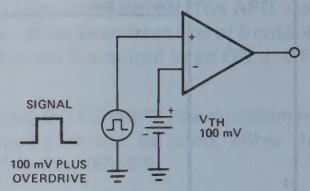


Figure 5-77

RESPONSE TIME FOR NE/SE521 COMPARATOR FOR VARIOUS INPUT OVERDRIVES

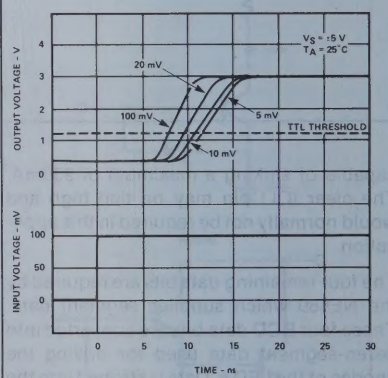


Figure 5-78

SE/NE521/522 Comparators

A general description of the comparator devices is included here to familiarize the user with available devices and their advantages.

Processed with state-of-the-art Schottky barrier diodes the NE 521/522 series devices provide good input characteristics while providing the fastest analog to TTL conversion to date. Total delay from input to output is typically 6ns with a guaranteed speed of 12ns. Additional features of this device include the dual configuration and individual output strobes to simplify system logic. The NE522, although sacrificing some speed, features open collector outputs for party line or wired-OR configurations for additional system flexibility.

NE/SE527 Comparator

Featuring darlington inputs for very low bias current, the NE527 is generically related to the NE529 comparator. Emitter follower inputs to the differential amplifier are used to trade better input parameters for slightly less speed. As Figure 5-81 shows, a factor of 10 improvement in I_{BIAS} is gained with an increase of propagation delay of only 4ns maximum.

NE529 Comparator

The NE529 is manufactured using Schottky technology. Although a few nano seconds slower than the NE521, the NE529 features variable supplies from ±5 to ±10 volts with a high common mode range of ±6 volts. Both the NE527 and NE529 Schottky comparators boast complimentary logic outputs with output A being in phase with input A. In addition the supplies of both the NE527 and NE529 may be non-symmetrical to produce a desired shift in the common mode range.

This technique is illustrated by the ECL to TTL and TTL to ECL translators of Figures 5-91 and 5-92 respectively. The only major requirement of the supplies is that the negative supply be at least 5 volts more negative than the ground terminal of the gate. This is necessary to insure that the internal bias arrangement has sufficient voltage to operate normally.

APPLICATIONS

Today's state-of-the-art ultra-high speed comparators are capable of making logic decisions in less than 10 nano seconds. They are easily applied and possess good input and power supply noise rejection. As with all linear ICs however, some preliminary steps should be taken in their use.

General Precautions

Layout

The comparator is capable of resolving submillivolt signals. To prevent unwanted signals from appearing at signal ports, good physical layout is required. For any high speed design, ground planes should be used to guard against ground loops and other sources of spurious signals. At high frequencies hidden signal paths become dominant. Of a particular nuisance is distributed capacitance. If care is not taken to isolate output from input, distributed capacitance can couple a few millivolts into the input, causing oscillation.

Another source of spurious signal is ground current. Input structures are relatively high impedance while the gate structures of comparators run with large signal and ground currents. If this gate ground current is allowed to pass near the input signal path, the small impedances of the ground circuit will cause millivolt changes in reference or signal voltages producing errors, sustained oscillation, or ringing. A ground plane arranged such that output currents do not flow near input areas is highly recommended.

Power Supplies

Another general precaution that should always be exercised is power supply bypassing. As mentioned the name of the game is speed. Very high speed gates are used to produce the desired output logic levels. Maximizing response speed also requires higher current levels, giving rise to power supply noise. For this reason good power supply by-passing is always mandatory very close to the device itself. A tantalum capacitor of 1 to 10μF in parallel with 500 to 1000pF will prove effective in most cases. Lead lengths should be as short as physically possible to preserve low impedances at high frequency.

Unused Inputs

Some currently available comparators such as the NE521 and NE522 are dual devices. Most often both sections of these devices will be utilized. Should a system utilize one device, the unused inputs should be biased in a known condition. The high gain-bandwidth may otherwise cause oscillations in the unused comparator section. A low impedance should be provided from both unused inputs to ground. A resistor of relatively high impedance may then be used to supply a differential input on the order of 100mV to insure the comparator assumes a known state.

If the inverting input is tied to the positive differential voltage the gate output will be low. The strobe inputs then provide a means of utilizing the Schottky gate for other system logic functions.

Common Mode Signals

As defined previously manufacturers specify the maximum voltage range over which the inputs may be taken. In addition the maximum differential voltage that may be safely applied to the inputs is specified. In the case of the NE529 comparator the differential voltage is restricted to less than ±5 volts, with a common mode of ±6 volts. That these two quantities interact cannot be overlooked during application. For instance with both inputs at ±4 volts the common mode restriction is satisfied. If V ref is now left at +4 volts the signal input may not be taken below ground more than 1 volt because the differential signal becomes 5 volts.

It is important to observe this maximum rating since exceeding the differential input voltage limit and drawing excessive current in breaking down the emitter-base junctions of the input transistors could cause gross degradation in the input offset current and bias current parameters.

Exceeding the absolute maximum positive input voltage limit of the device will saturate the input transistor and possibly cause damage through excessive current. However, even if the current is limited to a reasonable value so that the device is not damaged, erratic operation can result.

Input Impedance

The differential bias and offset currents of comparators are minimized by design. As was pointed out for op amps, the input resistance seen by both inputs should be equal. This reduces to a minimum the contribution of offset current to threshold error. Unbalanced input impedance also adds to the offset error due to the difference in voltage drop across the input resistances.

BASIC APPLICATIONS

The basic comparator circuit and its transfer function were presented by Figures 5-75 and 5-76.

When the input exceeds the reference voltage, the output switches either positive or negative, depending on how the inputs are connected.

The vast majority of specific applications involve only the basic configuration with a change of reference voltage. A to D converters are realized by applying the signal to one terminal and the voltage derived from a ladder network to the other. Limit detectors are likewise made from only the very basic

If the measurement were made without initial saturation (less than 100mV V threshold) the delay time would be smaller, due to the smaller storage times of unsaturated transistors.

STATE-OF-THE-ART

Comparator design has always been optimized for four basic parameters. They are:
1. High Speed
2. Wide Input Voltage Range
3. Low Input Current
4. Good Resolution

Unfortunately these four parameters are not compatible. For instance gain and input current can be improved by using thinner diffusions for higher beta, but only at the expense of input voltage range. Higher gain also means higher saturation for an increase in delay time. So it becomes obvious that comparators such as the 710 were designed with the best compromises in mind using standard processing.

One method of improving overall response adds gold doping to the processing flow. The gold dopant causes a decrease in minority carrier lifetime which aids the recombination process and shortens the saturation recovery time. Unfortunately the transistor beta is adversely affected by gold causing slightly higher bias and offset currents.

It was not until the advent of the Schottky clamp that a vast improvement in speed without input degradation was possible. A very familiar term in the semiconductor industry, the Schottky barrier diode's (SBD) location is illustrated in Figure 5-79.

The Schottky clamped transistor is formed by parallelling the Schottky diode with the base-collector junction of the npn transistor. Without the clamp, as base drive is increased the collector voltage falls until hard saturation occurs. At this point the collector voltage is very near the emitter voltage, and stored charges in the junctions causes slow recovery from saturation after base drive has been removed. The forward voltage drop of the Schottky diode is 0.4 volts—less than the forward drop of silicon diodes. This difference in forward drop is used by placing the diode across the transistor base-collector junction. The Schottky diode becomes forward biased when the collector voltage falls 0.4 volts below the base voltage. Excess base drive is then shunted into the collector circuit prohibiting the transistor from reaching classic saturation. With almost no stored charge in either the SBD or the transistor, there is a large reduction in storage time. Thus, transistor switching time is significantly reduced.

A cross sectional area of the Schottky diode is shown in Figure 5-80.

SCHOTTKY CLAMPED TRANSISTOR

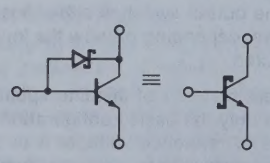


Figure 5-79

SCHOTTKY CLAMPED TRANSISTOR GEOMETRY

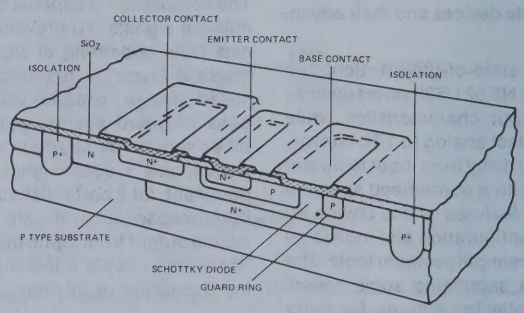


Figure 5-80

COMPARING THE COMPARATORS

Presently available comparator ICs range from the ultra fast SE/NE521 to the general purpose comparator fashioned from an inexpensive op amp. Selection of the device depends upon the application in which it will be used. Often times speed of conversion is of primary importance to minimize pulse position errors of high frequency signals. At other times the parameters are much less stringent allowing the use of a general purpose comparator.

A handy reference guide to the major parameters is summarized in Figure 5-81. At a glance the necessary parameters can be chosen to select the proper device.

COMPARATOR SELECTION GUIDE

Device	Propagation Delay (ns)	Vos (mV)	Ios (μA)	Ibias (μA)	Gain	CMR (V)	Benefits
NE521	12	7.5	5	20	5000	±3	Dual, very fast, standard supplies, TTL compatible, individual & common strobe.
NE522	15	7.5	5	20	5000	±3	Same as NE521 plus open collector outputs for additional decoding.
NE527	26	6	0.75	2	5000	±6	Fast, very low input current, differential outputs, flexible surplus wide common mode range.
NE529	22	6	5	20	5000	±6	Same as NE527 but with faster response.

Figure 5-81

NOTE Parameters are based on min/max limits at 25°C as defined in the individual data sheet.

circuit. Both are only a small deviation from the basic level detector.

Hysteresis

Normally saturated high or low, the amplifiers used in voltage comparators are seldom held in their threshold region.

They possess high gain-bandwidth products and are not compensated to preserve switching speed. Therefore if the compared voltages remain at or near the threshold for long periods of time, the comparator may oscillate or respond to noise pulses. For instance this is a common problem with successive approximation D/A converters where the differential voltage seen by the comparator becomes successively smaller until noise signals cause indecision. To avoid this oscillation in the linear range, hysteresis can be employed from output to input. Figure 5-82 defines the arrangement. Both positive and negative feedback is provided by R_{IN} and R_f.

Hysteresis occurs because a small portion of the "one" level output voltage is fed back in phase and added to the input signal. This feedback aids the signal in crossing the threshold. When the signal returns to the threshold, the positive feedback must be overcome by the signal before switching can occur. The switching process is then assured and oscillations cannot occur. The threshold "dead zone" created by this method, illustrated in Figure 5-83, prevents output chatter with signals having slow and erratic zero crossings.

As shown in Figure 5-82, the voltage feedback is calculated from the expression:

$$V_{HYST} = \frac{E_{OUT} \bullet R_{IN}}{R_{IN} + R_f}$$

LEVEL DETECTOR WITH HYSTERESIS

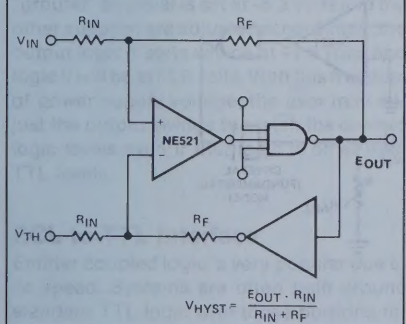


Figure 5-82

0 VOLT LEVEL DETECTOR WITH ± 10mV HYSTERESIS

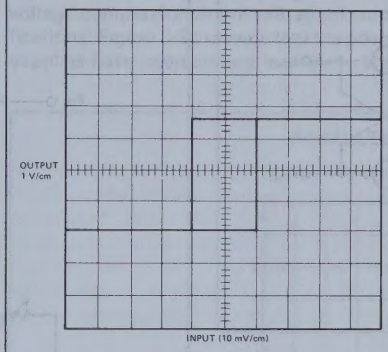


Figure 5-83

where E_{OUT} is the gate output voltage. The hysteresis voltage is bounded by the common mode range and the ability of the gate to source the current required by the feedback network. If symmetrical hysteresis is desired an additional inverting gate is required if the comparator does not have differential outputs. The NE527 and NE529 devices provide inverted signals from differential outputs while the NE521, NE522 and NE526 devices will require the inverter. Care should be taken in the selection of the inverter that propagation delay is minimum especially for very high speed comparators such as the NE521.

Line Receiver

Retrieving signals which have been transmitted over long cables in the presence of high electrical noise is a perfect application for differential comparators. Such systems as automated production lines and large computer systems must transmit high frequency digital signals over long distances.

If the twisted pair of the system is driven differentially from ground, the signals can be reclaimed easily via a differential line receiver.

Since the electrical noise imposed upon a pair of wires takes the form of a common mode signal, the very high common mode rejection of the NE521/522 makes the unit ideal for differential line receivers. Figure 5-84 depicts the simple schematic arrangement. The NE521 is used as a differential amplifier having a logic level output. Because common mode signals are rejected, noise on the cable disappears and only the desired differential signal remains. Figure 5-85 illustrates the NE521 response to the 200mV peak to peak 10MHz differential signal. In Figure 5-86 the same signal has been buried in 5 volts peak to peak of 1 HMz common mode "noise."

As shown the circuit suffers no degradation of signal. If desired several NE522 comparators may be "wire OR'd," or a latch output can be accomplished as shown.

The NE521 and NE529 comparators have the advantage of wider bandwidth to permit higher data rates.

Double Ended Limit Detector

Many system designs require that it be known when a signal level lies between two limits. This function is easily accomplished with a single NE522 package. The schematic and transfer curve of the circuit is shown in Figure 5-87.

Each half of the NE522 is referenced to the desired upper or lower voltage limit producing the desired transfer curve shown. Taking advantage of the dual configuration and the open collectors of the NE522 minimize external components and connections.

Crystal Oscillator

Any device with a reasonable gain can be made to oscillate by applying positive feedback in controlled amounts. The NE521 will lend itself to crystal control easily, provided the crystal is used in its fundamental mode. Figure 5-88 shows a typical oscillator circuit.

The crystal is operated in its series resonant mode, providing the necessary feedback through the capacitor to the input of the NE521. The resistor R_{adj} is used to control the amount of feedback for symmetry. Oscillations will start whenever a circuit disturbance such as turning on the power supplies occurs. The NE521 will oscillate up to 70MHz. However, crystals with frequencies higher than about 20MHz are usually operated in one of their overtones. To build an oscillator for a specific overtone requires tuned circuits in addition to the crystal to provide the necessary mode suppression. If the spurious modes are not tuned out the crystal will oscillate at the fundamental frequency. Higher frequency oscillators could be realized using input and output mode suppression or tuning. The NE522 is especially desirable since the bare collector topology allows the output to be collector tuned readily.

Analog to Digital Converter

There are many types of A to D converter

LINE RECEIVER

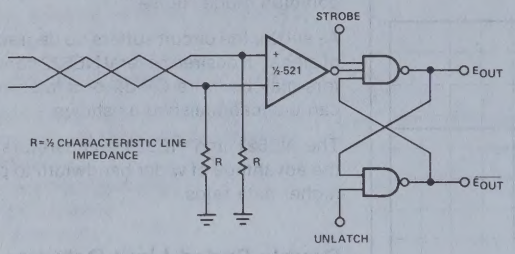


Figure 5-84

LINE RECEIVER RESPONSE

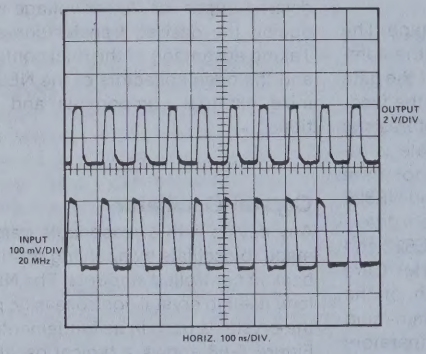
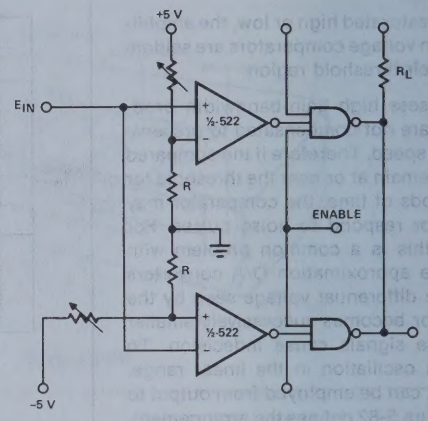


Figure 5-85

DOUBLE ENDED LIMIT DETECTOR



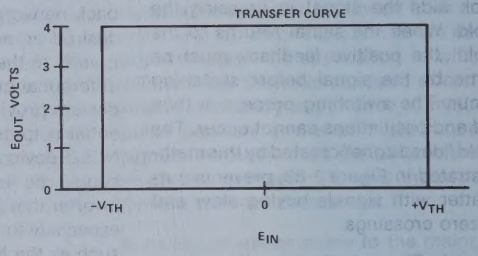


Figure 5-87

RESPONSE DURING COMMON MODE NOISE

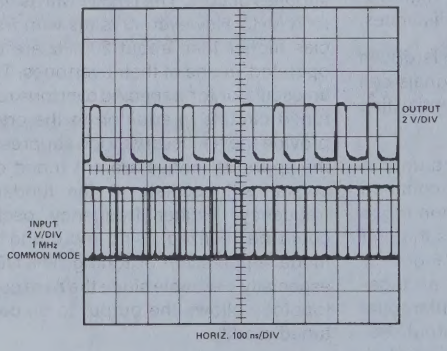


Figure 5-86

CRYSTAL OSCILLATOR

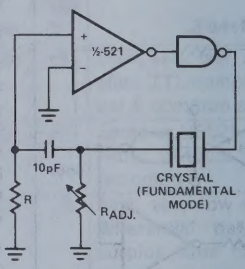


Figure 5-88

designs, each having its own merits. However, where speed of conversion is of prime interest the multi-threshold conversion type is used exclusively. It is apparent from Figure 5-89 that the conversion speed of this design is the sum of the delay through the comparator and the decoding gates.

The sacrifices which must be made to obtain speed are the number of components, bit accuracy and cost. The number of comparators needed for an N-bit converter is 2n-1. Although the NE521 provides two comparators per package, the length of parallel converters is usually limited to less than 4 bits. Accuracy of multi-threshold A-D converters also suffers since the integrity of each bit is dependent upon comparator threshold accuracy.

The implementation of a 3-bit parallel A-D converter is shown in Figure 5-90 with a 3-bit digital equivalent of an analog input shown in Figure 5-89.

Reference voltages for each bit are developed from a precision resistor ladder network. Values of R and 2R are chosen so that the threshold is one half of the least significant bit. This assures maximum accuracy of ±1/2 bit.

It is apparent from the schematic that the individual strobe line and duality features of the NE521 have greatly reduced the cost and complexity of the design. The speed of the converter is graphically illustrated by the photo of Figure 5-89. All 3-bit outputs have settled and are true a mere 15ns after the input step of 3 volts has arrived. The output is usually strobed into a register only after a certain time has elapsed to insure that all data has arrived.

Logic Interface

During the design of the NE527 and NE529 devices, particular attention was paid to the biasing network so that balanced supplies need not be provided. For example, if the "ground" terminal is set at -5.2 volts and the other supplies are adjusted accordingly, the output logic 1 state will be at -1.5 volts and logic 0 will be at -5.0 volts. With this freedom of power supply voltage, the user may adjust the output swings to match the desired logic levels even if that logic is other than TTL levels.

ECL to TTL Interface

Emitter coupled logic is very popular due to its speed. Systems are often built around standard TTL logic with those portions requiring higher speed being implemented with emitter coupled logic. As soon as such a decision is made the problem of interfacing TTL to ECL logic levels is encountered. The standard logic output swings of ECL are -0.8V to -1.8V at room temperatures. Converting these signals to TTL levels is accomplished simply by using the basic voltage comparator circuit with slight modifications. Figure 5-91 reveals that the power supplies have been shifted in order to shift the common mode range more negative. This insures that the common mode range is not exceeded by the logic inputs. Since ECL is extremely fast the NE529 is usually selected because of its superior speed so that a minimum of time is lost in translation.

PARALLEL A-D RESPONSE

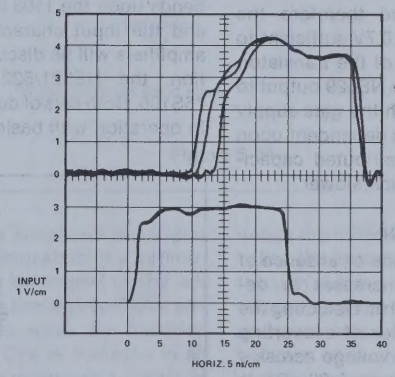


Figure 5-89

3-BIT PARALLEL A-D CONVERTER

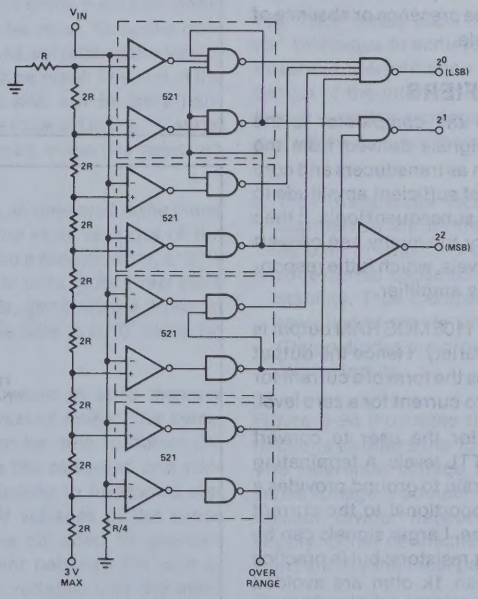


Figure 5-90

TTL to ECL

Operating in the reverse, TTL levels can also be converted to ECL levels by the NE529. Again the NE529 is selected as the fastest converter with the necessary power supply flexibility to accomplish the level shifting with a minimum of effort and cost.

A check of output voltage for the NE529 reveals that the voltage is slightly less than required by the ECL logic for fast switching. R2 and the diode of Figure 5-92 raises the gate supply voltage and therefore the NE529 output voltage by 0.7V sufficient to guarantee fast switching of the translator. Resistive pull up from the NE529 output to V_{CC} can also be used with the gate supply grounded. This method is dependent upon RC time constants of distributed capacitance and is therefore much slower.

Photo Diode Detector

Responding to the presence or absence of light, the photo diode increases or decreases the current through it. Detecting the changes becomes a matter of converting light and dark currents to voltage across a resistor as shown in Figure 5-93. R1 is selected to be large enough to generate detectable differences between light and dark conditions. Once the signal levels are defined by R1 and the diode characteristics, the average between light and dark signals is used for V reference and is produced by the resistive divider consisting of R1 and R2. The comparator then produces an output dependent upon the presence or absence of light upon the diode.

SENSE AMPLIFIERS

Closely related to the comparator is the sense amplifier. Signals derived from the many sources such as transducers and core memories are not of sufficient amplitude to be compatible with subsequent logic. It then becomes necessary to amplify and convert the signal to TTL levels, which is the responsibility of the sense amplifier.

As an example, the 1103 MOS RAM output is of the bare drain variety. Hence the output of the memory takes the form of a current for a one level with zero current for a zero level.

It remains, then, for the user to convert these currents to TTL levels. A terminating resistor from the drain to ground provides a voltage output proportional to the current and the resistor size. Larger signals can be produced by larger resistors; but in practice resistors larger than 1k ohm are avoided because of increasing access time. Distributed capacitance forms a time constant with this output resistance causing slow rise and fall times when the resistor is large, adding to the access time.

Virtually any voltage comparator or sense amplifier can be used. Since total time is the sum of all delays, the sense amplifier is most often the fastest available. Signetics comparators NE521 and NE522 are ideal in this application because of low input offset voltages and very fast response. Using these Schottky clamped comparators significantly reduces the total cycle time of the memory.

Design of the sense amplifier network depends upon the 1103 used (1103 or 1103-1) and the input characteristics. Two sense amplifiers will be discussed in this application, the NE521/522 and the 75S107/75S108. Both sets of devices are very similar in operation with basic differences in input parameters and speed. The significant specifications are given in Table 5-3.

DEVICE	V_{OS} (mV)	I_{B} (μA)	V_{IN} (MIN)(mV)	SPEED (NS) (V_{IN}=100mV)	GAIN
521	10	40	15	12	5000
522	10	40	15	15	5000
75S107	25	40	25	17	5000
75S108	25	40	25	17	5000

Table 5-3 IMPORTANT SENSE AMPLIFIER PARAMETERS

Consideration must first be given to the differential input voltage requirements of the sense amplifier. The required reference voltage is calculated from the relationship:

ECL TO TTL TRANSLATOR

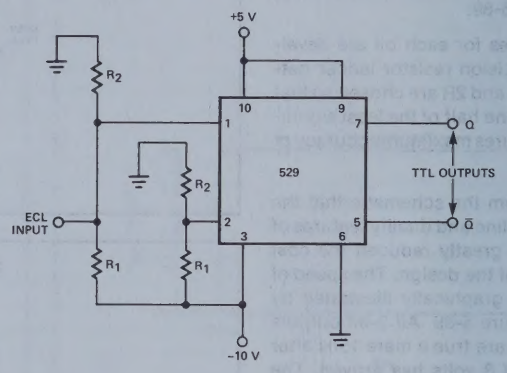


Figure 5-91

TTL TO ECL TRANSLATOR

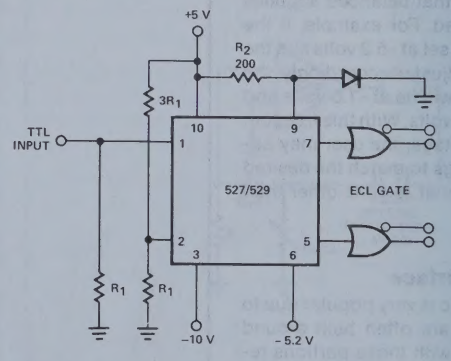


Figure 5-92

$V_{ref} \leq (I_1 - I_B)\ R1 - V_{diff}$

Where I_1 is the 1103 output current, I_B is sense amplifier bias current and V_{diff} is minimum differential voltage to switch the sense amplifier.

Thus, referring to Figure 5-68, the calculation for the NE522 and the 1103-1 becomes:

$V_{ref} \leq (900\mu A - 40\mu A)\ R - 15mV$

Hence V_{ref} must be less than 71mV for a 100 ohm resistor. Values of R1 can be selected from 100 to 1000 ohms. Resistor values less than 100 ohms do not produce sufficient voltage swings while values over 1k ohm tend to generate excessive noise from capacitively coupled signals.

In large systems noise coupled into the sense lines by stray capacitance can be very troublesome. Judicious layout patterns with sense lines being as short as possible will help, but large memories can still be difficult to control. One method of eliminating noise is to use a balanced sense line as shown in Figure 5-95.

During layout a dummy line is run parallel to the actual sense line in as close proximity as possible. One end is connected to the sense amplifier at the V_{ref} point while the other end is left open. The normal sense line is connected as usual. Electrical noise imposed upon the pair of sense lines takes the form of a common mode signal and will be rejected by the sense amplifier. Signal currents in the sense line, on the other hand, form differential signals at the sense amp causing the output to switch.

Core Memory Sense Amps

The core memory is another device requiring a sense amplifier.

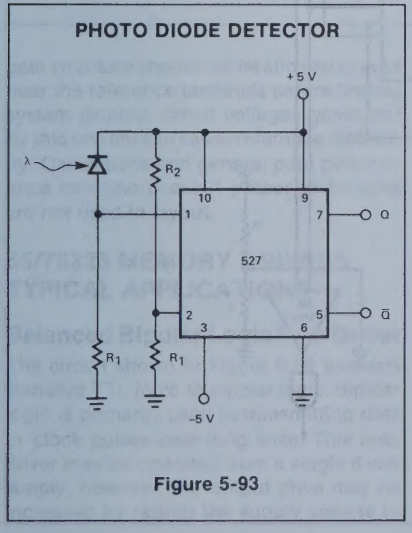


Figure 5-93

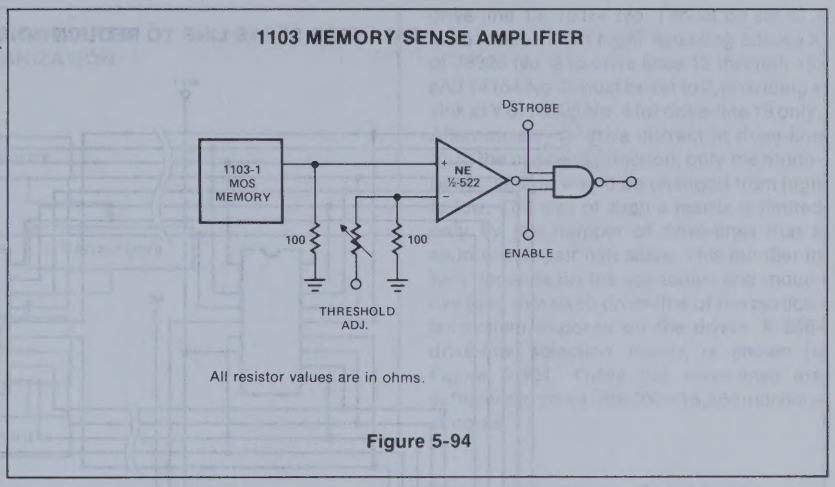


Figure 5-94

Figure 5-96 shows a simplified block diagram of memory organization in a computer. The appropriate command to the address register selects the appropriate x and y address lines. Two wires are threaded through each core. One is common to all cores in that column arranging a matrix in which any x-address line and any y-address line has only one core in common.

Both reading and writing are accomplished by driving current through the wires linking the cores. If this current exceeds a minimum value I_m, the core is reset to zero. Therefore, by driving $I_m/2$ through one of the x-address lines and through one of the y-address lines, any one core may be reset. Only the core common to both lines will receive the sum of the currents and will be reset. The rest of the cores receive $I_m/2$ and will be only half-selected. For a core to be set to the "1" state, the current is reversed in the two selecting wires.

A sense line linking all the cores in the plane together couples the read data out of the array. In order to read a specific core, a "0" is first written into that core. If its initial state was at "1", it is reset, generating a pulse on the sense line. If the core is in "0" state, no signal results.

The high currents used in core memory generate a good deal of noise. The sense amplifier used must be able to detect the difference between the disturbed one voltage, without responding to undesired signals. The threshold voltages of the sense amplifier should be adjusted to approximately the mid-point between the sum of the disturbed zero voltages and the minimum disturbed one voltage as defined in Figure 5-97.

The region on either side of the threshold voltage in which the sense amplifier cannot detect the difference between a 0 and a 1 is called the uncertainty region. This region is the sum of the varition of the input threshold voltage and the differential offset voltage and must be less than the voltage difference between ones and zeros generated by the memory core.

Signetics series 7520 Dual Core Memory Sense Amplifiers, successfully solve the basic sense amplifier problems: It provides a stable narrow input threshold, an adjustable reference and output logic functions to fulfill the several variations required in different core memory systems.

The 7520 series uses the "true comparator" technique to achieve superior amplifier threshold performance. A unique circuit design of the internal logic guarantees the fastest possible propagation. The 7520 series offers the user these advantages:

a. True Comparator technique guarantees that narrow input threshold devices can be built in volume production.
b. An external capacitor is not required for stability. True Comparator technique allows use of simple single stage preamp.
c. Clamp diodes are provided at all gate and strobe inputs.

Figure 5-98 illustrates the necessary connections to utilize the 7524 sense amplifier. The reference voltage against which the sense voltage is compared is derived via the resistor divider network from the 5 volt supply. Other connections are straight forward and for the most part self explanatory.

Care should be exercised in the board layout to minimize stray coupling of signals. Of extreme importance to the device, the reference voltage must be kept as clean as possible. For instance, ground currents from the

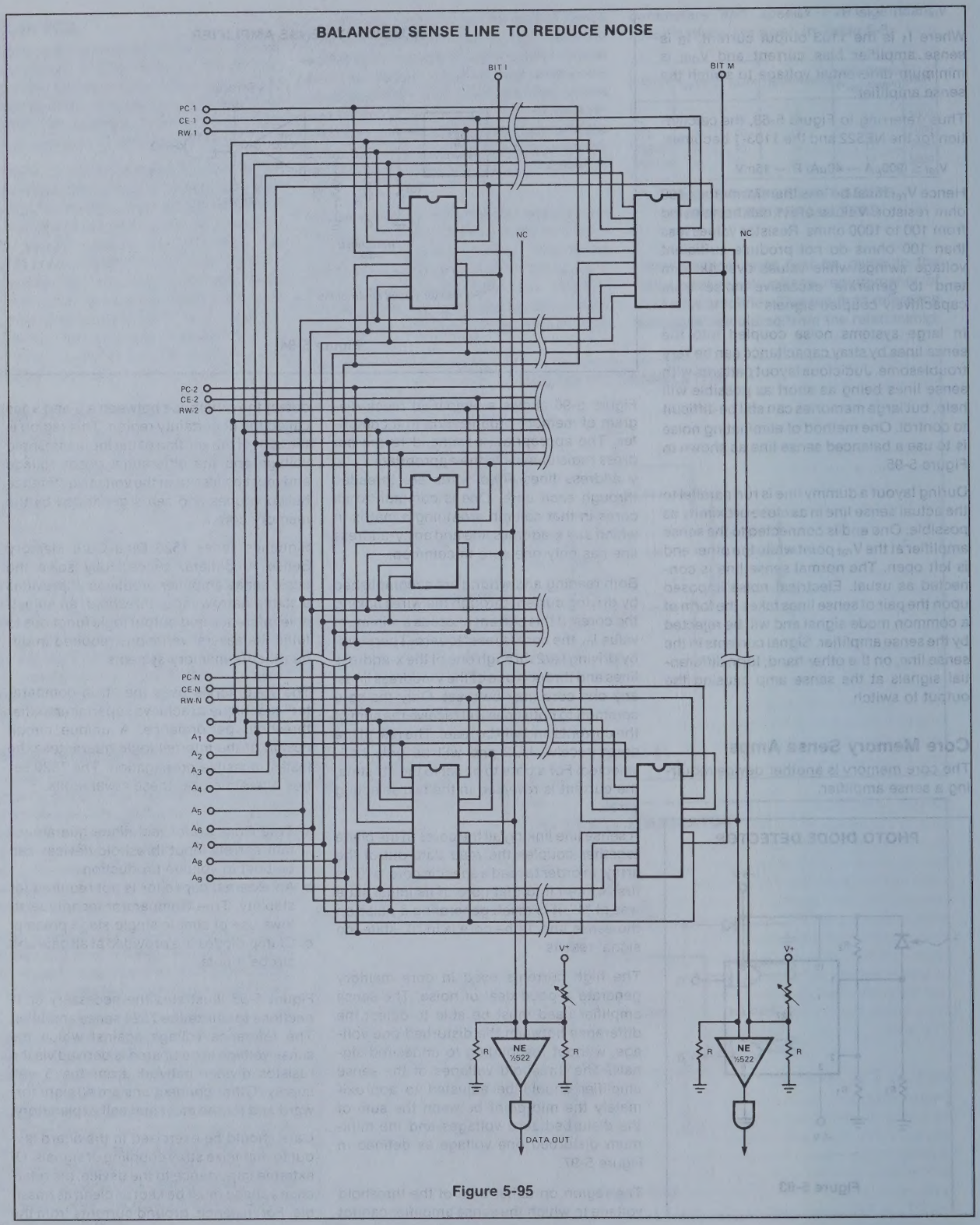

BALANCED SENSE LINE TO REDUCE NOISE
BIT I
BIT M
PC 1
CE 1
RW 1
NC
NC
PC 2
CE 2
RW 2
PC N
CE N
RW N
A1
A2
A3
A4
A5
A6
A7
A8
A9
V+
V+
R
NE
½522
R
R
NE
½522
R
DATA OUT

Figure 5-95

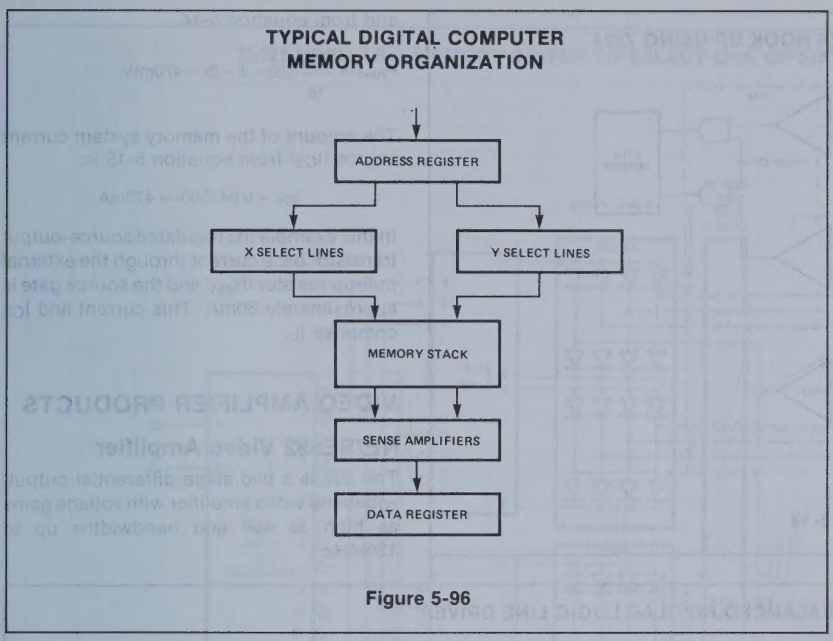


Figure 5-96

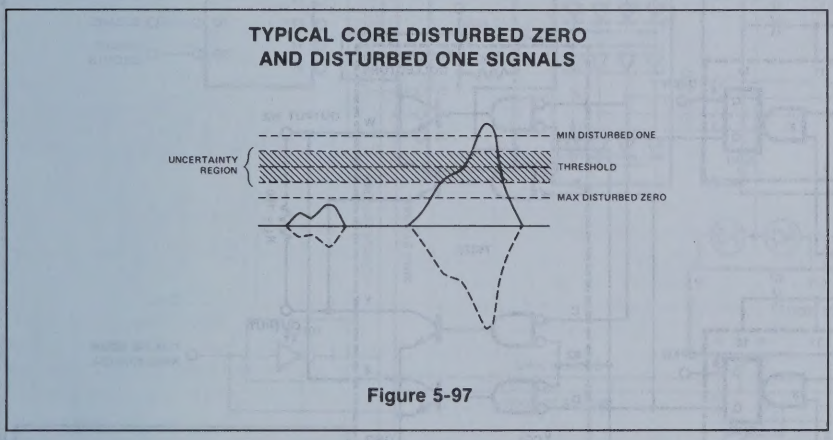


Figure 5-97

gate structure should not be allowed to pass near the reference terminals before finding system ground. Small voltages generated by this current can cause reference instability. Oscillations and general poor performance can also occur if proper techniques are not used in layout.

55/75325 MEMORY DRIVERS TYPICAL APPLICATIONS

Balanced Bipolar Logic Line Driver

The circuit shown in Figure 5-99 converts standard TTL logic to bipolar logic. Bipolar logic is primarily used in transmitting data or clock pulses over long lines. This line-driver may be operated from a single 5 volt supply; however; the output drive may be increased by raising the supply voltage to the source collectors. The circuit features a tri-state output which is off during the absence of data, thus not dissipating high power. It provides a balanced drive circuit giving maximum noise immunity when used with the proper line receiver. Large drive levels can be used to further increase noise immunity. The circuit is capable of driving twisted-pair lines of several miles in length or low-impedance coaxial lines.

In memory-drive applications the 75325 (or for full-temperature operation, the 55325) can be connected in any of several ways. Typically, however, sources and sinks are arranged in pairs from which many drive-lines branch off as shown in Figure 5-100. Here each drive-line is served by a unique combination of two source/sink pairs so that a selection matrix is formed. To select drive-line 13, 75154 No. 1 must be set to 3 (with mode select high), enabling source X of 75325 No. 2 to drive lines 12 through 15, and 74154 No. 2 must be set to 2, providing a sink at Y of 75325 No. 4 for drive-line 13 only. Alternatively, to drive current in drive-line 13 in the opposite direction, only the mode-select voltage would be changed from high to low. The size of such a matrix is limited only by the number of drive-lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive-line of the particular system imposes on the driver. A 256-drive-line selection matrix is shown in Figure 5-101. These 256 drive-lines are sufficient to serve $(256/2)^2 = 16{,}384$ individual cores.

External Resistor Calculation

A typical magnetic-memory word-drive requirement is shown in Figure 5-102. A source-output transistor of one 75325 delivers load current (I_L). The sink-output transistor of another 75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,(V_{CC2(min)} - V_S - 2.2)}{I_L - 1.6\,(V_{CC2(min)} - V_S - 2.9)} \qquad 5\text{-}13$$

where: R_{ext} is in kΩ,
$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts,
V_S is the source output voltage in volts with respect to ground,
I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 5-14.

$$P_{Rext} \approx \frac{I_L}{16}\left[V_{CC2(min)} - V_S - 2\right] \qquad 5\text{-}14$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 5-15.

$$I_{CS} \approx 0.94\, I_L \qquad 5\text{-}15$$

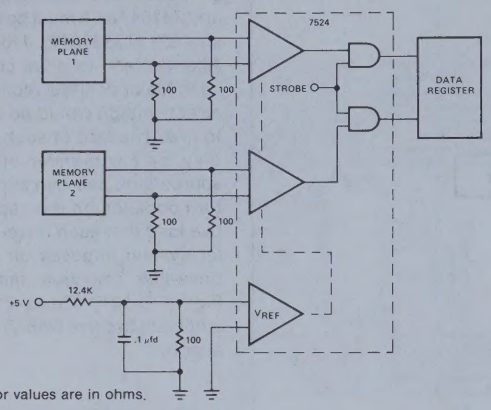
where: I_{CS} is in mA.

As an example, let $V_{CC2(min)} = 20V$ and $V_L = 3V$ while I_L of 500mA flows.

Using Equation 5-13,

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5k\Omega$$

TYPICAL SENSE AMPLIFIER HOOK UP USING 7524



All resistor values are in ohms.

Figure 5-98

and from equation 5-14,

$$P_{Rext} \approx \frac{500}{16}(20 - 3 - 2) \approx 470mW$$

The amount of the memory system current source (I_{CS}) from equation 5-15 is:

$$I_{CS} \approx 0.94\ (500) \approx 470mA$$

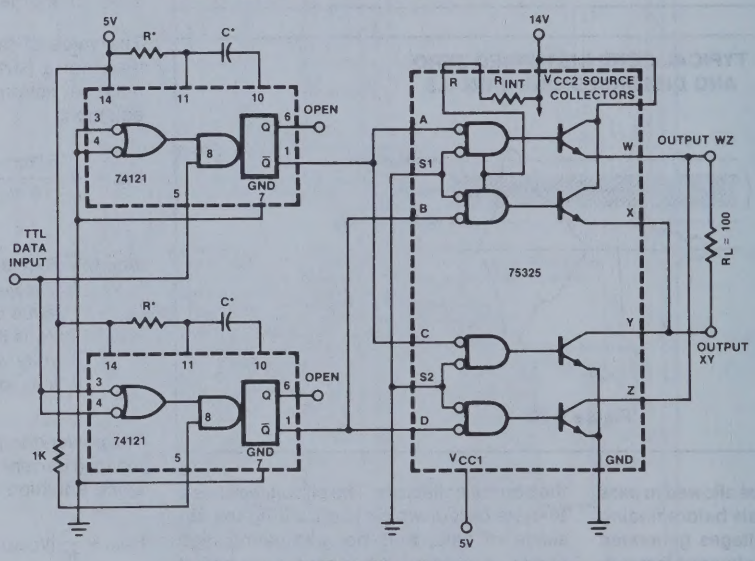
In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30mA. This current and I_{CS} comprise I_L.

VIDEO AMPLIFIER PRODUCTS

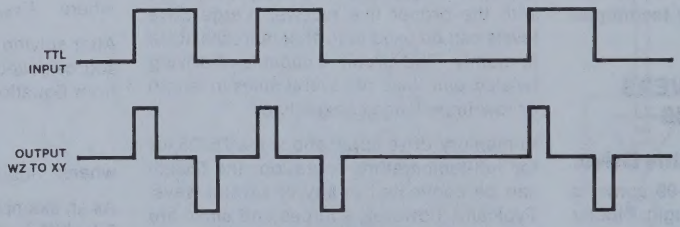
NE/SE592 Video Amplifier

The 592 is a two stage differential output, wideband video amplifier with voltage gains as high as 400 and bandwidths up to 120MHz.

BALANCED BIPOLAR LOGIC LINE DRIVER



a. Test Circuit

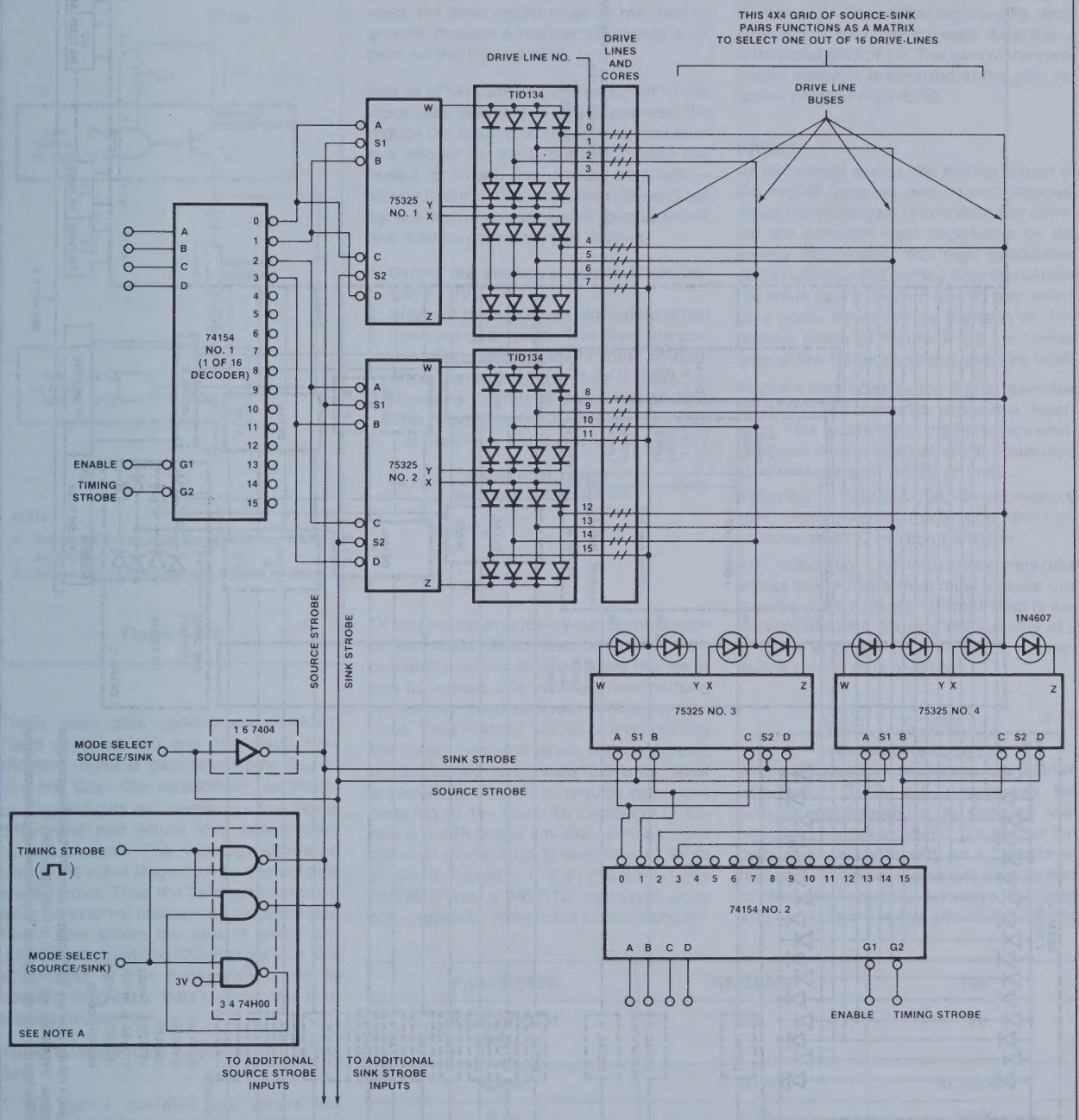


b. Voltage Waveforms

All resistors values are typical and in ohms.
*R and C are adjusted to give the desired bipolar output pulse width.

Figure 5-99

75325 USED AS A MEMORY DRIVER TO SELECT ONE OF SIXTEEN DRIVE LINES



NOTE A This optional mode select and timing strobe technique can be used in place of the 7440 mode select and 74154 timing strobe when minimum time skew is desired.

Figure 5-100

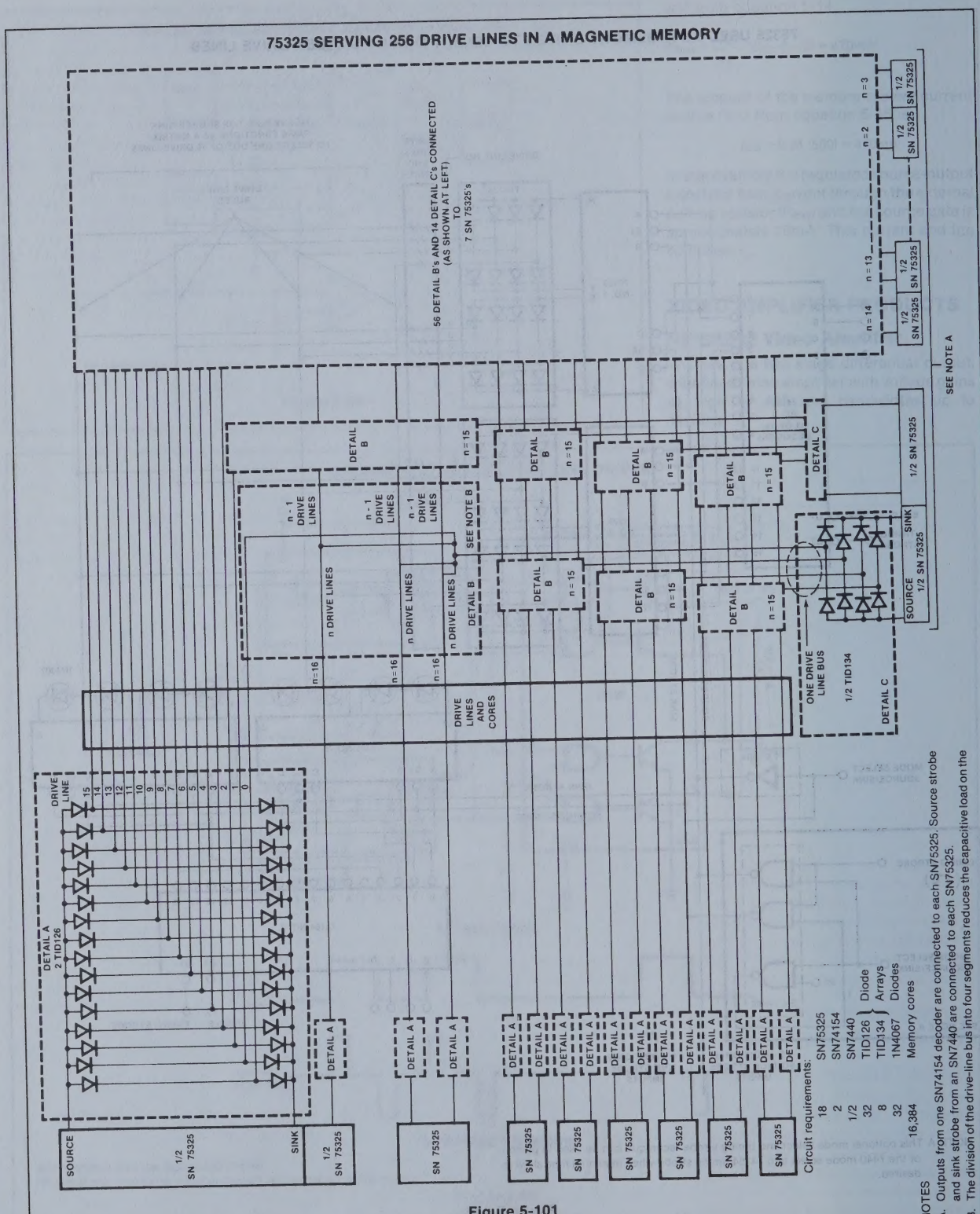
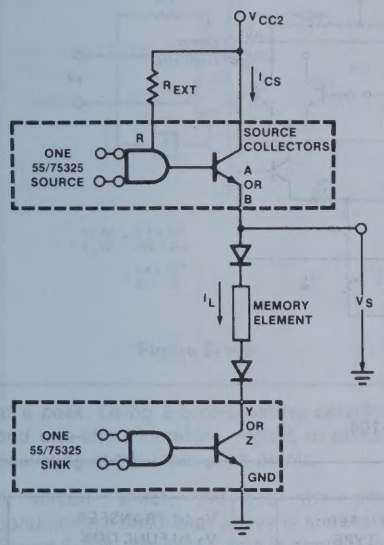

75325 SERVING 256 DRIVE LINES IN A MAGNETIC MEMORY
DETAIL A
2 TID126
DRIVE LINE
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
SOURCE
SINK
1/2 SN 75325
DETAIL A
SN 75325
DRIVE LINES AND CORES
n = 16
n DRIVE LINES
n - 1 DRIVE LINES
DETAIL B
SEE NOTE B
n = 15
56 DETAIL B's AND 14 DETAIL C's CONNECTED (AS SHOWN AT LEFT) TO 7 SN 75325's
n = 14
n = 13
n = 2
n = 3
1/2 SN 75325
SEE NOTE A
DETAIL C
ONE DRIVE LINE BUS
1/2 TID134
SOURCE
SINK
1/2 SN 75325
Circuit requirements:
18 SN75325
2 SN74154
1/2 SN7440
32 TID126 } Diode
8 TID134 } Arrays
32 1N4067 Diodes
16,384 Memory cores
NOTES
A. Outputs from one SN74154 decoder are connected to each SN75325. Source strobe and sink strobe from an SN7440 are connected to each SN75325.
B. The division of the drive-line bus into four segments reduces the capacitive load on the SN75325 driver.

Figure 5-101

TYPICAL MAGNETIC MEMORY WORD DRIVE REQUIREMENT



NOTE

A. For clarity, partial logic diagrams of two 75325's are shown.
B. Source and sink shown are in different packages.

Figure 5-102

Three basic gain options are provided. Fixed gains of 400 and 100 result from shorting together gain select pins G_{1A} — G_{1B} and G_{2A}—G_{2B} respectively. As shown by Figure 5-103 the emitter circuits of the differential pair return thru independent current sources. This topology allows no gain in the input stage if all gain select pins are left open. Thus the third gain option of tying an external resistance across the gain select pins allows the user to select any desired gain from 0 to 400 volts per volt. The advantages of this configuration will be covered in greater detail under the filter application section.

Three factors should be pointed out at this time:

1. The gains specified are differential. Single ended gains are one half the stated value.
2. The circuit 3dB bandwidths are a function of and are inversely proportional to the gain settings.
3. The differential input impedance is an inverse function of the gain setting.

In applications where the signal source is a transformer or magnetic transducer the input bias current required by the 592 may be passed directly thru the source to ground. Where capacitive coupling is to be used, the base inputs must be returned to ground through a resistor to provide a dc path for the bias current.

Due to offset currents, the selection of the input bias resistors is a compromise. To reduce the loading on the source, the resistors should be large, but to minimize the output dc offset, they should be small — ideally 0 ohms. Their maximum value is set by the maximum allowable output offset and may be determined as follows:

1. Define the allowable output offset (assume 1.5V).
2. Subtract the maximum 592 output offset (from the data sheet). This gives the output offset allowed as a function of input offset currents (1.5V — 1.0V = 0.5V).
3. Divide by the circuit gain (assume 100). This refers the output offset to the input.
4. The maximum input resistor size is:

$$R_{MAX} = \frac{\text{Input Offset Voltage}}{\text{Max Input Offset Current}} \qquad 5\text{-}16$$

$$\frac{.005V}{5\mu A}$$

$$= 1.00k\Omega$$

Of paramount importance during the design of the NE592 device was bandwidth. In a monolithic device, this precludes the use of pnp transistors and standard level shifting techniques used in lower frequency devices. Thus without the aid of level shifting the output common mode voltage present on the NE592 is typically 2.9 volts. Most applications, therefore, require capacitive coupling to the load. An exception to the rule is a differential amplifier with an input common mode range greater than +2.9V as shown in Figure 5-104. In this circuit, the NE592 drives a NE511B transistor array connected as a differential cascode amplifier. This amplifier is capable of differential output voltages of 48V peak-to-peak with a 3dB bandwidth of approximately 10MHz (depending on the capacitive load). For optimum operation, R1 is set for a no signal level of +18V. The emitter resistors, R_E, were selected to give the cascode amplifier a differential gain of 10. The gain of the composite amplifier is adjusted at the gain selected point of the NE592.

Filters

As mentioned earlier, the emitter circuit of the NE592 includes two current sources. Since the stage gain is calculated by dividing the collector load impedance by the emitter impedance, the high impedance contributed by the current sources causes the stage gain to be zero with all gain select pins open. As shown by the gain vs. frequency graph of Figure 5-105 the overall gain at low frequencies is a negative 48dB.

Higher frequencies cause higher gain due to distributed parasitic capacitive reactance. This reactance in the first stage emitter circuit causes increasing stage gain until at 10MHz the gain is 0dB or unity.

Referring to Figure 5-106, the impedance seen looking across the emitter structure includes small r_e of each transistor.

Any calculations of impedance networks across the emitters then must include this quantity. The collector current level is approximately 2mA causing the quantity of 2 r_e to be approximately 32 ohms. Overall device gain is thus given by

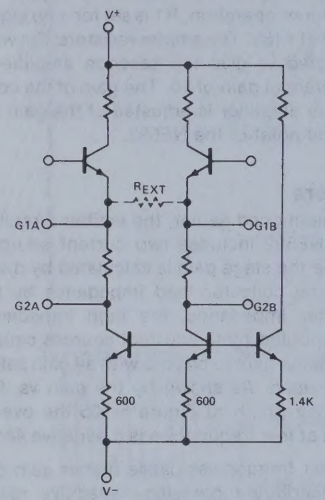
$$\frac{V_O(S)}{V_{IN}(S)} = \frac{1.4 \times 10^4}{Z_{(S)} + 32} \qquad (5\text{-}17)$$

where $Z_{(S)}$ can be a resistance or a reactive impedance. Table 5-5 summarizes the possible configurations to produce low, high, and bandpass filters. The emitter impedance is made to vary as a function of frequency by using capacitors or inductors to alter the frequency response. Included also in Table 5-5 is the gain calculation to

PARAMETER	NE/SE592	733
BANDWIDTH (MH_Z)	120	120
GAIN	0,100,400	10,100,400
R_{IN} (K)	4-30	4-250
V_{PP} (VOLTS)	4.0	4.0

Table 5-4 VIDEO AMPLIFIER COMPARISON FILE

592 INPUT STRUCTURE



All resistor values are in ohms.

Figure 5-103

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY (ALL GAIN SELECT PINS OPEN)

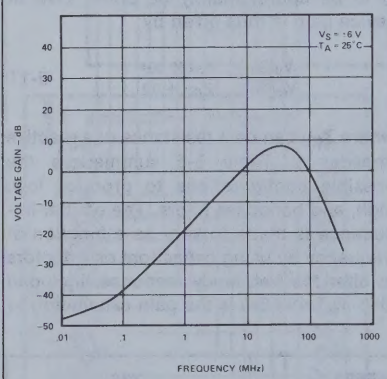


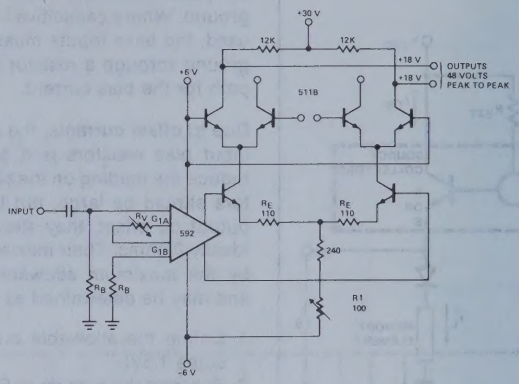
Figure 5-105

determine the voltage gain as a function of frequency.

Differentiation

With the addition of a capacitor across the gain select terminals the NE592 becomes a differentiator. The primary advantage of using the emitter circuit to accomplish differentiation is the retention of the high common mode noise rejection. Disc file playback systems rely heavily upon this common mode rejection for proper operation. Figure 5-107 shows a differential amplifier configuration with transfer function.

VIDEO AMPLIFIER WITH HIGH LEVEL DIFFERENTIAL OUTPUT



All resistor values are in ohms.

Figure 5-104

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
R, L	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
R, C	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
R, L, C	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\, s + 1/LC}\right]$
R, L, C	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE: In the networks above, the R value used is assumed to include 2 r_e, or approximately, 32 ohms.

Table 5-5 FILTER NETWORKS

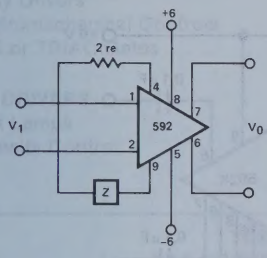
Disc file Decoding

In recovering data from disc or drum files, several steps must be taken to pre-condition the linear data. The NE592 video amplifier, coupled with the 8T20 bi-directional one-shot, provides all the signal conditioning necessary for phase encoded data.

When data is recorded on a disc, drum or tape system, the readback will be a Gaussian shaped pulse with the peak of the pulse corresponding to the actual recorded transition point. This readback signal is usually 500μV p-p to 3mV p-p for oxide coated disc files and 1 to 20mV p-p for nickel-cobalt disc files. In order to accurately reproduce the data stream originally written on the disc memory, the time of peak point of the Gaussian readback signal must be determined.

The classical approach to peak-time determination is to differentiate the input signal. Differentiation results in a voltage proportional to the slope of the input signal. The zero-crossing point of the differentiator, therefore, will occur when the input signal is

BASIC GAIN CONFIGURATION



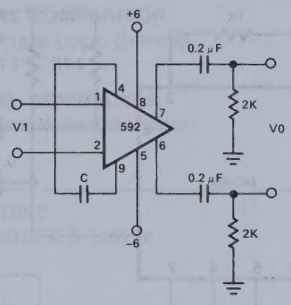
$$\frac{V_0(s)}{V_1(s)} = \frac{1.4 \times 10^4}{Z(s) + 2re} = \frac{1.4 \times 10^4}{Z(s) + 32}$$

Figure 5-106

at a peak. Using a zero-crossing detector and one-shot, therefore, results in pulses occurring at the input peak points.

A circuit which provides the preconditioning described above is shown in Figure 5-108. Readback data is applied directly to the input of the first NE592. This amplifier functions as a wideband ac coupled amplifier with a gain of 100. The NE592 is excellent for this use because of its high phase linearity, high gain and ability to directly couple the unit with the readback head. By direct coupling of readback head to amplifier, no matched terminating resistors are required and the excellent common mode rejection ratio of the amplifier is preserved. DC components are also rejected because the NE592 has no gain at dc due to the capacitance across the gain select terminals.

DIFFERENTIAL WITH HIGH COMMON MODE NOISE REJECTION



For frequency $F_1 << 1/2\ \pi(32)C$

$V_0 \cong 1.4 \times 10^4 C \frac{dvi}{dT}$

All resistor values are in ohms.

Figure 5-107

The output of the first stage amplifier is routed to a linear phase shift low pass filter. The filter is a single stage constant K filter, with a characteristic impedance of 200Ω. Calculations for the filter are as follows:

$L = 2R/\omega c$ Where R = characteristic impedance (ohms)

$C = 1/\omega c$ ωc = cutoff frequency (radians/sec)

The second NE592 is utilized as a low noise differentiator/amplifier stage. The NE592 is excellent in this application because it allows differentiation with excellent common mode noise rejection.

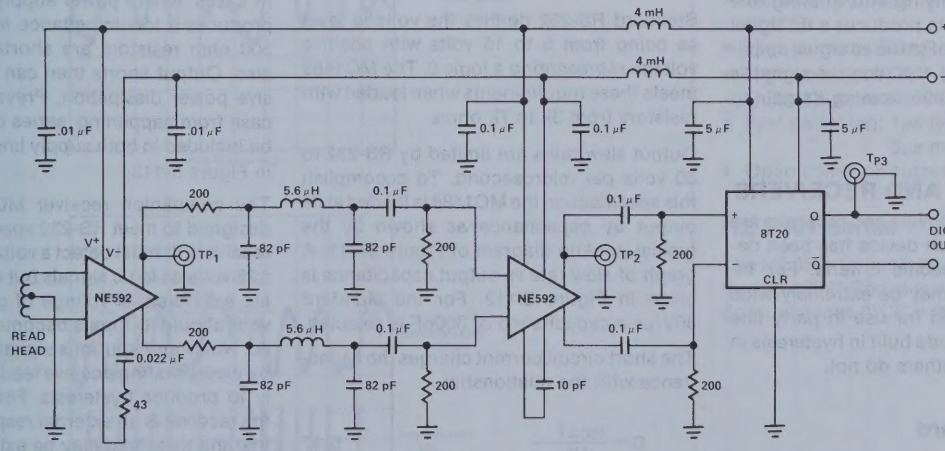
The output of the differentiator/amplifier is connected to the 8T20 bi-directional monostable unit to provide the proper pulses at the zero-crossing points of the differentiator.

The circuit in Figure 5-108 was tested with an input signal approximating that of a readback signal. The results are shown in Figure 5-110.

Automatic Gain Control

The NE592 can also be connected in conjunction with a MC1496 balanced modulator to form an excellent automatic gain control system. With the circuit of Figure 5-

5MHz PHASE—ENCODED DATA READ CIRCUITRY



All resistor values are in ohms

Figure 5-108

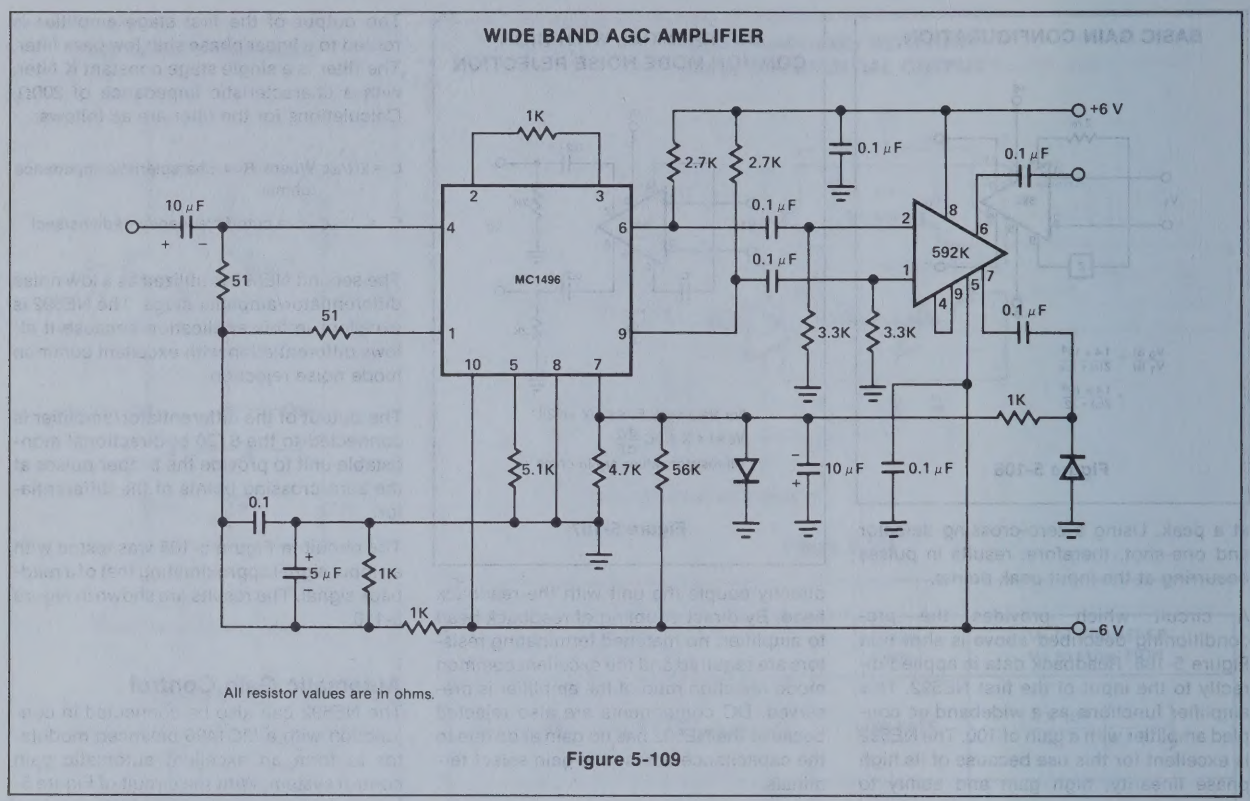


Figure 5-109

84, the signal is fed to the signal input of the MC1496 and RC coupled to the NE592. Unbalancing the carrier input of the MC1496 causes the signal to pass thru unattenuated. Rectifying and filtering one of the NE592 outputs produces a dc signal which is proportional to the ac signal amplitude. After filtering this control signal is applied to the MC1496 causing its gain to change.

LINE DRIVERS AND RECEIVERS

Many types of line drivers and receivers are available today. Each device has been designed to meet specific criteria. For instance, the device may be extremely wide band or be intended for use in party line systems. Some include built in hysteresis in the receiver while others do not.

The EIA Standard

The Electronic Industries Association has produced a set of specifications dealing with the transmission of data between data terminal and communications equipment. This is EIA Standard RS-232-C and delineates much information about signal levels and hardware configurations in data systems.

MC1488/1489

As line driver and receiver the MC1488 and MC1489 meet or exceed the RS-232 specification.

Standard RS-232 defines the voltage level as being from 5 to 15 volts with positive voltage representing a logic 0. The MC1488 meets these requirements when loaded with resistors from 3k to 7k ohms.

Output slew rates are limited by RS-232 to 30 volts per microsecond. To accomplish this specification the MC1488 is loaded at its output by capacitance as shown by the typical hookup diagram of Figure 5-111. A graph of slew rate vs output capacitance is given in Figure 5-112. For the standard 30V/μs a capacitance of 300pF is selected.

The short circuit current charges the capacitance with the relationship.

$$C = \frac{I_{SC}\Delta T}{\Delta V} \qquad 5\text{-}17$$

The EIA standard also states that output shorts to any other conductor of the cable must not damage the driver. Thus the MC1488 is designed such that the output will withstand shorts to other conductors indefinitely even if these conductors are at worst case voltage levels. In addition to output protection the MC1488 includes a 300 ohm resistor to ensure that the output impedance of the driver will be at least 300 ohms even if the power supply is turned off. In cases where power supply malfunction produces a low impedance to ground, the 300 ohm resistors are shorted to ground also. Output shorts then can cause excessive power dissipation. Preventing such a case from happening, series diodes should be included in both supply lines as pictured in Figure 5-113.

The companion receiver MC1489 is also designed to meet RS-232 specifications for receivers. It must detect a voltage from ±3 to ±25 volts as logic signals but cannot generate a differential voltage of greater than 2 volts should its inputs become open circuited. Noise and spurious signals are rejected by incorporating positive feedback internally to produce hysteresis. Featured also in the receiver is an external response node so that the threshold may be externally varied to fit the application. Figure 5-114 shows the shift in high and low trip points as a function of the programming resistance.

PERIPHERAL DRIVERS

Peripheral drivers are general purpose interface devices which interface between logic and devices requiring high current.

Application Areas

POWER SWITCHING
- Relay Drivers
- Electromechanical Controls
- SCR or TRIAC Gates

LAMP DRIVERS
- Pilot Lamps
- Intensity Control

LEVEL SHIFTERS
- TTL-to-MOS
- MOS-to-TTL

SIGNAL COMPARISON
- In-Phase Logic Detector

SIGNAL GENERATION
- Square Wave Generator

TIMING
- Dual Channel One Shot
- Two Phase MOS Clock Driver

TEST RESULTS OF DISC
FILE DECODER CIRCUIT (FIGURE 5-108)

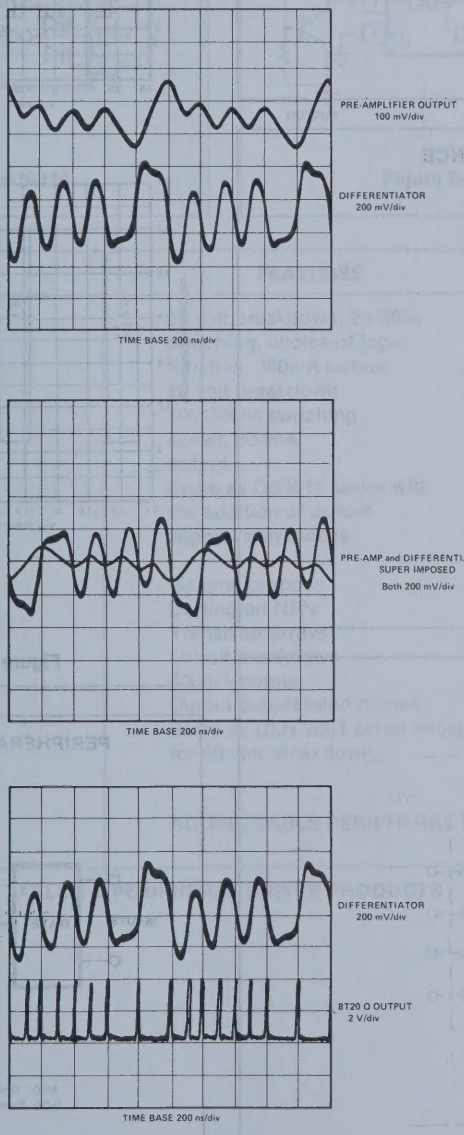


Figure 5-110

Basic Requirements for a Peripheral Driver

- Input Logic Compatibility
- High Output Current/High Voltage Compliance
- High Speed
- Application Versatility

Other Requirements Include:

- Compatability with popular supply voltages
- Medium to high power capability
- Economical packaging
- Good pin arrangement

A peripheral driver has two basic building blocks:

(See Figure 5-115)

1. TTL gate
2. Discrete transistor with good output drive capabilities

DARLINGTON TRANSISTOR ARRAYS

Darlington Transistor Arrays are high voltage, high current arrays comprised of seven silicon npn Darlington pairs on a common monolithic substrate.

ULN 2001 Series

The ULN 2001 Series features
- General purpose (DTL, TTL, PMOS, CMOS)
- High current: 500mA continuous
- High voltage: VCE = 50V
- Output suppression diodes
- Fast switching: 1μs typ.
  5μs max.
- Open collector outputs

NE 5501 Series

The NE 5501 Series features are the same as the ULN 2001 Series but with higher breakdown voltages (VCE = 90V).

5

TYPICAL LINE DRIVER-RECEIVER APPLICATION

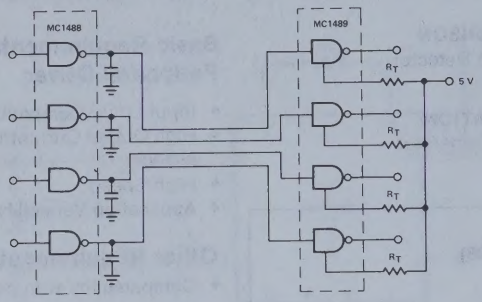


Figure 5-111

OUTPUT SLEW RATE vs. LOAD CAPACITANCE

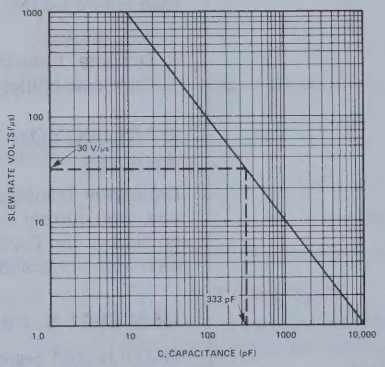


Figure 5-112

PROTECTION FROM POWER SUPPLY MALFUNCTION

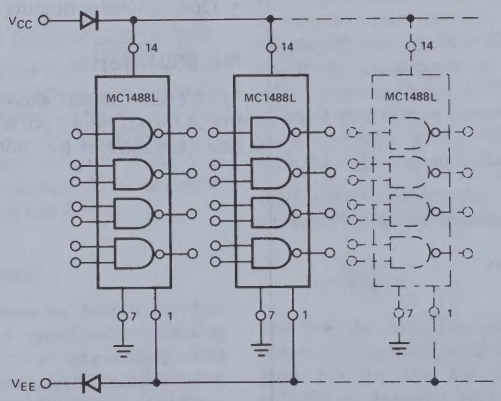
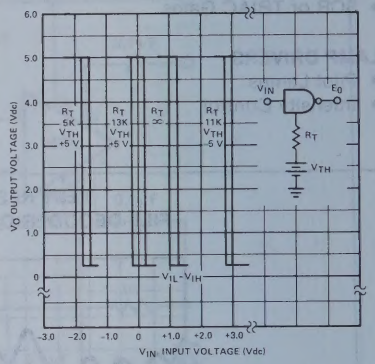


Figure 5-113

HYSTERESIS AS A FUNCTION OF PROGRAMMING RESISTANCE



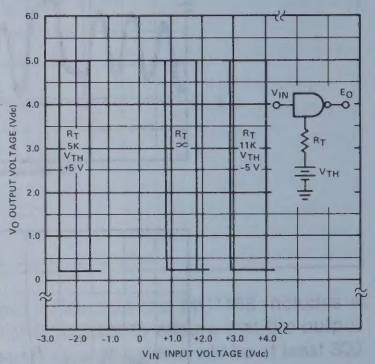


Figure 5-114

PERIPHERAL DRIVER

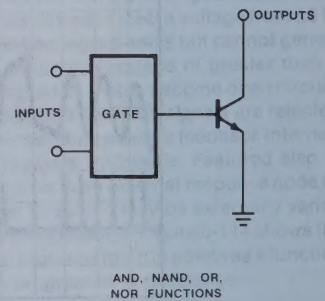


Figure 5-115

Typical Applications (NE5500 series used for V+> 50V)

P-MOS TO LOAD ULN 2002

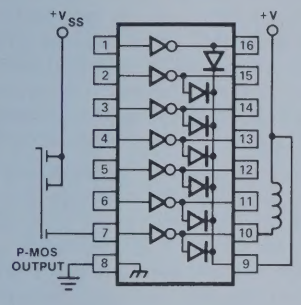


Figure 5-116

TTL TO LOAD ULN 2003

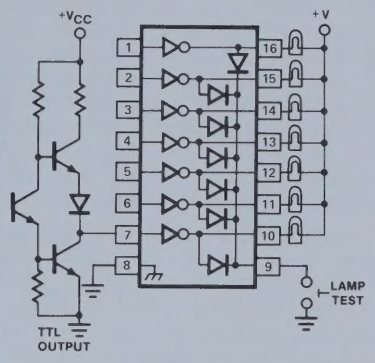


Figure 5-117

BUFFER FOR HIGHER CURRENT LOADS ULN2004

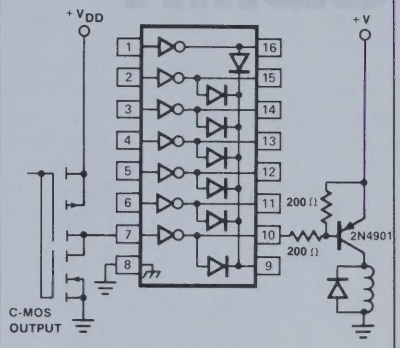
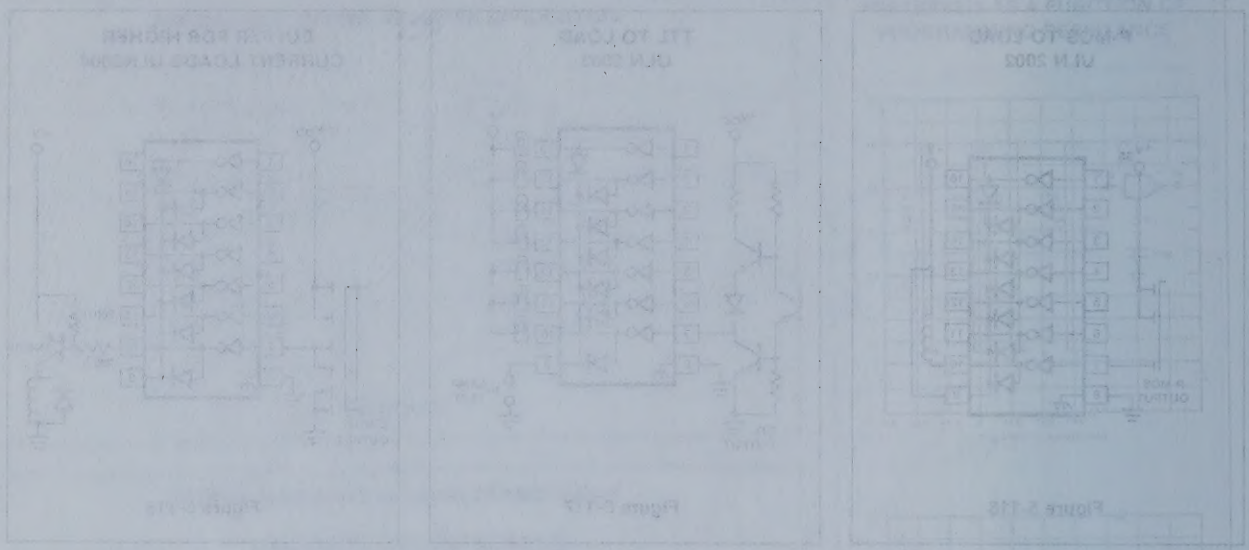


Figure 5-118

DEVICE	FEATURES
75450B	30 volt breakdown, 24-35ns
75451B	switching, choise of logic
75452B	function, 300mA output
DS3611	80 volt breakdown
DS3612	100-300ns switching
DS3613	speed, 300mA
DS3614	output
UDN5711	Same as DS3611 series with
UDN5712	the addition of output
UDN5713	suppression diodes
UDN5714	
ULN2001	General purpose
ULN2002	Darlington NPN
ULN2003	Transistor arrays
ULN2004	50 volt breakdown
	500mA output
	Output suppression diodes
NE5501	Same as ULN 2001 series except
NE5502	for 90 volt breakdown.
NE5503	
NE5504	
NE590	ADDRESSABLE PERIPHERAL DRIVERS
NE591	

TABLE 5-6 PERIPHERAL DRIVER PRODUCTS



SECTION 6
TIMERS

INTRODUCTION

In mid 1972, Signetics introduced the 555 timer, a unique functional building block that has enjoyed unprecedented popularity. The timer's success can be attributed to several inherent characteristics foremost of which are versatility, stability and low cost. There can be no doubt that the 555 timer has altered the course of the electronics industry with an impact not unlike that of the I.C. operational amplifier.

The simplicity of the timer in conjunction with its ability to produce long time delays in a variety of applications has lured many designers from mechanical timers, op amps, and various discrete circuits into the ever increasing ranks of timer users.

DESCRIPTION

The 555 timer consists of two voltage comparators, a bistable flip-flop, a discharge transistor, and a resistor divider network. To understand the basic concept of the timer let's first examine the timer in block form as in Figure 6-1.

555/556 TIMER FUNCTIONAL BLOCK DIAGRAM

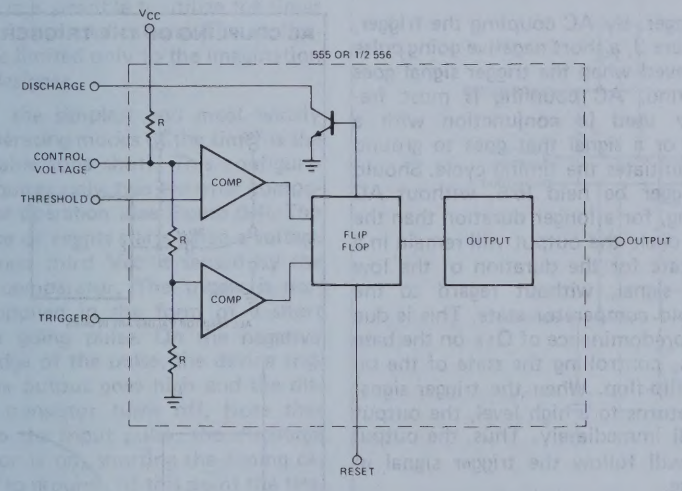


Figure 6-1

The resistive divider network is used to set the comparator levels. Since all three resistors are of equal value, the threshold comparator is referenced internally at 2/3 of supply voltage level and the trigger comparator is referenced at 1/3 of supply voltage. The outputs of the comparators are tied to the bistable flip-flop. When the trigger voltage is moved below 1/3 of the supply, the comparator changes state and sets the flip-flop driving the output to a high state. The threshold pin normally monitors the capacitor voltage of the RC timing network When the capacitor voltage exceeds 2/3 of the supply, the threshold comparator resets the flip-flop which in turn drives the output to a low state. When the output is in a low state, the discharge transistor is "on", hereby discharging the external timing capacitor. Once the capacitor is discharged, the timer will await another trigger pulse, the timing cycle having been completed.

The 555 and its complement, the 556 Dual Timer, exhibit a typical initial timing accuracy of 1% with a 50ppm/°C timing drift with temperature. To operate the timer as a one shot, only two external components are necessary; resistance & capacitance. For an oscillator, only one additional resistor is necessary. By proper selection of external components, oscillating frequencies from one cycle per half hour to 500KHz can be realized. Duty cycles can be adjusted from less than one percent to 99 percent over the frequency spectrum. Voltage control of timing and oscillation functions is also available,

Timer Circuitry

The timer is comprised of five distinct circuits; two voltage comparators, a resistive voltage divider reference, a bistable flip-flop, a discharge transistor, and an output stage that is the "totem pole" design for sink or source capability.

Q_{10} - Q_{13} comprise a Darlington differential pair which serves as a trigger comparator. Starting with a positive voltage on the trigger; Q_{10} and Q_{11} turn on when the voltage at pin 2 is moved below one third of the supply voltage. The voltage level is derived from a resistive divider chain consisting of R_7, R_8 and R_9. All three resistors are of equal value (5K ohms). At fifteen volts supply, the triggering level would be five volts. When Q_{10} and Q_{11} turn on, they provide a base drive for Q_{15}, turning it on. Q_{16} and Q_{17} form a bistable flip-flop. When Q_{15} is saturated, Q_{16} is 'off' and Q_{17} is saturated. Q_{16} and Q_{17} will remain in these states even if the trigger is removed and Q_{15} is turned 'off'. While Q_{17} is saturated, Q_{20} and Q_{14} are turned off.

The output structure of the timer is a "totem pole"design, with Q_{22} and Q_{24} being large geometry transistors capable of providing 200mA with a fifteen volt supply. While Q_{20} is 'off', base drive is provided for Q_{22} by Q_{21}, thus providing a high output.

For the duration that the output is in a high state, the discharge transistor is 'off'. Since the collector of Q_{14} is typically connected to the external timing capacitor, C, while Q_{14} is off the timing capacitor now can charge thru the timing resistor, R_A.

The capacitor voltage is monitored by the threshold comparator (Q_1 - Q_4) which is a Darlington differential pair. When the capacitor voltage reaches two thirds of the supply voltage, the current is directed from Q_3 and Q_4 thru Q_1 and Q_2. Amplification of the current change is provided by Q_5 and Q_6. Q_5 - Q_6 and Q_7 - Q_8 comprise a diode-biased amplifier. The amplified current change from Q_6 now provides a base drive for Q_{16} which is part of the bistable flip-flop to change states. In doing so, the output is driven "low", and Q_{14} the discharge transistor is turned "on" shorting the timing capacitor to ground.

The discussion to this point has only encompassed the most fundamental of the timer's operating modes and circuitry. Several points of the circuit are brought out to the real world which allow the timer to function in a variety of modes. It is important; more than that, it is essential that one understands all the variations possible in order to utilize this device to its fullest extent.

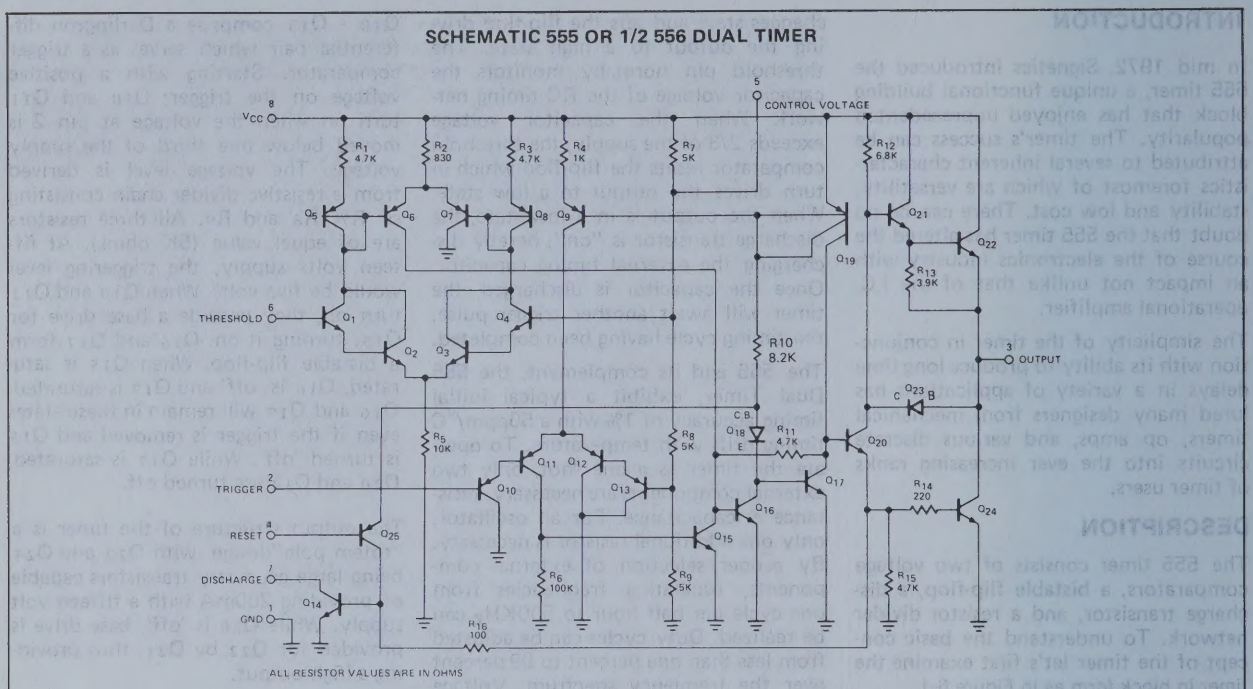


Figure 6-2

Reset Function

Regressing to the trigger mode, it should be noted that once the device has triggered and the bistable flip-flop set, continued triggering will not interfere with the timing cycle. However, there may come a time when it is necessary to interrupt or halt a timing cycle. This is the function that the reset accomplishes.

In the normal operating mode the reset transistor, Q_{25}, is off with its base held high. When the base of Q_{25} is grounded, it turns on, providing base drive to Q_{14}, turning it on. This discharges the timing capacitor, resets the flip-flop at Q_{17}, and drives the output low. The reset overrides all other functions within the timer.

Trigger Requirements

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 3, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Control Voltage

One additional point of significance, the control voltage, is brought out on the timer. As mentioned earlier, both the trigger comparator, Q_{10} - Q_{13}, and the threshold comparator, Q_1 - Q_4, are referenced to an internal resistor divider network, R_7, R_8, R_9. This network establishes the nominal two thirds of supply voltage (Vcc) trip point for the threshold comparator and one third of

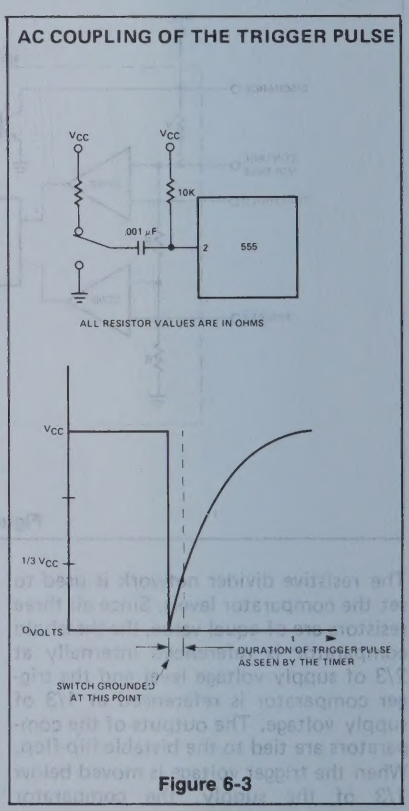


Figure 6-3

Vcc for the trigger comparator. The two thirds point at the junction of R_7, R_8 and the base of Q_4 is brought out. By imposing a voltage at this point, the comparator reference levels may be shifted either higher or lower than the nominal levels of one third and two thirds of the supply voltage. Varying the voltage at this point will vary the timing. This feature of the timer opens a multitude of application possibilities such as using the timer as a voltage controlled oscillator, pulse width modulator, etc. For applications where the control voltage function is not used, it is strongly recommended that a bypass capacitor (.01μF) be place across the control voltage pin and ground. This will increase the noise immunity of the timer to high frequency trash which may monitor the threshold levels causing timing error.

Monostable Operation

The timer lends itself to three basic operating modes:

1. Monostable (one shot)
2. Astable (oscillatory)
3. Time delay

By utilizing any one or combination of basic operating modes and suitable variations it is possible to utilize the timer in a myriad of applications. The applications are limited only to the imagination of the designer.

One of the simplest and most widely used operating modes of the timer is the monostable (one shot). This configuration requires only two external components for operation (See Figure 6-4). The sequence of events starts when a voltage below one third Vcc is sensed by the trigger comparator. The trigger is normally applied in the form of a short negative going pulse. On the negative going edge of the pulse, the device triggers, the output goes high and the discharge transistor turns off. Note that prior to the input pulse, the discharge transistor is on, shorting the timing capacitor to ground. At this point the timing capacitor, C, starts charging thru the timing resistor, R. The voltage on the capacitor increases exponentially with a time constant T = RC. Ignoring capacitor leakage, the capacitor will reach the two thirds Vcc level in 1.1 time constants or

$$T = 1.1\ RC \qquad 6\text{-}1$$

where T is in seconds; R is in ohms and; C is in Farads. This voltage level trips the threshold comparator, which in turn drives the output low and turns on the discharge transistor. The transistor discharges the capacitor, C, rapidly. The timer has completed its cycle and will now await another trigger pulse.

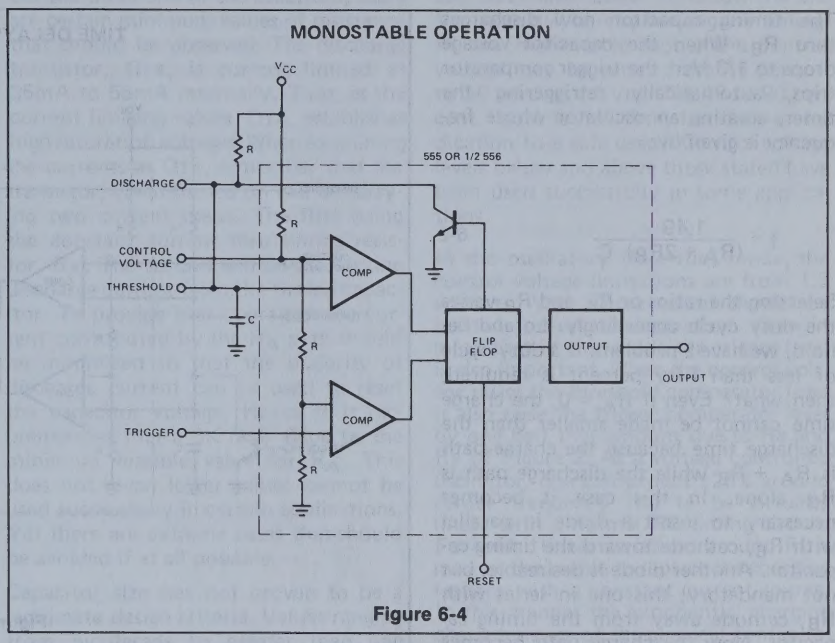


Figure 6-4

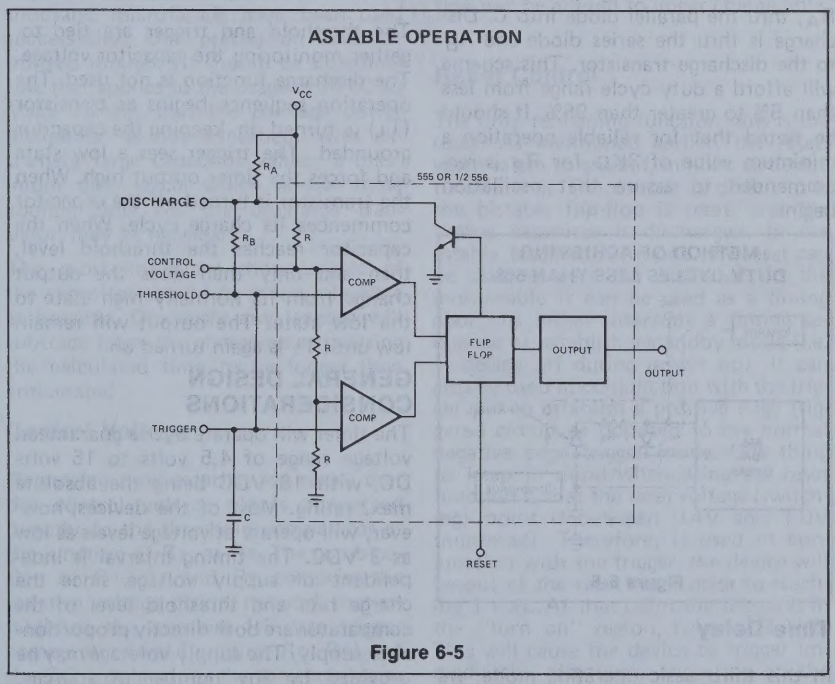


Figure 6-5

Astable Operation

In the astable (free run) mode, only one additional component, Rb is necessary. The trigger is now tied to the threshold pin. At power up, the capacitor is discharged, holding the trigger low. This triggers the timer, which establishes the capacitor charge path thru R_A and R_B. When the capacitor reaches the threshold level of 2/3 Vcc, the output drops low and the discharge transistor turns on.

The timing capacitor now discharges thru R_B. When the capacitor voltage drops to 1/3 Vcc, the trigger comparator trips, automatically retriggering the timer, creating an oscillator whose frequency is given by:

$$f = \frac{1.49}{(R_A + 2R_B)\ C} \qquad 6\text{-}2$$

Selecting the ratios or R_A and R_B varies the duty cycle accordingly. Lo and behold, we have a problem. If a duty cycle of less than fifty percent is required, then what? Even if $R_A = 0$, the charge time cannot be made smaller than the discharge time because the charge path is $R_A + R_B$ while the discharge path is R_B alone. In this case it becomes necessary to insert a diode in parallel with R_B, cathode toward the timing capacitor. Another diode is desireable, but not mandatory, this one in series with R_B, cathode away from the timing capacitor. Now the charge path becomes R_A, thru the parallel diode into C. Discharge is thru the series diode and R_B to the discharge transistor. This scheme will afford a duty cycle range from less than 5% to greater than 95%. It should be noted that for reliable operation a minimum value of 3KΩ for R_B is recommended to assure that oscillation begins.

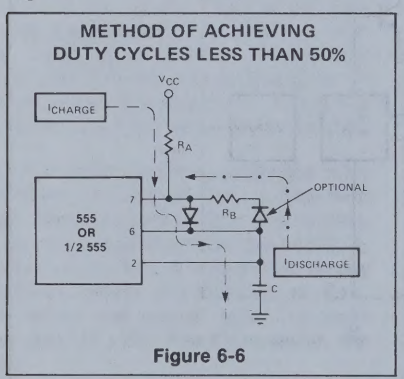


Figure 6-6

Time Delay

In this third basic operating mode, we aim to accomplish something a little different from monostable operation. In the monostable mode, when a trigger was applied, the output immediately changed to the high state, timed out, and returned to its pre-trigger low state. in the time delay mode, we require the output not to change state upon triggering, but at some precalculated time after trigger is received.

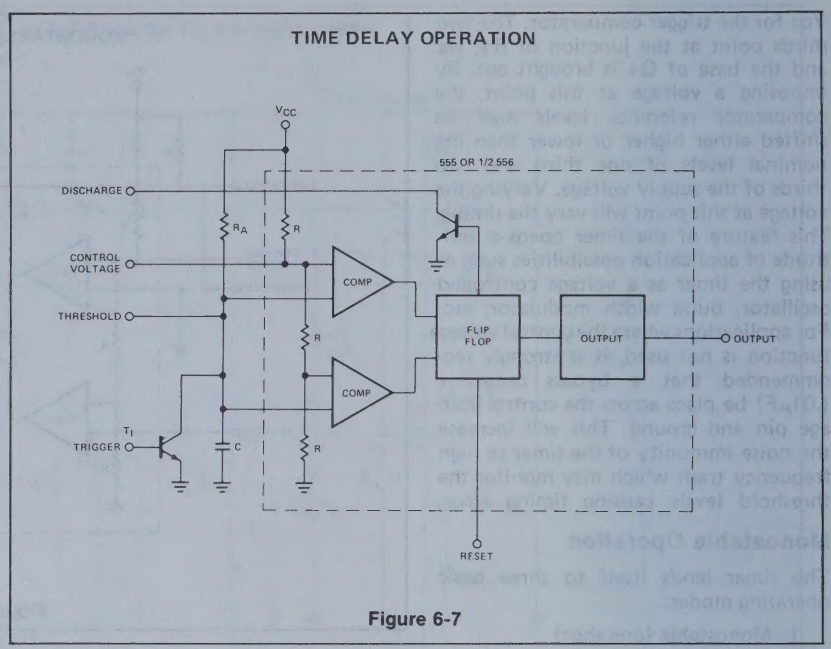


Figure 6-7

The threshold and trigger are tied together monitoring the capacitor voltage. The discharge function is not used. The operation sequence begins as transistor (T_1) is turned on, keeping the capacitor grounded. The trigger sees a low state and forces the timer output high. When the transistor is turned off the capacitor commences its charge cycle. When the capacitor reaches the threshold level, then and only then does the output change from its normally high state to the low state. The output will remain low until T_1 is again turned on.

GENERAL DESIGN CONSIDERATIONS

The timer will operate over a guaranteed voltage range of 4.5 volts to 15 volts DC, with 16 VDC being the absolute max. rating. Most of the devices, however, will operate at voltage levels as low as 3 VDC. The timing interval is independent of supply voltage since the charge rate and threshold level of the comparator are both directly proportional to supply. The supply volatage may be provided by any number of sources: however, several precautions should be taken. The most important, the one which provides the most headaches if not practiced, is good power supply filtering and adequate bypassing. Ripple on the supply line can cause loss of timing accuracy. The threshold level shifts causing a change of charging current. This will cause a timing error for that cycle.

Due to the nature of the output structure, a high power totem pole design, the output of the timer can exhibit large current spikes on the supply line. Bypassing is necessary to eliminate this phenomenon. A capacitor across the Vcc and ground, ideally, directly across the device is necessary. The size of capacitor will depend on the specific application. Values of capacitance from .01μF to 10μF are not uncommon. Note that the bypass capacitor would be as close to the device as physically possible.

Selecting External Components

In selecting the timing resistor and capacitor, there are several considerations to be taken into account.

Stable external components are necessary for the RC network if good timing accuracy is to be maintained. The timing resistor(s) should be of the metal film variety if timing accuracy and repeatability are important design criteria. The timer exhibits a typical initial accuracy of one percent. That is, with any one RC network, from timer to timer only one percent change is to be expected. Most of the initial timing error (i.e. deviation from the formula) is due to inaccuracies of external components. Resistors range from their rated values by .01% to 10 and 20 percent. Capacitors may have a 5 to 10 percent deviation from rated capacity. Therefore, in a

system where timing is critical, an adjustable timing resistor or precision components are necessary. For best results, a good quality trim pot, placed in series with the largest feasible resistance will allow for best adjustability and performance.

The timing capacitor should be a high quality, stable component with very low leakage characteristics. *Under no circumstances should ceramic disc capacitors be used in the timing network!* Ceramic disc capacitors are not sufficiently stable in capacitance to operate properly in an RC mode. Several acceptable capacitor types are: silver mica, mylar, polycarbonate, polystyrene, tantulum or similar types.

The timer typically exhibits a small negative temperature coefficient (50ppm/°C). If timer accuracy over temperature is a consideration, timing components with a small positive temperature coefficient should be chosen. This combination will tend to cancel timing drift due to temperature.

In selecting the values for the timing resistors and capacitor, several points should be considered. A minimum value of threshold current is necessary to trip the threshold comparator. This value is .25μA. To calculate the maximum value of resistance, keep in mind that at the time the threshold current is required, the voltage potential on the threshold pin is two thirds of supply. Therefore:

$$V_{potential} = V_{cc} - V_{capacitor}$$

$$V_{potential} = V_{cc} - 2/3\ V_{cc} = 1/3\ V_{cc}$$

Maximum resistance is then defined as

$$R_{max} = \frac{V_{cc} - V_{cap}}{I_{thresh}} \qquad 6\text{-}3$$

Example: $V_{cc} = 15V$

$$R_{max} = \frac{15 - 10}{.25\ (10^{-6})} = 20M\Omega$$

$V_{cc} = 5V$

$$R_{max} = \frac{5 - 3.33}{.25\ (10^{-6})} \qquad 6.6M\Omega$$

NOTE: If using a large value of timing resistor, be certain that the capacitor leakage is significantly lower than the charging current available to minimize timing error.

On the other end of the spectrum, there are certain minimum values of resistance that should be observed. The discharge transistor, Q_{14}, is current limited at 35mA to 55mA internally. Thus, at the current limiting values, Q_{14}, establishes high saturation voltages. When examining the currents at Q_{14}, remember that the transistor, when turned on will be carrying two current loads. The first being the constant current thru timing resistor, R_A. The second will be the varying discharge current from the timing capacitor. To provide best operation the current contributed by the R_A path should be minimized so that the majority of discharge current can be used to reset the capacitor voltage. Hence it is recommended that a 5K ohm value be the minimum feasible value for R_A. This does not mean lower values cannot be used successfully in certain applications. Yet there are extreme cases that should be avoided if at all possible.

Capacitor size has not proven to be a legitimate design criteria. Values ranging from picofarads to greater than one thousand microfarads have been used successfully. One precaution need be utilized though. (It should be a cardinal rule that applies to the usage of all I C's.) Make certain that the package power dissipation is not exceeded. With extremely large capacitor values, a maximum duty cycle which allows some cooling time for the discharge transistor, may be necessary.

The most important characteristic of the capacitor should be as low a leakage as possible. Obviously any leakage will subtract from the charge count causing the calculated time to be longer than anticipated.

Control Voltage

Regressing momentarily, we recall that the control voltage pin is connected directly to the threshold comparator at the junction of R_7, or R_8. The combination of R_7, R_8 and R_9 comprise the resistive voltage divider network that establishes the nominal 1/3 Vcc trigger comparator level (junction R_8, R_9) and the 2/3 Vcc level for the threshold comparator (junction R_7, R_8).

For most applications, the control voltage function is not used and therefore is bypassed to ground with a small capacitor for noise filtering. The control voltage function, in other applications becomes an integral part of the design. By imposing a voltage at this pin, it becomes possible to vary the threshold comparator "set" level above or below the 2/3 Vcc nominal, hereby varying the timing. In the monostable mode, the control voltage may be varied from 45 percent to 90 percent of Vcc. The 45 to 90 percent figure is not firm, but only an indication to a safe usage. Control voltage levels below and above those stated have been used successfully in some applications.

In the oscillatory (free run) mode, the control voltage limitations are from 1.7 volts to Vcc. These values should be heeded for reliable operation. Keep in mind that in this mode the trigger level is also important. When the control voltage raises the threshold comparator level it also raise the trigger comparator level by one half that amount due to R_8 and R_9 of Figure 2. As a voltage controlled oscillator, one can expect ±25% around center frequency (f_o) to be virtually linear with a normal RC timing circuit. For wider linear variations around F_o it may be desireable to replace the charging resistor with a constant current source. In this manner the exponential charging characteristics of the classical configuration will be altered to linear charge time.

Reset Control

The only remaining function now is the reset. As mentioned earlier, the reset, when taken to ground, inhibits all device functioning. The output is driven low, the bistable flip-flop is reset, and the timing capacitor is discharged. In the astable (oscillatory) mode, the reset can be used to gate the oscillator. In the monostable it can be used as a timing abort to either interrupt a timing sequence or establish a standby mode (i.e. – device off during power up). It can also be used in conjunction with the trigger pin to establish a positive edge triggered circuit as opposed to the normal negative edge trigger mode. One thing to keep in mind when using the reset function is that the reset voltage (switching) point is between 0.4V and 1.0V (min/max). Therefore, if used in conjunction with the trigger, the device will be out of the reset mode prior to reaching 1 volt. At that point the trigger is in the "turn on" region, below 1/3 Vcc. This will cause the device to trigger immediately, effectively triggering on the positive going edge if a pulse is applied to pins 4 and 2 simultaneously.

FREQUENTLY ASKED APPLICATIONS QUESTIONS

The following is a harvest of various maladies, exceptions, and idiosyncracies that may exhibit themselves from time

to time in various applications. Rather than cast aspersions, a quick review of this list may uncover a solution to the problem at hand.

1. In the oscillator mode when reset is released the *first time constant* is approximately *twice as long as the rest.* Why?

   Answer: In the oscillator mode the capacitor voltage fluctuates between 1/3 and 2/3 of the supply voltage. When reset is pulled down the capacitor discharges completely. Thus for the first cycle it must charge from ground to 2/3 Vcc which takes twice as long.

2. What is *maximum frequency of oscillations?*

   Answer: Most devices will oscillate about 1M Hz. However, in the interest of temperature stability one should operate only up to about 500kHz.

3. What is *temperature drift* for *oscillator mode?*

   Answer: Temperature drift of oscillator mode is 3 times that of one shot mode due to addition of second voltage comparator. Frequency always increases with an increasing temperature. Therefore it is possible to partially offset this drift with an offsetting temperature coefficient in the external resistor/capacitor combination.

4. Oscillator exhibits spurious *oscillations on cross over points.* Why?

   Answer: The 555 can oscillate due to feedback from power supply. Always bypass with sufficient capacitance close to the device for all applications.

5. Trying to drive a *relay* but 555 *hangs up.* How come?

   Answer: Inductive feedback. A clamp diode across the coil prevents the coil from driving pin 3 below a negative .6 volts. This negative voltage is sufficient in some cases to cause the timer to malfunction. The solution is to drive the relay through a diode thus preventing pin 3 from ever seeing a negative voltage.

6. Double triggering of the TTL loads sometimes occurs. Why?

   Answer: Due to the high current capability and fast rise and fall times of the output a totem pole structure different from the TTL classical structure was used. Near TTL threshold this output exhibits a cross over distortion which may double trigger logic. A 1000 pF capacitor from the output to ground will eliminate any false triggering.

7. What is the longest time I can get out of the timer?

   Answer: Times exceeding an hour are possible, but not always practical. Large capacitors with low leakage specs are quite expensive. It becomes cheaper to use a countdown scheme (see Figure 15) at some point dependent on required accuracy. Normally 20 to 30 min. is the longest feasible time.

DRIVING HIGH Q INDUCTIVE LOADS

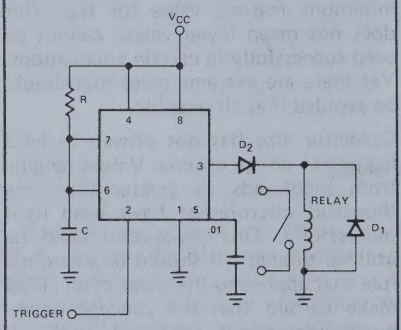


Figure 6-8

DESIGN FORMULAS

Before entering the section on specific applications it is advantageous to review the timing formulas. The formulas given here apply to the 555 and 556 devices.

MONOSTABLE TIMING

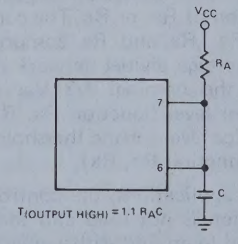


Figure 6-9a

TRUE TIME DELAY

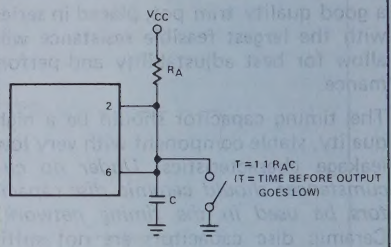


Figure 6-9b

MODIFIED DUTY CYCLE (ASTABLE)

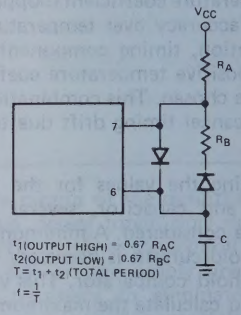


Figure 6-9c

ASTABLE TIMING

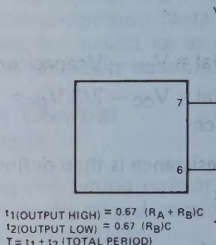


Figure 6-9d

APPLICATIONS

The timer since introduction has spurred the imagination of thousands. Thus the ways in which this device has been used are far too numerous to present each one. A review of the basic operation and basic modes has previously been given. Presented here are some ingenious applications devised by our applications engineers and by some of our customers.

Missing Pulse Detector

Using the circuit of Figure 6-10a, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure 6-10b shows the actual waveforms seen in this mode of operation.

SCHEMATIC DIAGRAM

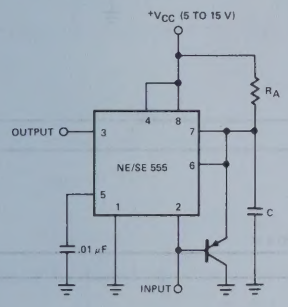


Figure 6-10a

EXPECTED WAVE FORMS

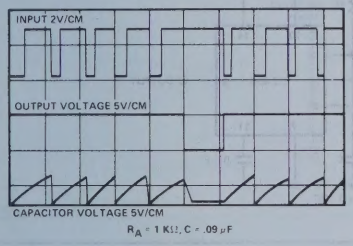


Figure 6-10b

Frequency Divider

If the input frequency is known, the timer can easily be used as a frequency divider by adjusting the length of the timing cycle.

SCHEMATIC DIAGRAM

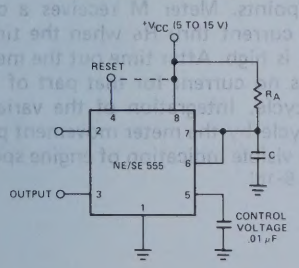


Figure 6-11a

EXPECTED WAVE FORMS

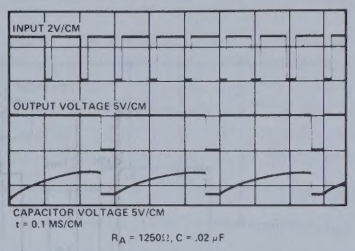


Figure 6-11b

Figure 6-11b shows the waveforms of the timer in Figure 6-11a when used as a divide by three circuit. This application makes use of the fact that this circuit cannot be retriggered during the timing cycle.

Pulse Width Modulation (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 6-12a. The circuit is triggered with a continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (pin 5). This has the effect of modulating the pulse width as the control voltage varies. Figure 6-12b shows the actual waveform generated with this circuit.

DEVICE SCHEMATIC

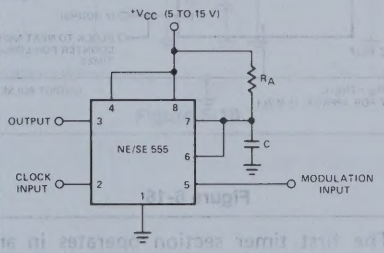


Figure 6-12a

EXPECTED WAVE FORMS

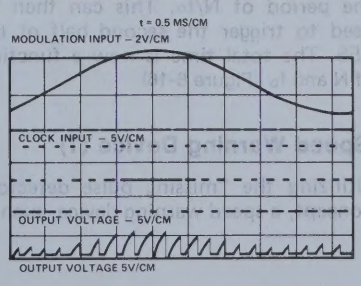


Figure 6-12b

Pulse Position Modulation (PPM)

This application uses the timer connected for astable (free-running) operation, Figure 6-13a, with a modulating signal again applied to the control voltage terminal. Now the pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 6-13b shows the waveform generated for triangle wave modulation signal.

SCHEMATIC DIAGRAMS

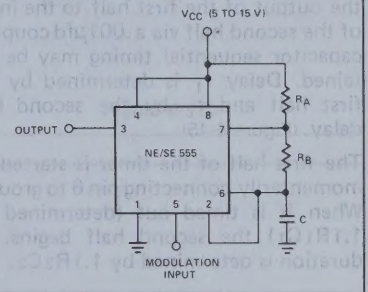


Figure 6-13a

EXPECTED WAVE FORMS

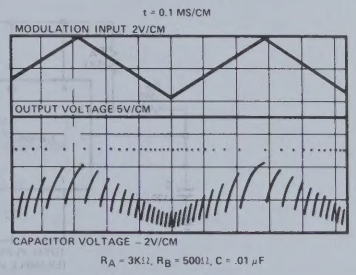


Figure 6-13b

TONE BURST GENERATOR

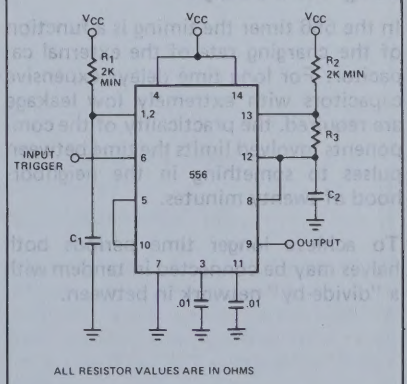


Figure 6-14

Tone Burst Generator

The 556 Dual Timer makes an excellent tone burst generator. The first half is connected as a one shot and the second half as an oscillator. (Figure 6-14)

The pulse established by the one shot turns on the oscillator allowing a burst to be generated.

Sequential Timing

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a .001μfd coupling capacitor sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay. (Figure 6-15)

The first half of the timer is started by momentarily connecting pin 6 to ground. When it is timed out (determined by $1.1R_1C_1$) the second half begins. Its duration is determined by $1.1R_2C_2$.

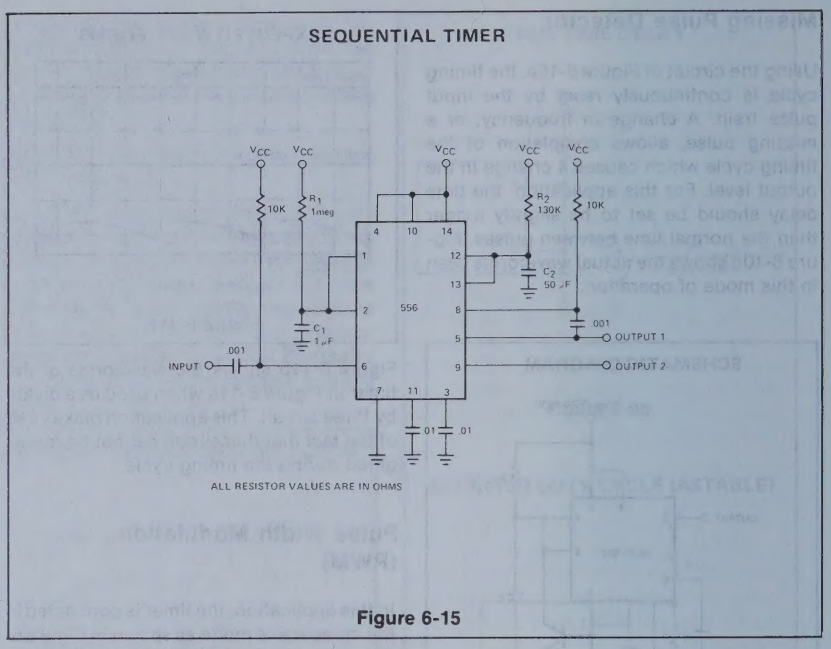


Figure 6-15

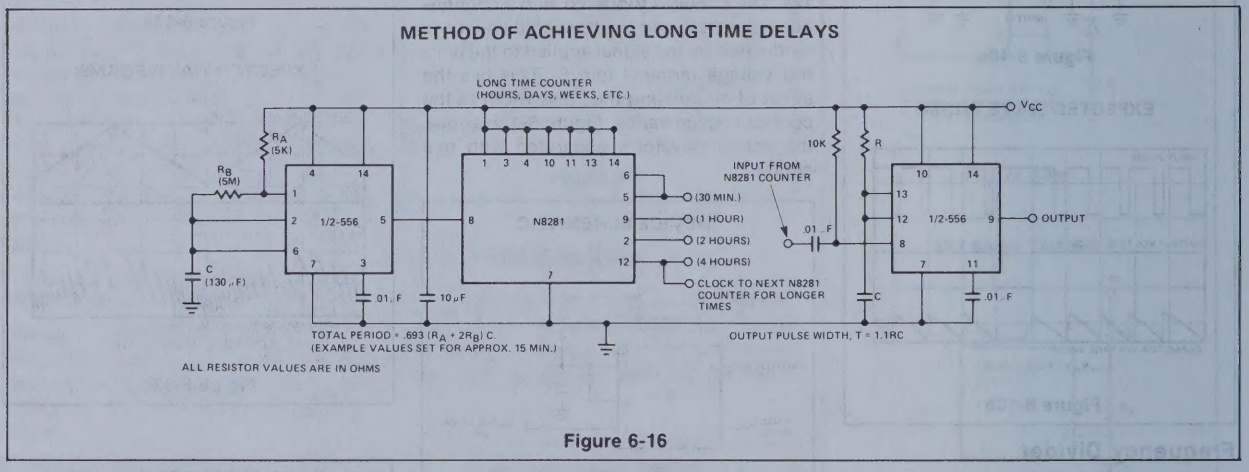


Figure 6-16

Long Time Delays

In the 556 timer the timing is a function of the charging rate of the external capacitor. For long time delays expensive capacitors with extremely low leakage are required. the practicality of the components involved limits the time between pulses to something in the neighborhood of twenty minutes.

To achieve longer time periods both halves may be connected in tandem with a "divide-by" network in between.

The first timer section operates in an oscillatory mode with a period of $1/f_o$. This signal is then applied to a "Divide-by-N" network to give an output with the period of N/f_o. This can then be used to trigger the second half of the 556. The total time is now a function of N and f_o (Figure 6-16)

Speed Warning Device (1)

Utilizing the "missing pulse detector" concept, a speed warning device, such as depicted, becomes a simple and inexpensive circuit (Figure 6-17a).

Car Tachometer (1)

The timer receives pulses from the distributor points. Meter M receives a calibrated current thru R_6 when the timer output is high. After time out the meter receives no current for that part of the duty cycle. Integration of the variable duty cycle by the meter movement provides a visible indication of engine speed (Figure 6-18).

SCHEMATIC OF SPEED WARNING DEVICE

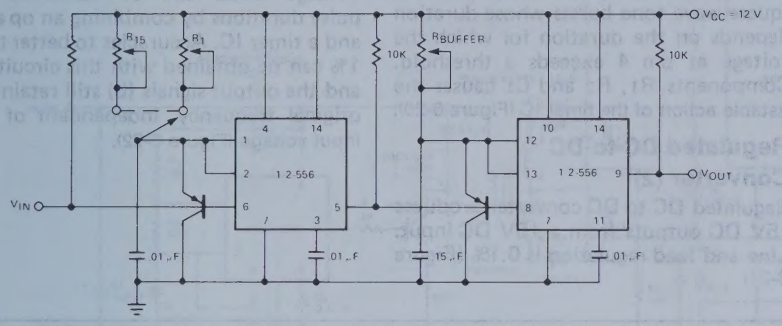


Figure 6-17a

OPERATING WAVE FORMS OF SPEED WARNING DEVICE

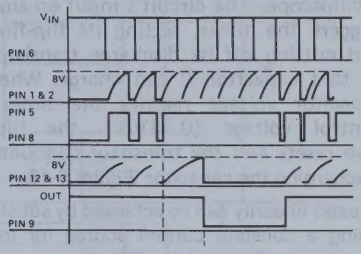


Figure 6-17b

TACHOMETER

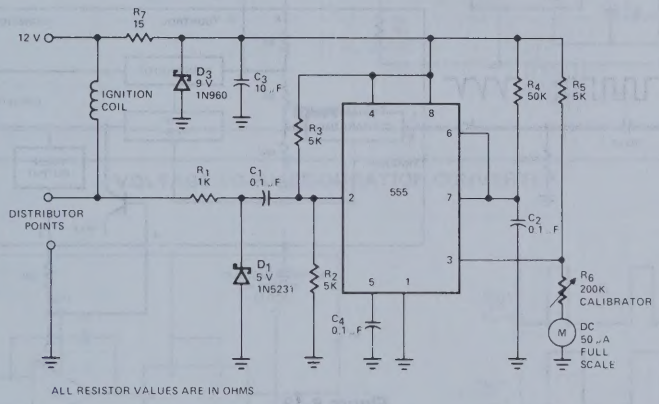


Figure 6-18

Oscilloscope Triggered Sweep

The 555 timer holds down the cost of adding a triggered sweep to an economy oscilloscope. The circuit's input op amp triggers the timer, setting its flip-flop and cutting off its discharge transistor so that capacitor C can charge. When capacitor voltage reaches the timer's control voltage (0.33Vcc), the flip-flop resets and the transistor conducts, discharging the capacitor (Figure 6-19).

Greater linearity can be achieved by substituting a constant current source for the frequency adjust resistor (R).

Square Wave Tone Burst Generator (4)

Depressing the pushbutton provides square-wave tone bursts whose duration depends on the duration for which the voltage at pin 4 exceeds a threshold. Components R_1, R_2 and C_1 causes the astable action of the timer IC (Figure 6-20).

Regulated DC-to-DC Converter (2)

Regulated DC to DC converter produces 15V DC outputs from a +5V DC input. Line and load regulation is 0.1% (Figure 6-21).

Voltage to Pulse Duration Converter (1)

Voltage levels can be converted to pulse durations by combining an op amp and a timer IC. Accuracies to better than 1% can be obtained with this circuit (a) and the output signals (b) still retain the original frequency, independent of the input voltage (Figure 6-22).

SCHEMATIC OF TRIGGERED SWEEP

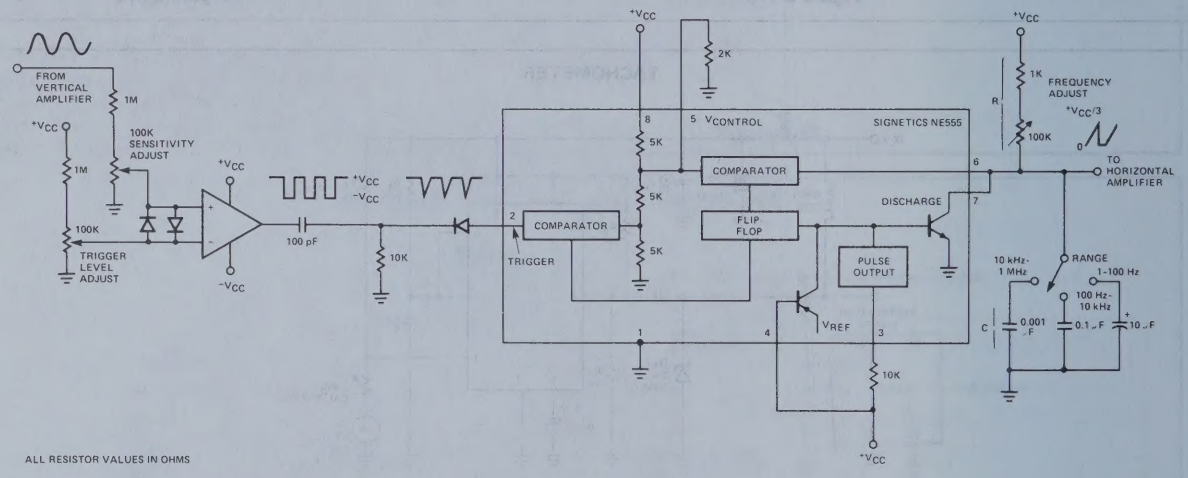


Figure 6-19

SQUARE WAVE TONE BURST GENERATOR

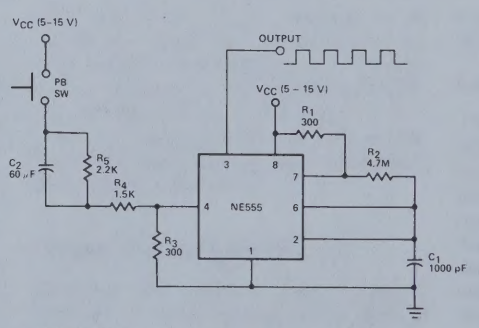


Figure 6-20

REGULATED DC TO DC CONVERTER

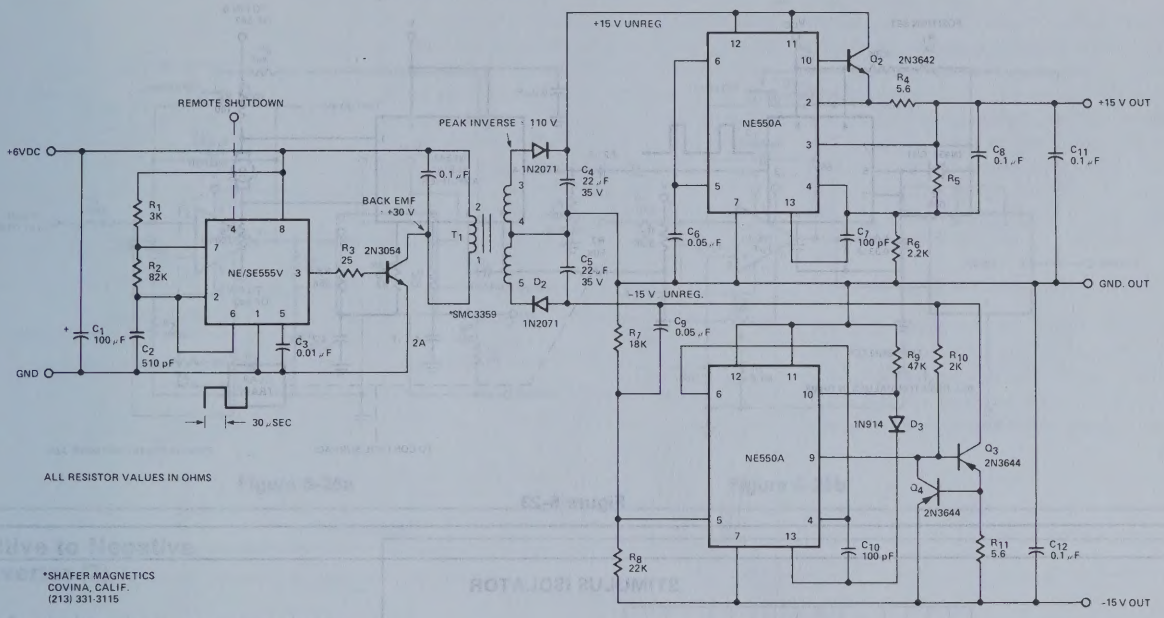


Figure 6-21

VOLTAGE-TO-PULSE-DURATION CONVERTER

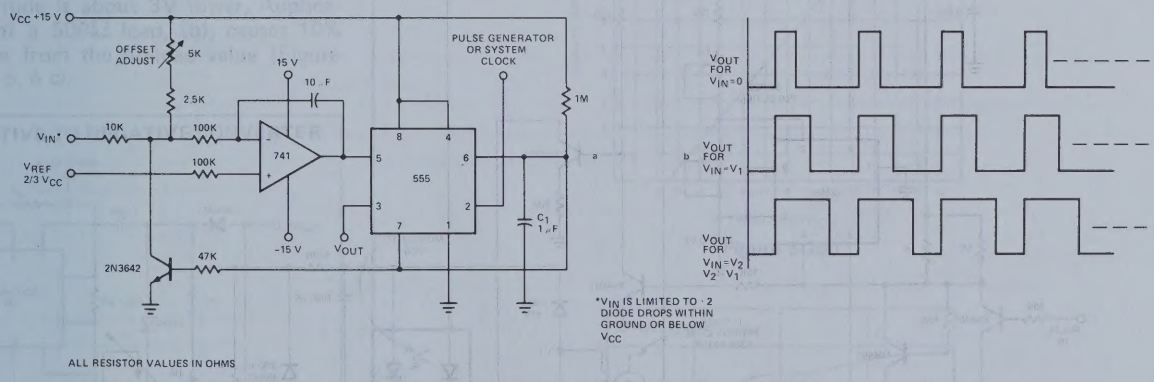


Figure 6-22

Servo System Controller (1)

To control a servo motor remotely, the 555 needs only six extra components (Figure 6-23).

Stimulus Isolator (5)

Stimulus isolator uses a photo-SCR and a toroid for shaping pulses of up to 200V at 200μA (Figure 6-24).

Voltage to Frequency Converter (0.2% Accuracy) (6)

Linear voltage-to-frequency converter (a) achieves good linearity over the 0 to −10V. Its mirror image (b) provides the same linearity over the 0-to+10V range but is not DTL/TTL compatible (Figure 6-25a & b.)

SERVO SYSTEM CONTROLLER

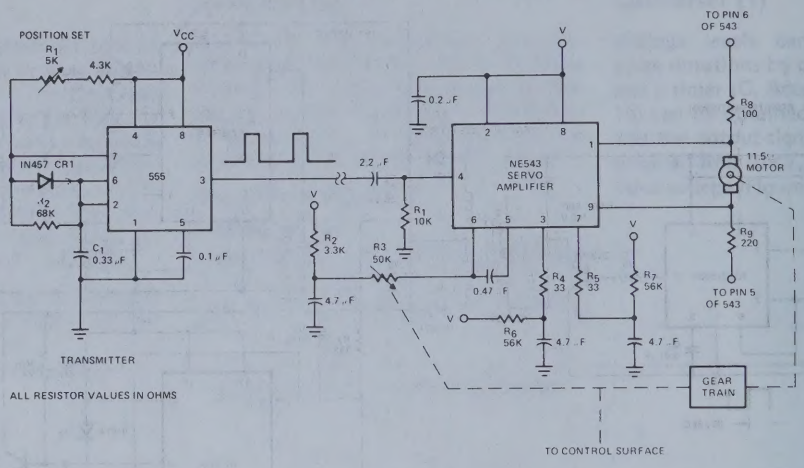


Figure 6-23

STIMULUS ISOLATOR

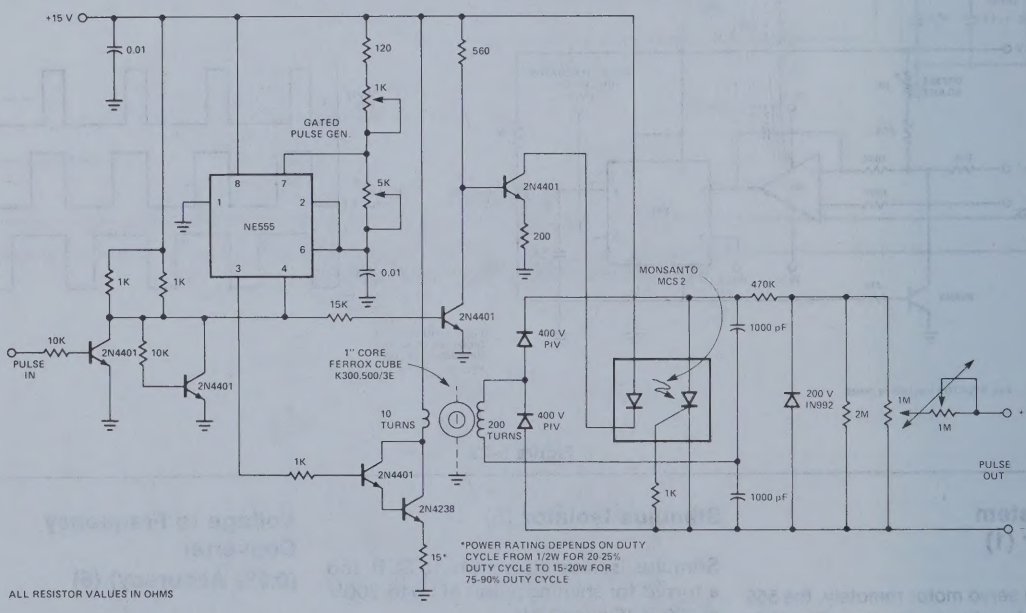


Figure 6-24

VOLTAGE-TO-FREQUENCY CONVERTER (0.2% ACCURACY)

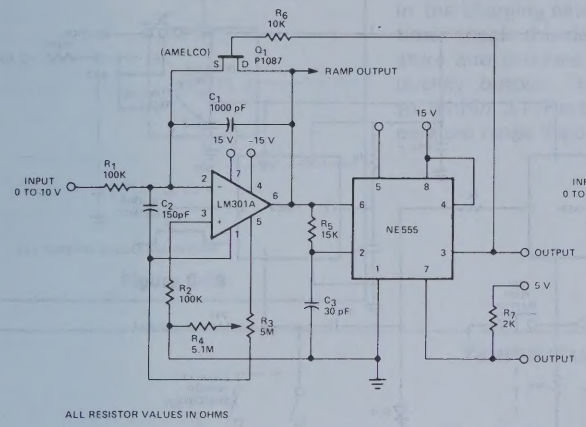


Figure 6-25a

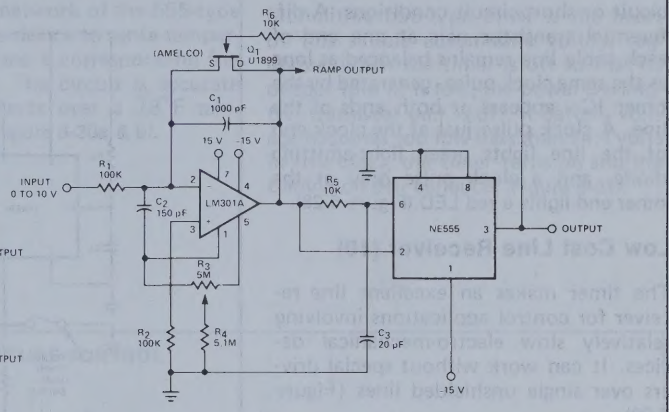


Figure 6-25b

Positive to Negative Converter (7)

Transformerless dc-dc converter derives a negative supply voltage from a positive. As a bonus the circuit also generates a clock signal.

The negative output voltage tracks the dc input voltage linearity (a), but its magnitude is about 3V lower, Application of a 500Ω load, (b), causes 10% change from the no-load value (Figure 6-26a, b, & c).

POSITIVE TO NEGATIVE CONVERTER

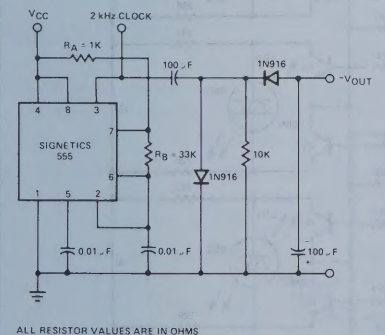


Figure 6-26a

Auto Burglar Alarm (8)

Timer A produces a safegaurd delay, allowing driver to disarm alarm and eliminating vulnerable outside control switch. The SCR prevents timer A from triggering timer B, unless timer B is triggered by strategically located sensor switches (Figure 6-27).

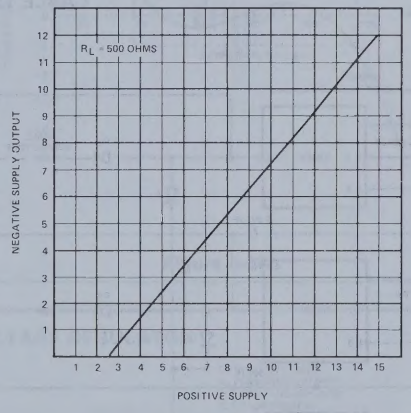


Figure 6-26b

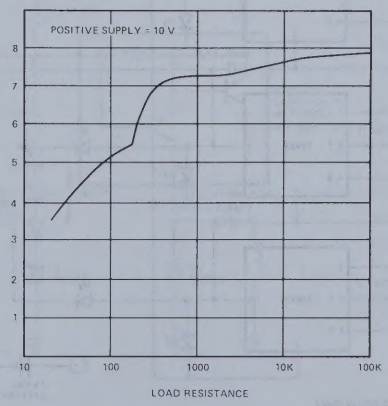


Figure 6-26c

Cable Tester (9)

Compact tester checks cables for open-cicuit or short-circuit conditions. A differential transistor pair at one end of each cable line remains balanced as long as the same clock pulse - generated by the timer IC - appears at both ends of the line. A clock pulse just at the clock end of the line lights green light-emitting diode; and a clock pulse only at the other end lights a red LED (Figure 6-28).

Low Cost Line Receiver (10)

The timer makes an excellent line receiver for control applications involving relatively slow electro-mechanical devices. It can work without special drivers over single unshielded lines (Figure 6-29).

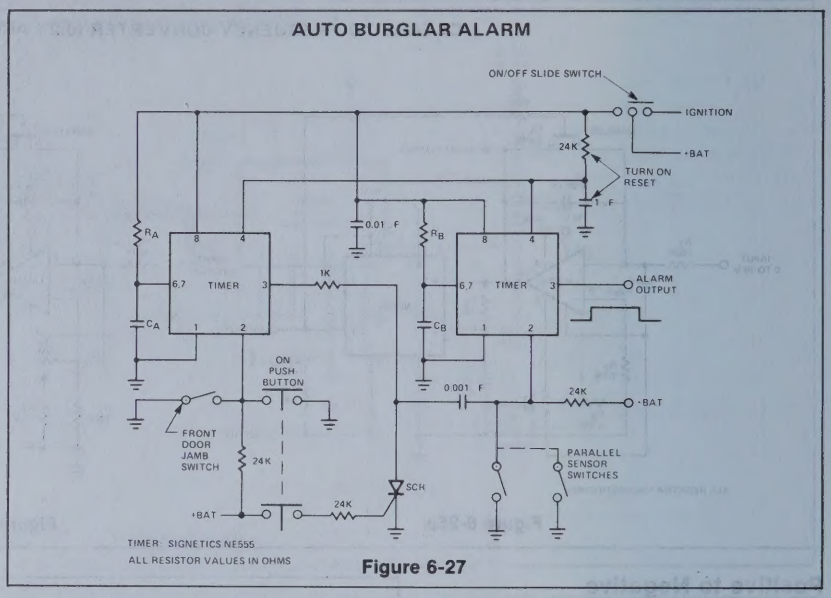


Figure 6-27

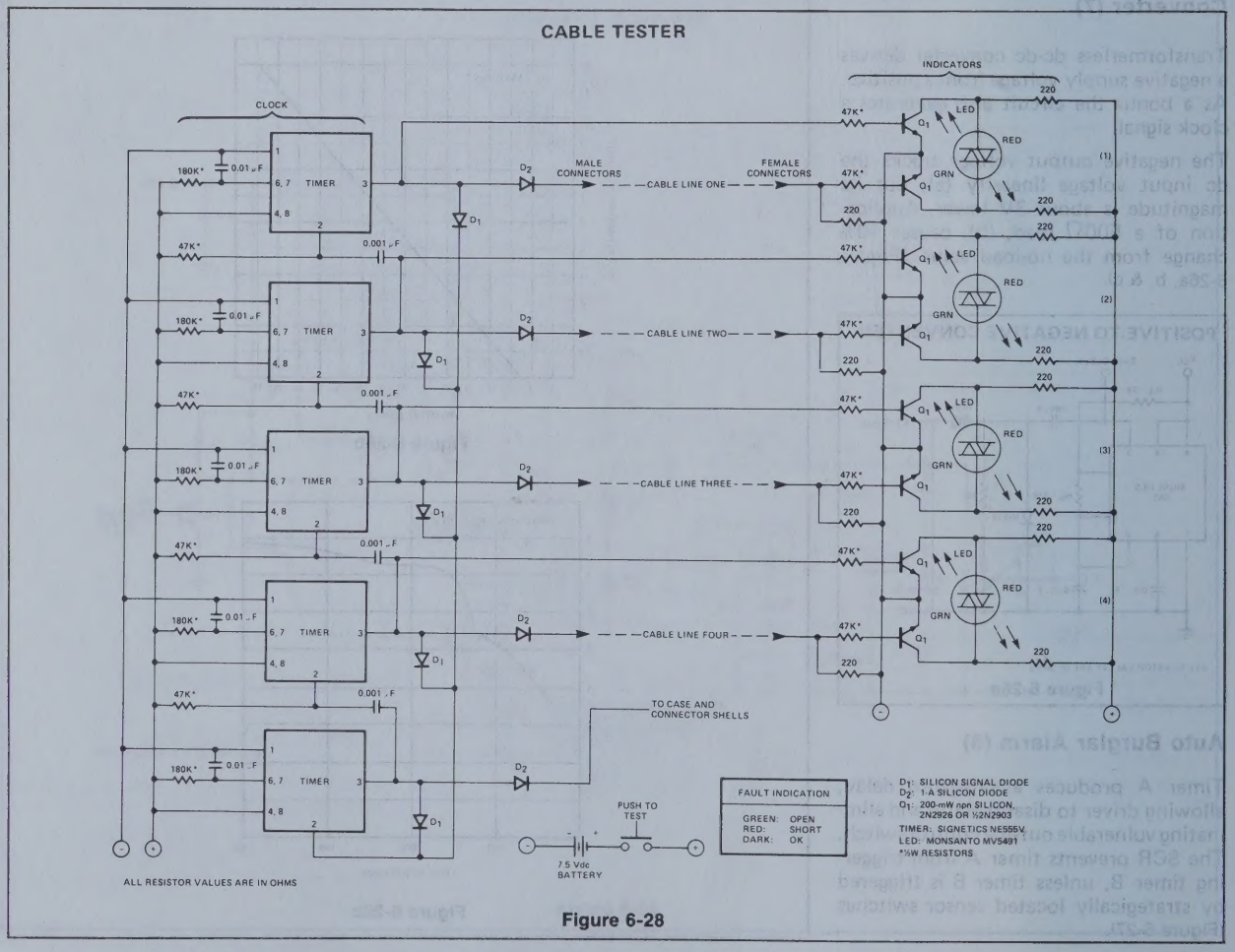


Figure 6-28

LOW COST LINE RECEIVER

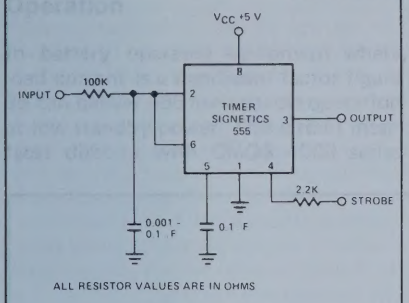


Figure 6-29

Temperature Control (11)

A couple of transistors and thermistor in the charging network of the 555-type timer enable this device to sense temperature and produce a corresponding frequency output. The circuit is accurate to within ±1 Hertz over a 78°F temperature range (Figure 6-30a & b).

Automobile Voltage Regulator (12)

Monolithic 555-type timer is the heart of this simple automobile voltage regulator. When the timer is off so that its output (pin 3) is low, the power Darlington transistor pair is off. If battery voltage becomes too low (less than 14.4 volts in this case), the timer turns on and the Darlington pair conducts (Figure 6-31).

TEMPERATURE CONTROL

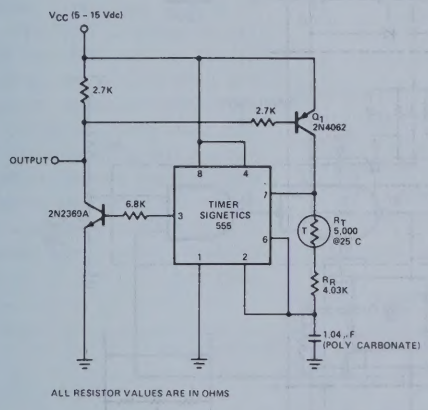


Figure 6-30a

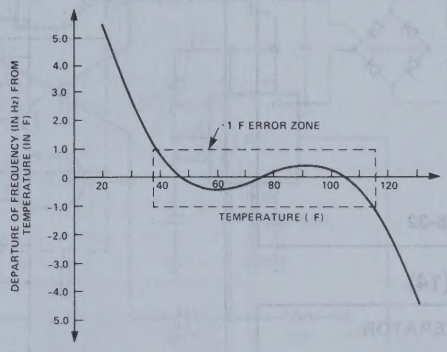


Figure 6-30b

AUTOMOBILE VOLTAGE REGULATOR

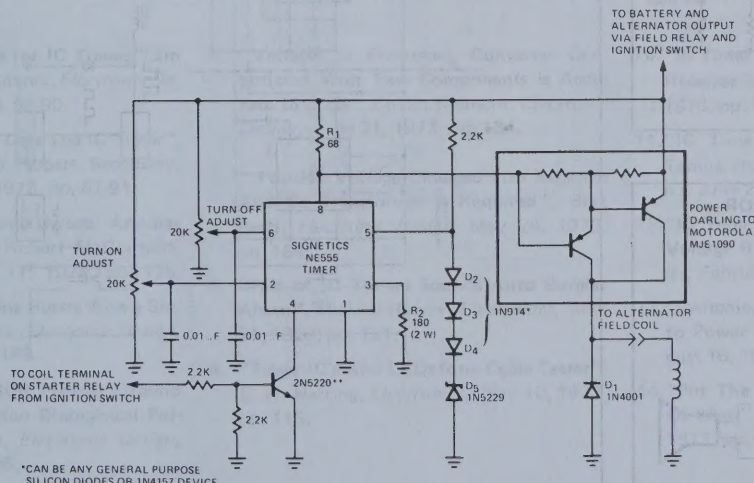


Figure 6-31

Switching Regulator (13)

The basic regulator of Figure 6-32 is shown here with its associated timing and pulse generating circuitry. The block diagram illustrates how the over-all regulator works. The multivibrator determines switching frequency, and the error amplifier adjusts the pulse width of the modulator to maintain output voltage at the desired level. The output resistor divider provides the sensing voltage. (Figure 6-35)

DC-to-DC Converter (14)

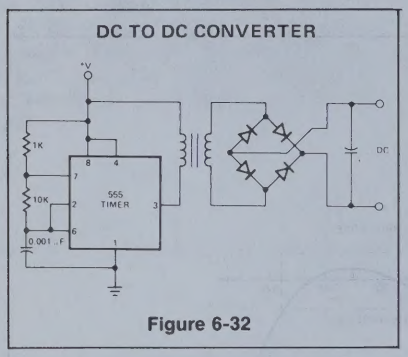


Figure 6-32

Ramp Generator (14)

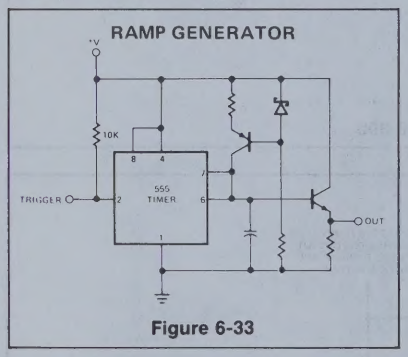


Figure 6-33

Audio Oscillator (14)

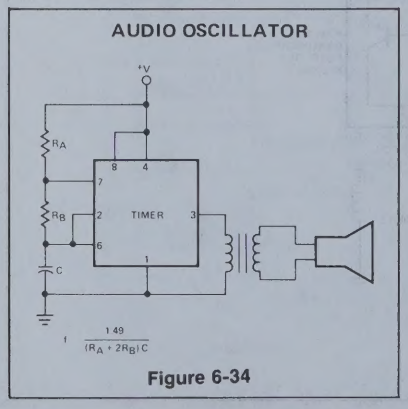


Figure 6-34

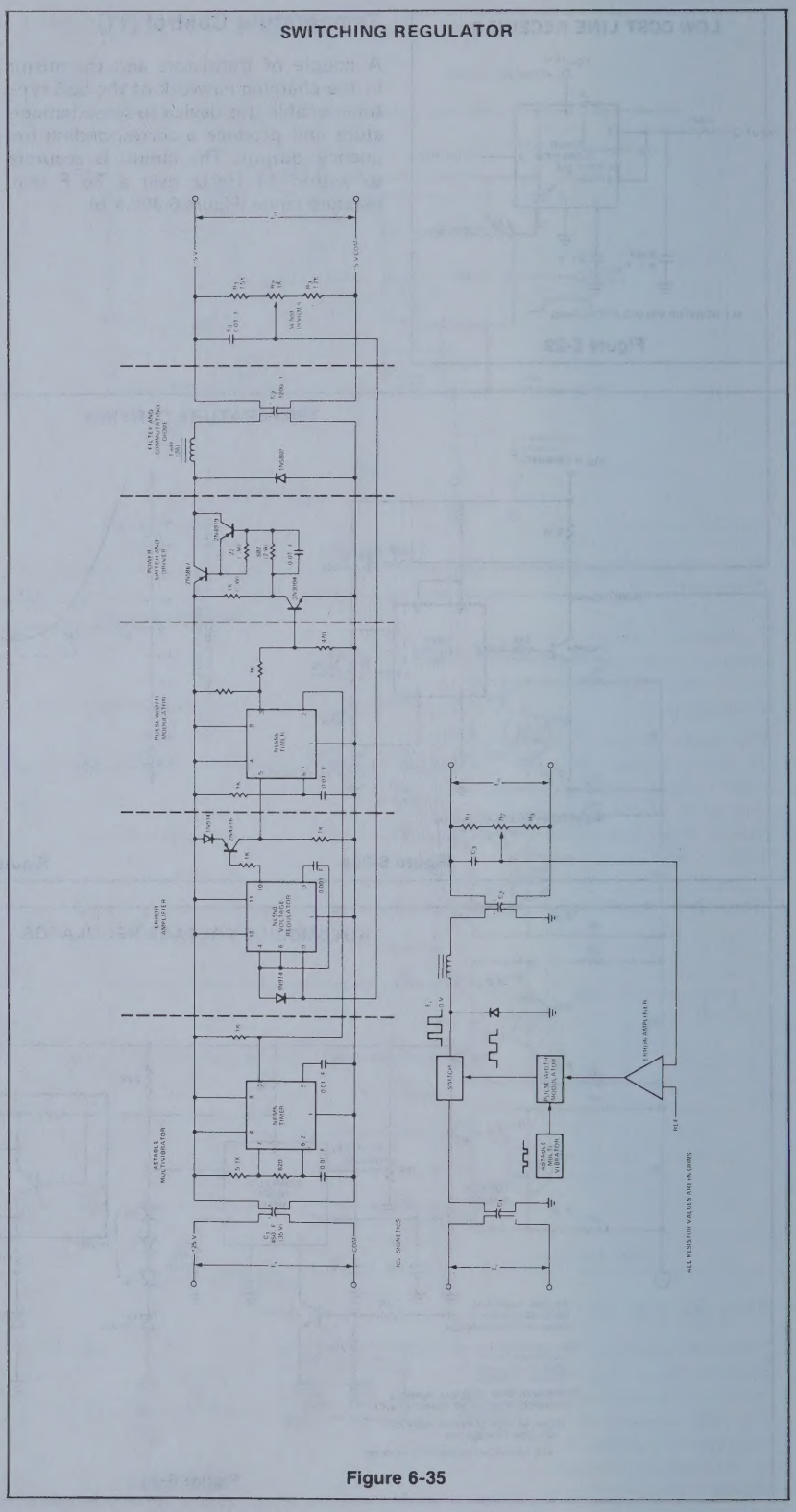


Figure 6-35

Low Power Monostable Operation

In battery operated equipment where load current is a significant factor figure 36 can deliver 555 monostable operation at low standby power. This circuit interfaces directly with CMOS 4000 series and 74L00 series. During the monostable time, the current drawn is 4.5mA for T = 1.1RC. The rest of the time the current drawn is less than 50μA. Circuit submitted by Karl Imhof, Executone Inc., Long Island City, NY.

In other low power operations of the timer where Vcc is removed until timing is needed, it is necessary to consider the output load. If the output is driving the base of a PNP transistor, for example, and its power is not removed, it will sink current into pin 3 to ground and use excessive power. Therefore, when driving these types of loads, one should recall this internal sinking path of the timer.

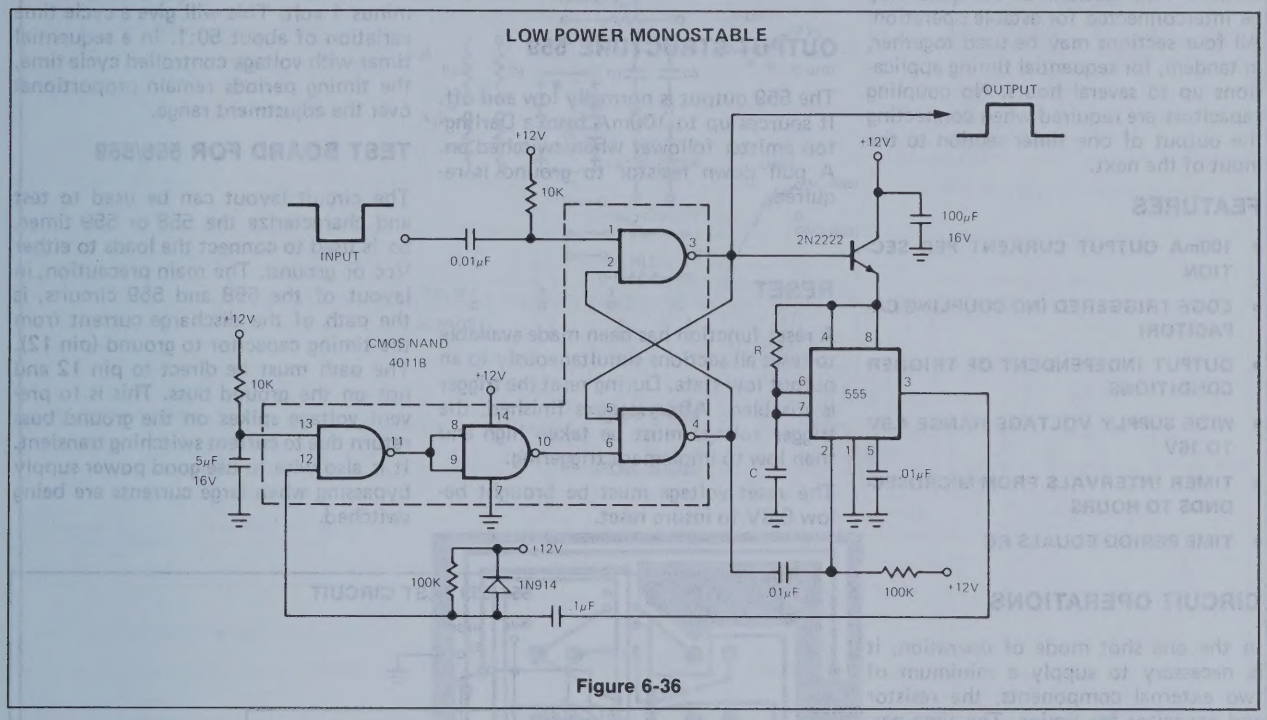


Figure 6-36

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4. **"Get Square Wave Tone Bursts With a Single Timer IC"**, Sol Black, *Electronic Design*, September 1973, pp. 148.
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13. **"Switching Regulators, The Efficient Way to Power"**, Robert Olla, *Electronics*, August 16, 1973, pp. 94-95.
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INTRODUCTION

The 558/559 are monolithic Quad Timers designed to be used in the timing range from a few microseconds to a few hours. Four entirely independent timing functions can be acheived, using a timing resistor and capacitor for each section. Two sections of the quad may be interconnected for astable operation. All four sections may be used together, in tandem, for sequential timing applications up to several hours. No coupling capacitors are required when connecting the output of one timer section to the input of the next.

FEATURES

- 100mA OUTPUT CURRENT PER SECTION
- EDGE TRIGGERED (NO COUPLING CAPACITOR)
- OUTPUT INDEPENDENT OF TRIGGER CONDITIONS
- WIDE SUPPLY VOLTAGE RANGE 4.5V TO 16V
- TIMER INTERVALS FROM MICROSECONDS TO HOURS
- TIME PERIOD EQUALS RC

CIRCUIT OPERATIONS

In the one shot mode of operation, it is necessary to supply a minimum of two external components, the resistor and capacitor for timing. The time period is equal to the product of R and C. An output load must be present to complete the circuit due to the output structure of the 558/559.

For astable operation, it is desireable to cross couple two devices from the 558/559 Quad. The outputs are direct coupled to the opposite trigger input. The duty cycle can be set by ratio of R_1C_1 to R_2C_2 from close to zero to almost 100%. An astable circuit using one timer is shown in Figure 6-41b.

OUTPUT STRUCTURE 558

The 558 structure is open collector which requires a pull-up resistor to Vcc and is capable of sinking 100mA per unit but not to exceed the power dissipation and junction temperature rating of the die and package. The output is normally low and is switched high when triggered.

OUTPUT STRUCTURE 559

The 559 output is normally low and off. It sources up to 100mA from a Darlington emitter follower when switched on. A pull down resistor to ground is required.

RESET

A reset function has been made available to reset all sections simultaneously to an output low state. During reset the trigger is disabled. After reset is finished, the trigger voltage must be taken high and then low to implement triggering.

The reset voltage must be brought below 0.8V to insure reset.

THE CONTROL VOLTAGE

The control voltage is also made available on the 558/559 timers. This allows the threshold voltage to be modulated, therefore controlling the output pulse width and duty cycle with an external control voltage. The range of this control voltage is from about 0.5V to Vcc minus 1 volt. This will give a cycle time variation of about 50:1. In a sequential timer with voltage controlled cycle time, the timing periods remain proportional over the adjustment range.

TEST BOARD FOR 558/559

The circuit layout can be used to test and characterize the 558 or 559 timer. S_2 is used to connect the loads to either Vcc or ground. The main precaution, in layout of the 558 and 559 circuits, is the path of the discharge current from the timing capacitor to ground (pin 12). The path must be direct to pin 12 and not on the ground buss. This is to prevent voltage spikes on the ground buss return due to current switching transient. It is also wise to use good power supply bypassing when large currents are being switched.

558/559 TEST CIRCUIT

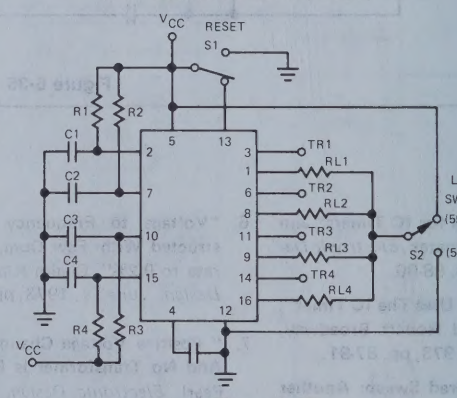


Figure 6-37

558/559 TEST BOARD LAYOUT

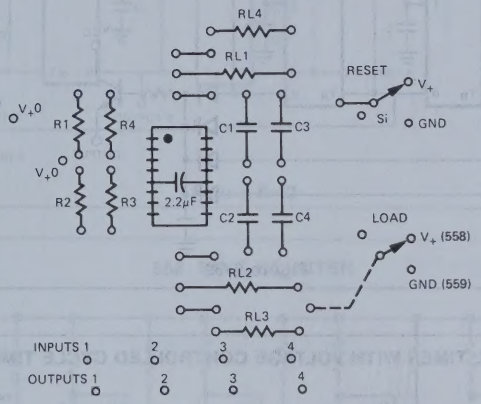


Figure 6-38a

FOIL SIDE

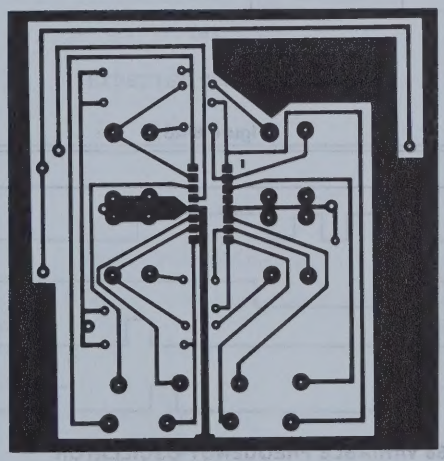
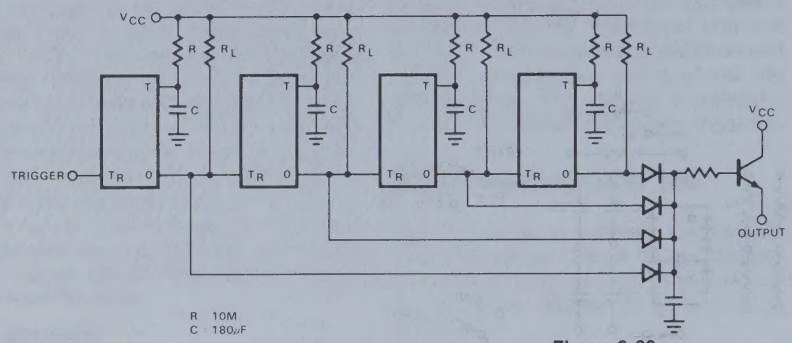


Figure 6-38b

558 TWO HOUR TIMER



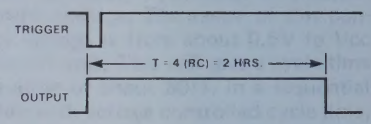
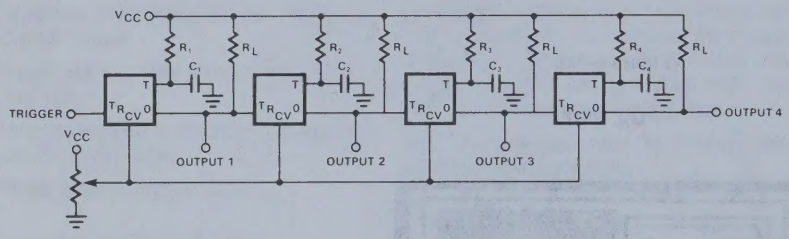
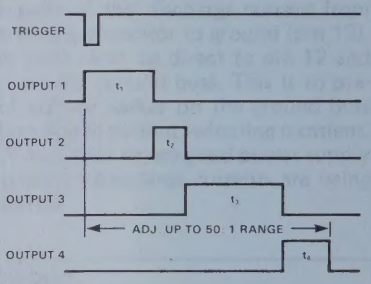


Figure 6-39

558 SEQUENTIAL TIMER WITH VOLTAGE CONTROLLED CYCLE TIME (50:1 RANGE)

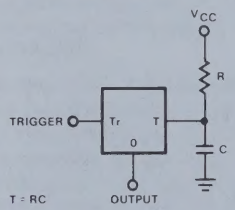




NOTE
t_1, t_2, t_3, t_4 remain proportional over entire adj. range.

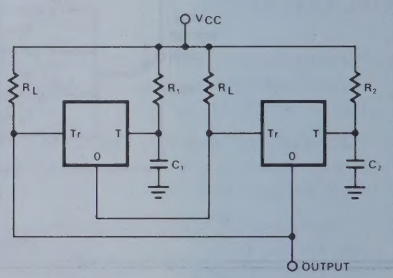
Figure 6-40

MONOSTABLE OPERATION (ONE SHOT)



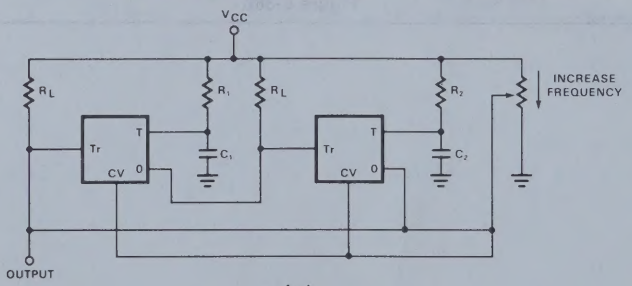
(a)

558 ASTABLE OPERATION (OSCILLATOR)



(b)

558 VARIABLE FREQUENCY OSCILLATOR WITH FIXED DUTY CYCLE



(c)

Figure 6-41

558 LONG-TIME DELAY

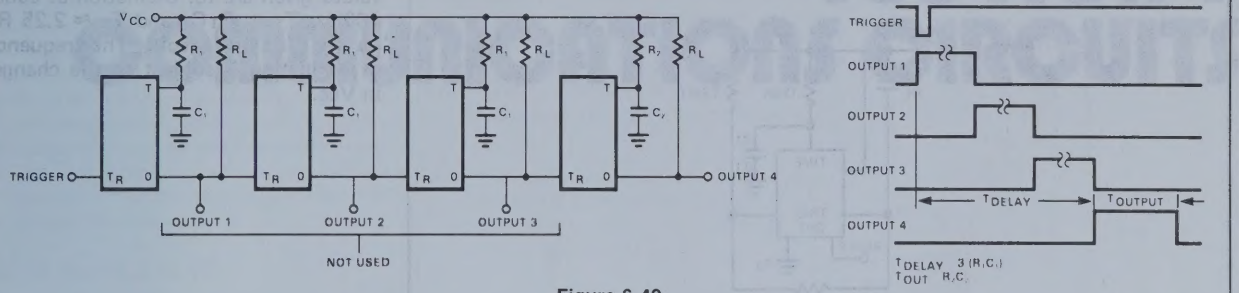
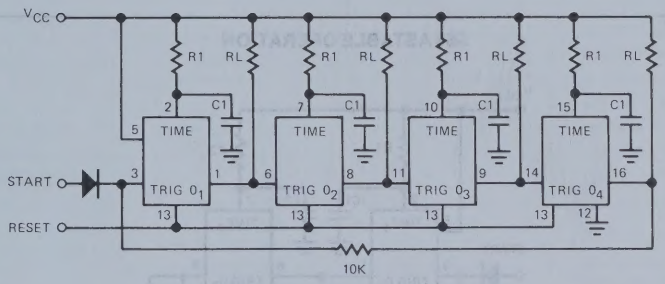


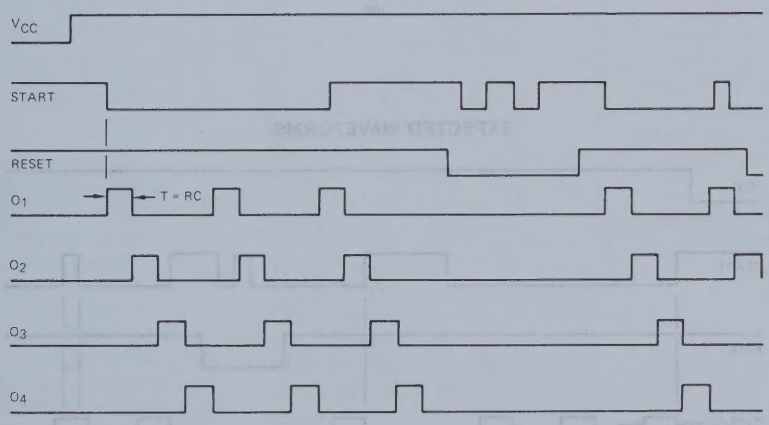
Figure 6-42

558 RING COUNTER



(a)

EXPECTED WAVEFORMS



(b)

Figure 6-43

APPLICATIONS

A single section of the Quad time may be used as a non precision oscillator. The values given are for oscillation at about 400Hz. $T_1 \approx R_1 C_1$ and $T_2 \approx 2.25\ R_2\ C_2$ for Vcc of 15 volts. The frequency of oscillation is subject to the changes in Vcc.

NE558 400 Hz SQUARE WAVE OSCILLATOR

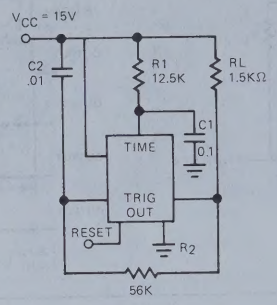
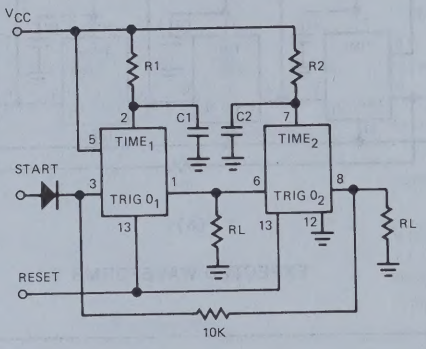


Figure 6-44

559 ASTABLE OPERATION



EXPECTED WAVEFORMS

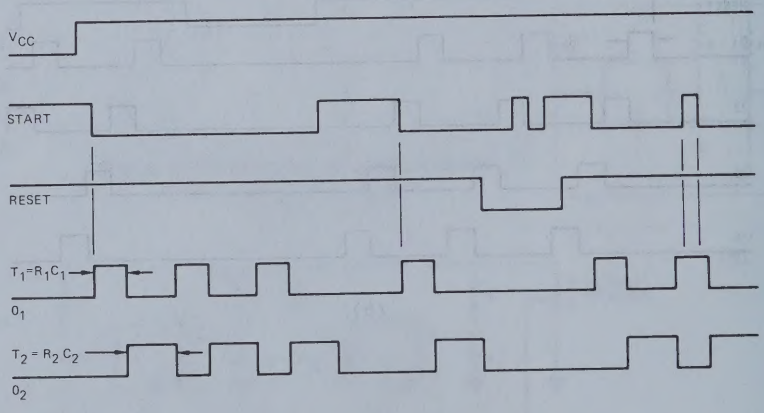


Figure 6-45

SECTION 7
COMMUNICATIONS CIRCUITS

INTRODUCTION

The following chapter will cover those devices which can be referred to as communications circuits. Such devices as balanced modulators, RF/IF amplifiers, and video amplifiers are included. Many other devices such as the ULN2111 partially fit the communication heading but also fit the consumer category since they are intended primarily for the home entertainment market. These devices will be covered in detail in the consumer section.

RF/IF AMPLIFIERS

Ideally, semiconductor devices for use in the RF amplifiers should have a high forward transconductance and a low reverse transadmittance, that is, low feedback capacitance. A single transistor may have a high transconductance, but it will also have high reverse transadmittance, making it difficult to fully utilize its high tranconductance in a tuned amplifier.

DIFFERENTIAL AMPLIFIER

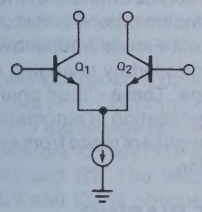


Figure 7-1

There are two multiple transistor circuit configurations available that allow the reduction of the reverse transadmittance. The first circuit, Figure 7-1, is basically a differential amplifier with a high impedance emitter coupling circuit (a current generator). Rearranging the circuit and adding a source, load, and ground result in the circuit of Figure 7-2. The input stage is common collector and the output stage is common base. Therefore, the currents in the collector to base capacitance of the input stage are completely isolated from the input stage. The reverse transadmittance then consists primarily of the stray capacitive reactance occurring in the package in which the device is encased. Figure 7-3 shows the circuit with suitable biasing applied.

The second circuit, Figure 7-4, is a series transistor connection. When a source and loading are incorporated, it is apparent that this is a common emitter-common base connection, commonly called a "cascode" circuit. Again, as in the circuit of Figure 7-3, the currents in the collector to base capacitance of the output stage are completely isolated from the input circuitry. The currents in the collector to base capacitance of the input stage do not flow directly to ground as in the circuit of Figure 7-3 and some feedback does occur. However, it is negligible because the collector of the first stage is heavily loaded by the emitter of the second stage. Therefore, very little feedback voltage may be developed across it. Figure 7-6 shows the circuit as it might be used. It has a gain capability greater than the circuit of Figure 7-3.

REARRANGEMENT SHOWING COMMON COLLECTOR-COMMON BASE STAGES

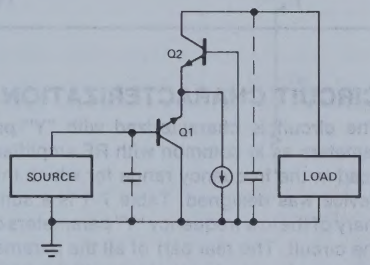


Figure 7-2

COMMON COLLECTOR-COMMON BASE STAGE WITH BIASING

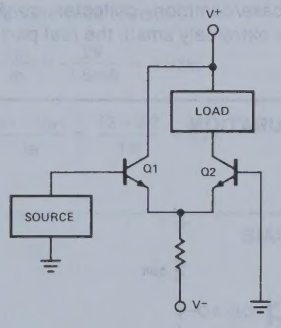


Figure 7-3

COMMON EMITTER-COMMON BASE AMPLIFIER

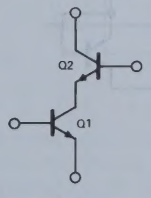


Figure 7-4

REARRANGEMENT SHOWING LOADS AND PARASITIC ELEMENTS

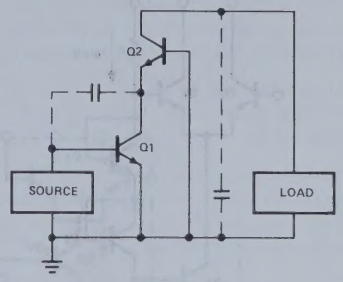


Figure 7-5

In most RF/IF amplifiers, the circuit designer wishes to operate from a single power supply. To permit this method of operation, a bias must be supplied for the bases of transistors Q1 and Q2.

This bias is obtained by inserting two more diodes, D1 and D2, in a series with the bias current resistor R, of Figure 7-7. Two diodes are used to ensure that if either of the transistors, Q1 or Q2, should become saturated the voltage cannot fall low enough to disturb the operation of the current generator.

COMMON EMITTER-COMMON BASE AMPLIFIER WITH BIASING

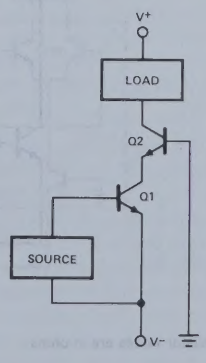


Figure 7-6

ADDITIONAL BIASING TECHNIQUE

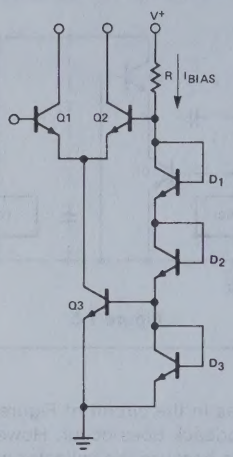


Figure 7-7

DC AND LOW FREQUENCY PARAMETERS

PARAMETER	CC-CB		CE-CB		Unit
	V+ = 6 V	V+ = 12 V	V+ = 6 V	V+ = 12 V	
Bias Network Current	1.5	3.2	1.5	3.2	mA
Quiescent Input Current	25	50	50	100	μA
Quiescent Output Current	0.6	1.4	1.2	2.8	mA
Input Conductance (Y_{11})	0.25	0.4	1.0	2.0	mmho
Output Conductance (Y_{22})	0.01	0.01	0.01	0.01	mmho
Input Capacitance	4.0	4.5	8	10	pF
Output Capacitance	3.0	2.5	3.0	2.5	pF
Feedback Capacitance	0.1	0.1	0.1	0.1	pF
Forward Transconductance (Y_{21})	11	21	45	75	mmho

Table 7-1

The final circuit design is shown in Figure 7-8. The transistors used are of small geometry and have an F_T of about 700MHz.

As shown the NE510 and NE511 configurations are quite similar. The emitters of the current sources are brought out for the 511 so that degeneration may be introduced for better signal handling capability and linearity.

CIRCUIT CHARACTERIZATION

The circuit is characterized with "Y" parameters as is common with RF amplifiers used in the frequency range for which this device was designed. Table 7-1 is a summary of the low frequency "Y" parameters of the circuit. The real part of all the parameters remains nearly constant until the operating frequency exceeds 10MHz, at which time input and output conductances start to rise and the forward transconductance starts to fall.

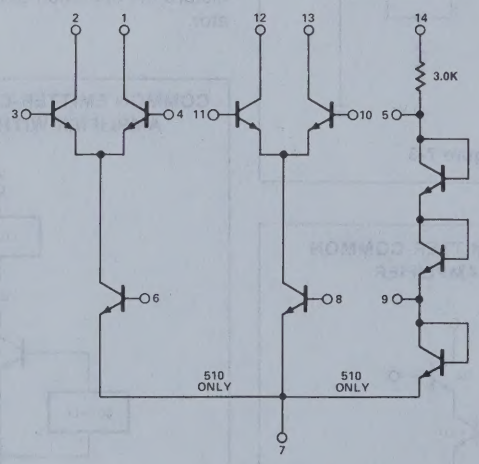
The reverse transconductance of both the common emitter/common base and common base/common collector configurations is extremely small, the real part being negligible while the imaginary part corresponds to a capacitance of less than 0.1 pico Farad.

Table 7-1 shows that the forward transconductance, Y21, of both configurations is a function of power supply voltage. A plot of Y21 versus bias network current for the common collector—common base configuration, Figure 7-9, shows that the Y21 is directly proportional to the bias current. A plot of Y21 versus differential input voltage of the common emitter—common collector configuration, Figure 7-10, shows that Y21 may be controlled by changing differential input voltage. These circuit characteristics allow the application of automatic gain control to RF amplifiers made from either circuit configuration.

CIRCUIT BIASING

Since this circuit is completely devoid of resistors and bias networks, their selection

FINAL CIRCUIT CONFIGURATION OF NE510/511



All resistor values are in ohms

Figure 7-8

TRANSCONDUCTANCE vs BIAS CURRENT

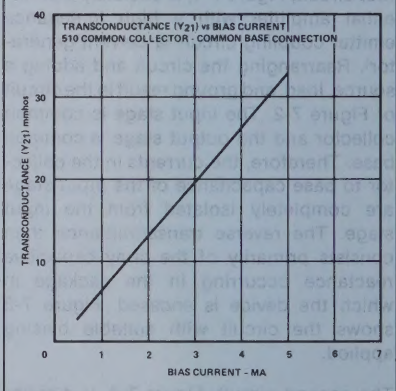


Figure 7-9

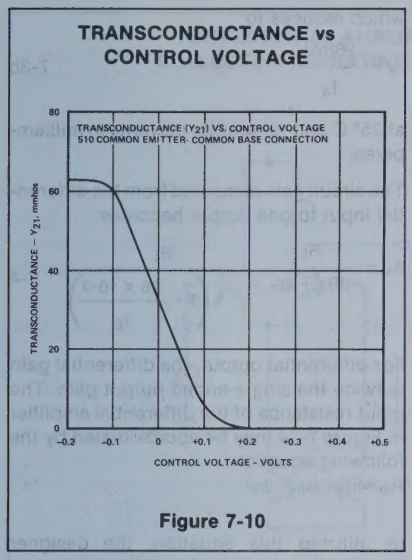


Figure 7-10

is at the discretion of the user. This allows the circuit designer complete freedom of choice in operating parameters and transistor interconnections. The only constraints are the absolute maximum ratings of the device; for example, applied voltage, current, junction temperature, etc.

A typical bias connection, option No. 1, is given in Figure 7-11. Operating currents are determined by the voltage between the base of the transistors Q1 and Q2 and V−, and resistors R1 and R2. The voltage for the bases of Q1 and Q2 is obtained from the temperature compensated voltage divider consisting of R3, R4, and diode D1. Including D1 in the bias network compensates for the temperature coefficient of the base-emitter voltage of Q1 and Q2. The current in the voltage divider should be approximately 75% of the emitter current of Q1 and Q2. Should it become necessary for the collector currents of Q1 and Q2 to be unequal but of the same order of magnitude, then it is suggested that the voltage divider current be selected as the average of the emitter currents. A design example is as follows:

1. Assume operating currents of 2mA for I_{C1} and I_{C2}.
2. Assume V− is at ground and V+ at +12 volts.
3. Assume that the design requires that resistors R1 and R2 be 1000ohms.
4. Calculate the voltage at the emitters and the bases of Q1 and Q2.

$V_{E1} = V_{E2} = I_{C1} \times R_I = 1000\Omega \times 2mA = +2V$

$V_{B1} = V_{B2} = V_{E1} + V_{BE} = +2V + 0.7V$

$= +2.7V\ (T_a = 25°\ C)$

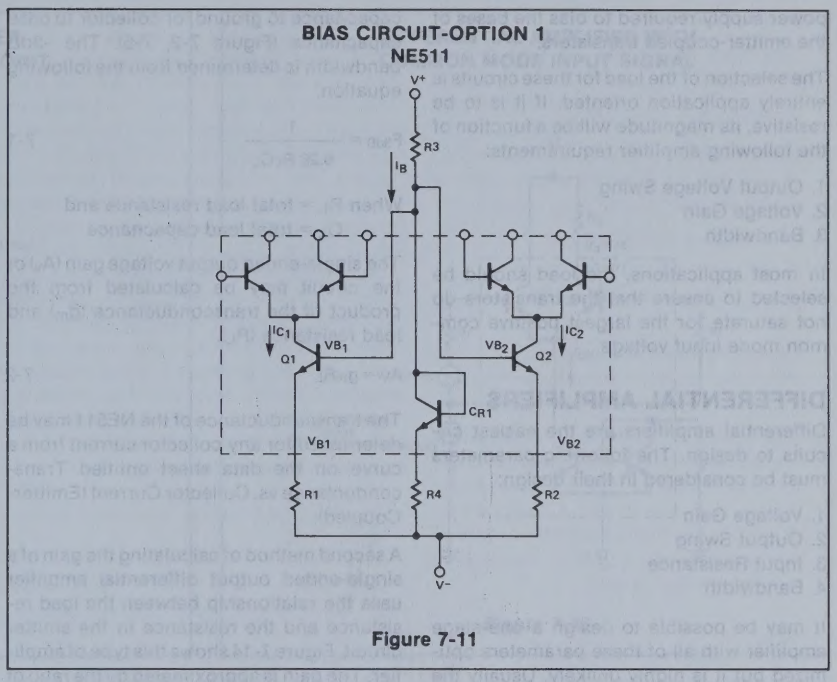


Figure 7-11

5. Calculate bias network current.

$I_B = 0.75 I_{C1}$, $I_{C2} = 0.75 \times 2mA = 1.5mA$

6. Calculate bias resistors.

$$R4 = \frac{V_{E1}}{I_B} = \frac{2V}{1.5mA} = 1.33k;$$

$$R3 = \frac{V^+ - V_{B1}}{I_B} = \frac{12 - 2.7}{1.5} = 6.2k$$

The bias diode is formed from a planar type transistor which has had its collector and base connected together. It may be operated in either the forward mode or in the reverse breakdown region as a 6.8V Zener diode. When used as a Zener diode, the operating current should be kept less than 10mA.

Figure 7-12, option No. 2, shows utilization of the diode in this mode to develop a third

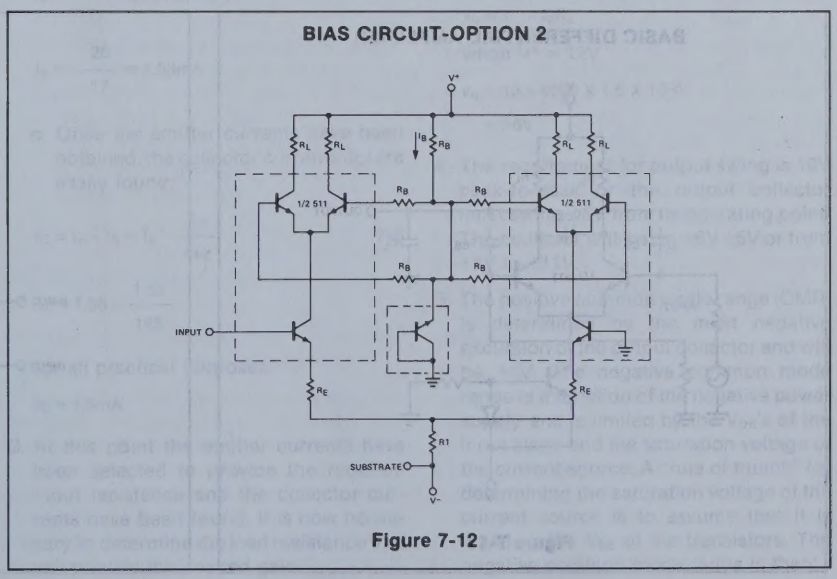


Figure 7-12

power supply required to bias the bases of the emitter-coupled transistors.

The selection of the load for these circuits is entirely application oriented. If it is to be resistive, its magnitude will be a function of the following amplifier requirements:

1. Output Voltage Swing
2. Voltage Gain
3. Bandwidth

In most applications, the load should be selected to ensure that the transistors do not saturate for the largest positive common mode input voltage.

DIFFERENTIAL AMPLIFIERS

Differential amplifiers are the easiest circuits to design. The following parameters must be considered in their design:

1. Voltage Gain
2. Output Swing
3. Input Resistance
4. Bandwidth

It may be possible to design a one-stage amplifier with all of these parameters optimized but it is highly unlikely. Usually the designs are a compromise of these parameters. For example, several cascaded stages may be required to obtain the desired gain. The gain and the output swing may have to be compromised so the required input resistance and bandwidth may be obtained.

Until bandwidths of greater than 10MHz are required, the bandwidth of the amplifier is determined solely by the RC time constant consisting of the load resistance and load capacitance, be it a discrete capacitor, stray capacitance to ground, or collector to base capacitance (Figure 7-2, 7-5). The -3dB bandwidth is determined from the following equation:

$$F_{3dB} = \frac{1}{6.28\ R_L C_L} \qquad 7\text{-}1$$

When R_L = total load resistance and
C_L = total load capacitance

The single-ended output voltage gain (A_V) of the circuit may be calculated from the product of the transconductance (g_m) and load resistance (R_L).

$$A_V = g_m R_L \qquad 7\text{-}2$$

The transconductance of the NE511 may be determined for any collector current from a curve on the data sheet entitled Transconductance vs. Collector Current (Emitter-Coupled).

A second method of calculating the gain of a single-ended output differential amplifier uses the relationship between the load resistance and the resistance in the emitter circuit. Figure 7-14 shows this type of amplifier. The gain is approximated by the ratio of the load resistance to the total resistance in the emitter circuit.

The resistance in the emitter circuit consists of the emitter contact and bulk resistance, R_E and the diffusion resistance, r_e. For the NE510/511, R_E is approximately 3 ohms per transistor and r_e is given by the following equation:

$$r_e = \frac{kT}{qI_e} \qquad 7\text{-}3a$$

which reduces to:

$$r_e = \frac{26mV}{I_e} \qquad 7\text{-}3b$$

at 25° C and for emitter currents in milliamperes.

The circuit gain measured from the differential input to one output becomes:

$$A_V = \frac{R_L}{2R_E + 2r_e} = \frac{R_L}{2\left(3 + \frac{26 \times 10^{-3}}{I_E}\right)} \qquad 7\text{-}4$$

For differential output, the differential gain is twice the single-ended output gain. The input resistance of the differential amplifier in Figure 7-14 may be approximated by the following equation:

$R_{in} = h_{FE}(2R_E + 2r_e)$

In utilizing this equation, the designer should be cognizant of the fact that the h_{FE} and r_e will change as a function of temperature and emitter current. The h_{FE} is typically 125 for collector currents of 1mA (at 25° C). The output swing capability is determined by the power supply voltage available. The maximum power supply voltage is determined by the absolute maximum ratings of the collector to base voltage of the differential transistors. It is this voltage which sets the maximum peak-to-peak swing for non-inductive loads. To maximize the output swing, the collector current is set so that the quiescent output voltage is one-half of the positive supply voltage. A circuit example is Figure 7-15. If, however, the input signal is differential in nature with a common mode

BASIC DIFFERENTIAL AMPLIFIER

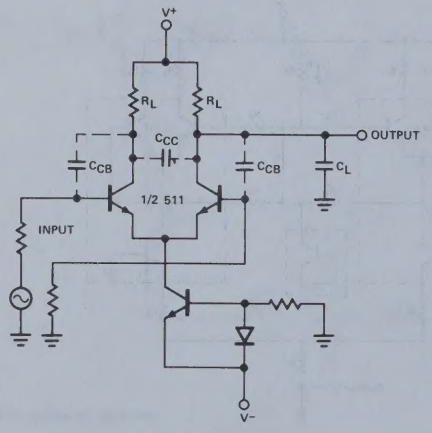


Figure 7-13

DIFFERENTIAL GAIN CALCULATIONS

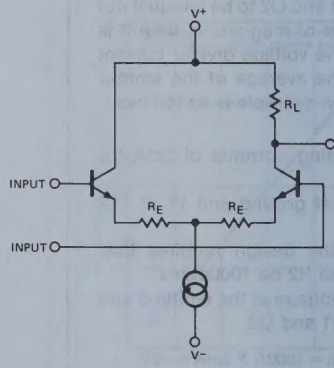


Figure 7-14

DIFFERENTIAL AMPLIFIER COLLECTOR OPERATING POINT

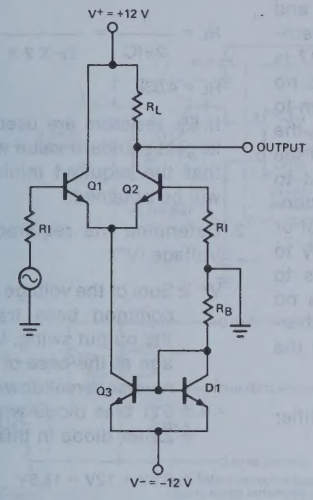


Figure 7-15

DIFFERENTIAL AMPLIFIER WITH COMMON MODE INPUT SIGNAL

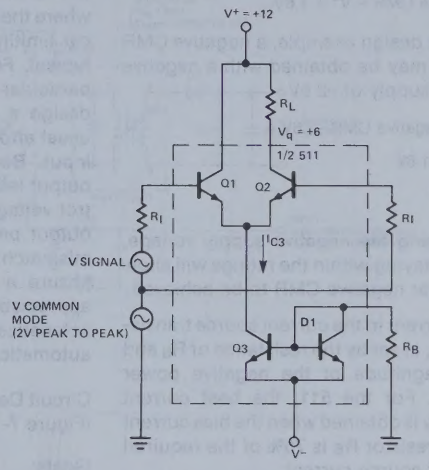


Figure 7-16

signal relative to ground, the collector operating point must be made more positive to allow for the common mode input signal if nonsymmetrical distortion is to be eliminated. For example, if the input signal is 10mV peak-to-peak riding a 2V common mode signal, the collector operating point must be raised according to the following equation:

$$V_O = \frac{V^+ + V_{cm}}{2} \qquad 7\text{-}5$$

When $V^+ = 12V$, $V_O = 7V$

The circuit of Figure 7-16 is a differential amplifier designed using the following design criteria.

Circuit Design Example: Differential Input, Single-Ended Output Amplifier

Goals:
1. Gain = 100
2. Output Swing = 10V peak-to-peak
3. Common Mode Range = ±1V
4. Input Resistance = 5000Ω

Assumptions:
1. $h_{FE} = 125$
2. Ambient Temperature (T_a) = 25° C

Solution:
1. The input resistance of a differential amplifier is set by the emitter currents of the transistors. Therefore, in order to obtain the required amplifier input resistance, the emitter currents must be determined first.

   a. Find r_e:

   $$R_{in} = h_{FE}(2R_E + 2r_e)$$

   $$r_e = \frac{R_{in}}{2h_{FE}} - R_E = \frac{5000}{2 \times 125} - 3\Omega$$

   $$r_e = 17\Omega$$

   b. Determine required emitter current to give desired r_e:

   $$I_e = \frac{26}{r_e} \text{ mA at } 25^\circ C$$

   $$I_e = \frac{26}{17} = 1.53mA$$

   c. Once the emitter currents have been obtained, the collector currents (I_C) are easily found:

   $$I_C = I_e - I_b = I_e - \frac{I_e}{h_{FE}} \qquad 7\text{-}6$$

   $$I_C = 1.53 - \frac{1.53}{125}$$

   for all practical purposes

   $$I_C \approx 1.5mA$$

2. At this point the emitter currents have been selected to provide the required input resistance and the collector currents have been found. It is now necessary to determine the load resistance that will provide the desired gain.

   The voltage gain

   $$(A_V) = \frac{R_L}{2R_E + 2r_e} \text{ or} \qquad 7\text{-}7$$

   $$R_L = 2A_V(R_E + r_e)$$
   $$= 2 \times 100\ (3 + 17)$$
   $$= 4000\Omega$$

3. Having determined the load resistance, we next determine the collector operating point, V_q.

   $$v_q = V^+ - I_C R_L$$

   when $V^+ = 12V$

   $$v_q = 12 - 4000 \times 1.5 \times 10^{-3}$$
   $$= +6V$$

4. The requirement for output swing is 10V peak-to-peak or the output collector must swing ±5V from its operating point. The collector will swing +6V ±5V or from +1V to +11V.

5. The positive common mode range (CMR) is determined by the most negative excursion of the output collector and will be +1V. The negative common mode range is a function of the negative power supply and is limited by the V_{be}'s of the input stage and the saturation voltage of the current source. A "rule of thumb" for determining the saturation voltage of the current source is to assume that it is equal to the V_{be} of the transistors. The negative common mode range is then:

Negative CMR = $V^- + 2V_{be}$

The V_{be}'s of the 511 are 0.8V or less, therefore:

Negative CMR = $V^- + 1.6V$.

For the design example, a negative CMR of -1V may be obtained with a negative power supply of -2.6V.

V^- = Negative CMR -1.6V

= -1V -1.6V

= -2.6V

Increasing the negative supply voltage, while staying within the ratings will allow a greater negative CMR to be achieved.

6. The current in the current source transistor, Q3, is set by the resistance of R_B and the magnitude of the negative power supply. For the 511, the best current stability is obtained when the bias current in the resistor R_B is 75% of the required current source current.

$$R_B = \frac{V^- - V_{be}}{0.75I_{c3}} = \frac{V^- - V_{be}}{1.5I_e} \qquad 7\text{-}8$$

For the design example where $V^+ = 12V$.

$$R_B = \frac{12 - 0.8}{1.5 \times 1.5 \times 10^{-3}}$$

$R_B \cong 5000\Omega$

CASCODE RF/IF AMPLIFIER (CE-CB)

The cascode configuration will be used where the maximum gain is required and where there is no requirement for symmetrical limiting. The circuit of Figure 7-17 is typical. For frequencies below 10Mhz, no particular precautions need to be taken to design a stable amplifier, other than the usual efforts to isolate the output from the input. Because of the excellent input to output isolation and because the gain control voltage has little effect on the input or output parameters, it is not necessary to mismatch the interstage transformers to ensure a stable amplifier that shows no appreciable change in the bandwidth characteristics as the gain is adjusted by the automatic gain control voltage.

Circuit Design Example: Cascode Amplifier (Figure 7-18)

Goals:

1. Output Voltage Swing (V_O) = 12V peak-to-peak
2. Voltage Gain ≥ 10.
3. Bandwidth ≥ 2MHz (with 20pF capacitive load).

Assumptions:

1. Assume high h_{FE}'s (typically 125)
2. $T_a = 25°$ C

Solution:

1. Determine the maximum load resistance. It is a function of required bandwidth.

$$R_L = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 2 \times 10^6 \times 20 \times 10^{-12}}$$

$R_L = 4.03k$

If 5% resistors are used, a 3.6kΩ is the largest standard value which will ensure that the required minimum bandwidth will be obtained.

2. Determine the required Power Supply Voltage (V^+):

$V^+ \geq$ Sum of the voltage at the base of the common base transistor (Q2) and the output swing, V_o. The bias voltage at the base of Q2 is set by the reverse breakdown voltage of the 511 bias diode which is used as a Zener diode in this example.

$V^+ \geq 6.8V + 12V = 18.8V$

To allow for power supply fluctuations and measurement tolerances, use $V^+ = 20V$.

3. Determine the output collector current:

$$I_C = \frac{V^+ - V_q}{R_L} \qquad 7\text{-}9$$

where: V_q is the quiescent dc output level.

CE-CB CASCODE AMPLIFIER

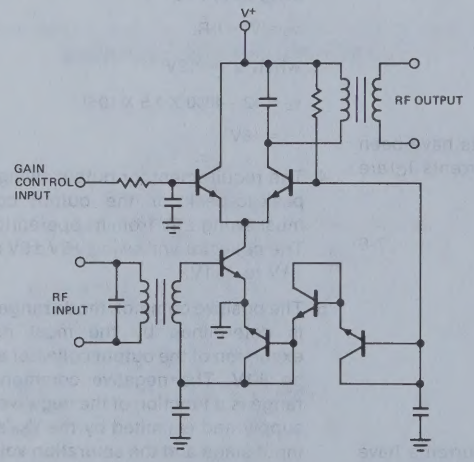
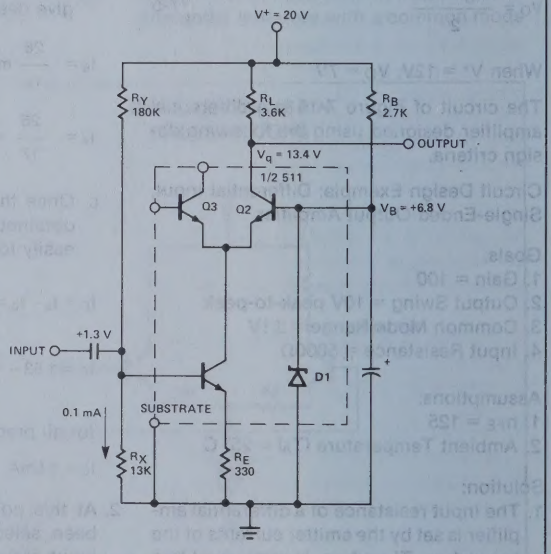


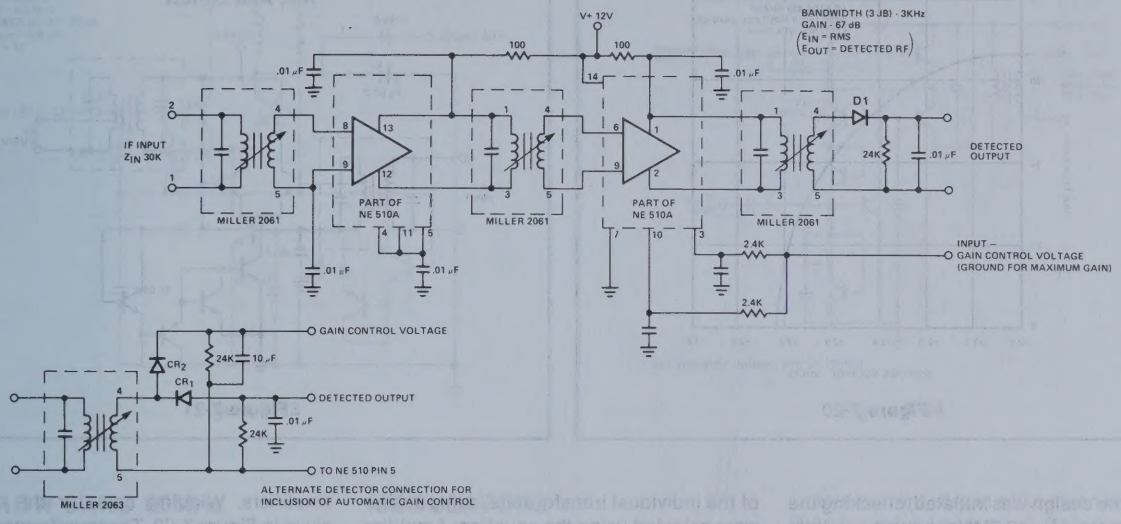
Figure 7-17

CASCODE AMPLIFIER



All resistor values are in ohms

Figure 7-18



All resistor values are in ohms

Figure 7-19

V_q = Power supply voltage minus one-half the possible output swing

$$V_q = V^+ - \left[\frac{V^+ - V_b}{2}\right] = 13.4V \qquad 7\text{-}10$$

therefore:

$$I_C = \frac{20V - 13.4V}{3600\Omega} = 1.83A$$

4. Determine the resistance of R_E:

   The voltage gain of the circuit is a function of the ratio of the load resistance to the resistance in the emitter circuit.

$$\text{Circuit Gain} = \frac{R_L}{R_E + r_e + r_c} \qquad 7\text{-}11$$

where: r_e is the diffusion resistance and is

$$\frac{26mV}{1.83mA}$$

$r_e = 14.2\Omega$, $T_a = 25°C$

r_c is the emitter contact resistance and is 3Ω.

Substituting in the circuit gain equation from above:

$$10 = \frac{3600}{R_E + 14.2 + 3}$$

$R_E = 360 - 17.2 = 343\Omega$.

5. Select the bias network resistors:
   a. The 511 data sheet shows that the bias diode, when operated in the reverse breakdown region, has a low dynamic resistance for currents up to 10mA. The bias current was arbitrarily set at 5mA, this being a point halfway between the knee of the curve and the 10mA limit.
   b. R_X and R_Y are selected to apply the appropriate bias at the base of Q1. This voltage is determined by the level which must appear across R_E to obtain the desired operating current and the base emitter voltage of Q1. In the example, the base voltage of Q1 is +1.3V. The voltage divider resistor is selected to provide this voltage when the input bias current is 10μA.

In the design, a number of approximations were made. In all but the most critical applications, this design technique will prove quite adequate.

An expansion of the cascode amplifier is the 455KHz IF strip shown in Figure 7-19.

This amplifier has been designed using "off the shelf" IF transformers. The circuit was built using the NE510 in a 14 dual in-line plastic package. The resulting amplifier has a voltage gain of 66dB when the gain control input is grounded. Gain, in this instance, is defined as a ratio of dc output voltage at the detector to RMS input voltage. Figure 7-20 is a curve of the gain versus gain control voltage. At the maximum gain setting, the input was set so that there was no output clipping and the dc output voltage was plus 2 volts.

10.7MHz LIMITING IF AMPLIFIER

An RF amplifier, using the NE510 in the common collector—common base configuration, is shown in Figure 7-21. Although the common collector/common base circuit has a lower gain than the common emitter/common collector configuration, it will prove extremely useful when a limiting amplifier is required. When it is operated in this configuration, an input level of 0.3 volts peak-to-peak will cause the maximum realizable output swing, and no further increase in the input signal level will affect the output. In addition, selecting the load impedance so that the output transistor can never saturate will ensure a limiter design having excellent characteristics with a minimum of phase distortion.

Figure 7-22 is a schematic of the IF amplifier using the circuit of Figure 7-21. The intent of the design is to demonstrate the device characteristics and the ease with which the circuit was designed and constructed. The IF frequency used in commercial FM broadcast receivers (10.7MHz) was selected for the IF frequency for this amplifier so that there would be a basis for comparison.

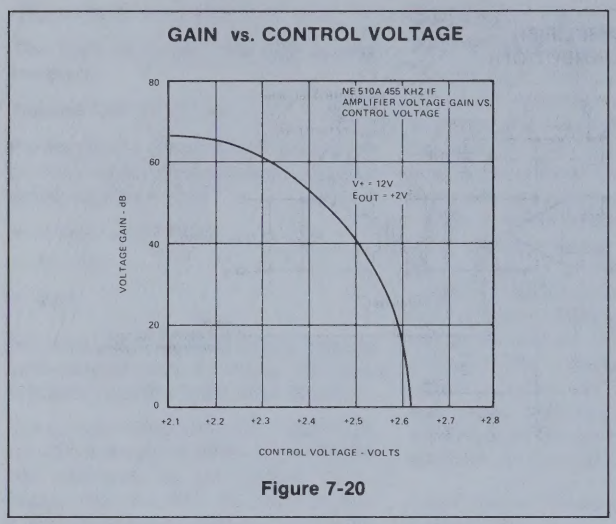


Figure 7-20

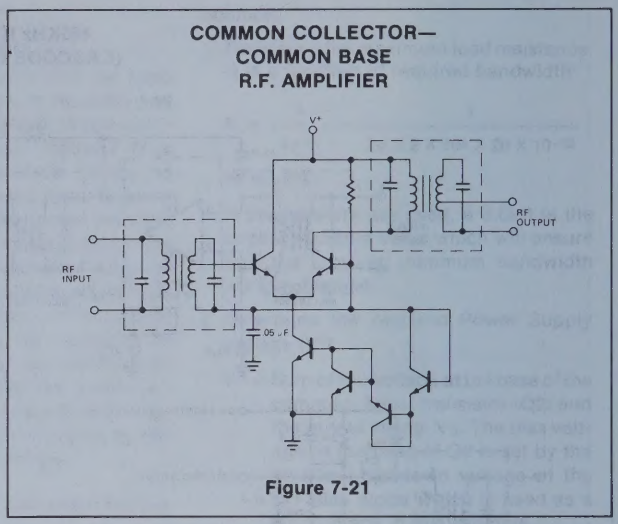


Figure 7-21

When the design was initiated, checking the Y parameters for 10.7MHz showed very little deviation from the dc and low frequency parameters. Since the feedback capacitance was very small, it was decided to use low frequency design techniques and not attempt to mismatch the coupling circuits. It was felt that if the design were made in this manner, and no instability problems occurred, the usefulness of the circuit would be proved. A typical commercial 10.7MHz IF amplifier has a 3dB bandwidth of 250 to 300KHz. It was decided to design this amplifier for 300KHz bandwidth. The bandwidths of the individual transformers in this design were selected using the equation: Amplifier Bandwidth (3dB) = Transformer Bandwidth (3dB) X $\sqrt{2^{1/n}-1}$ where "n" is the number of transformers. In our case, n = 3 and $\sqrt{2^{1/n}-1}$ = 0.5. Therefore, each transformer must have a bandwidth of 600KHz. In order to have transformers critically coupled and have a minimum saddle, the primary to secondary winding space is quite large, precluding the use of subminiature transformers for this first design. It was decided to use dual cup core transformers of the type used for many years in vacuum tube IF amplifiers. Winding data for the coils is given in Figure 7-22. The transformers used were taken from an old receiver and all the windings stripped and rewound. The transformers had a capacitance of about 12 picofarads in the base, so an additional 39 picofarads were added to the transformer externally to obtain the desired tuning capacitance.

The final amplifier designed had the desired bandwidth of 300KHz and full limiting was obtained with an input voltage at 70 microvolts RMS. No circuit prmblems appeared and tuning was not critical.

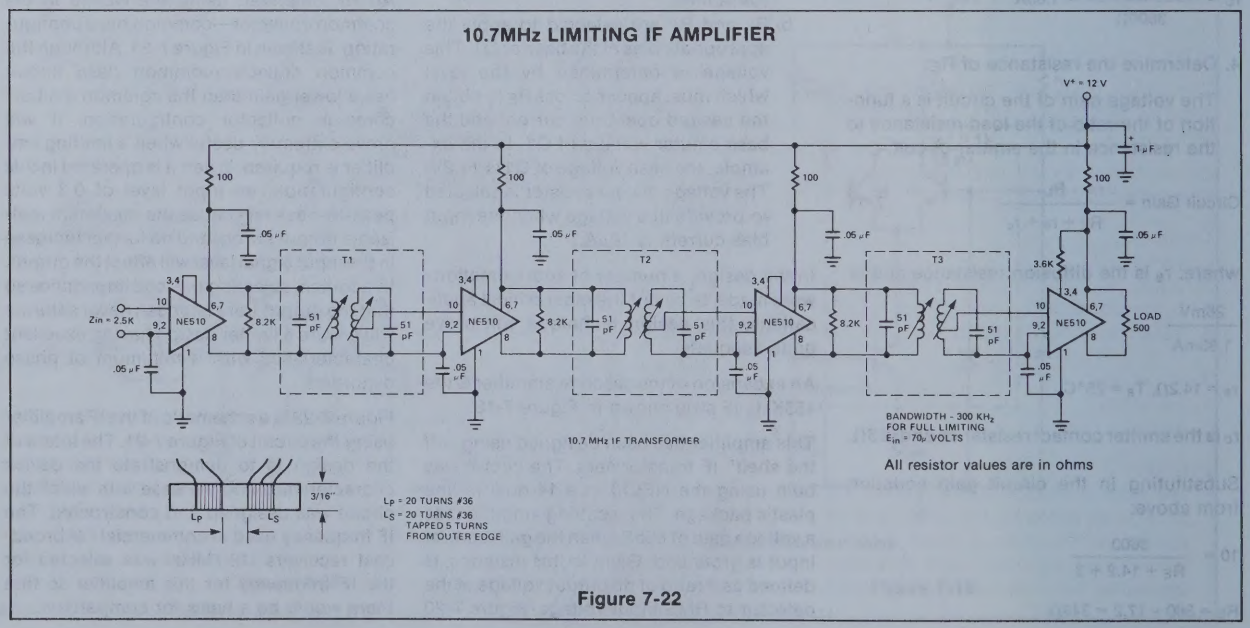


Figure 7-22

60MHz BAND PASS AMPLIFIER

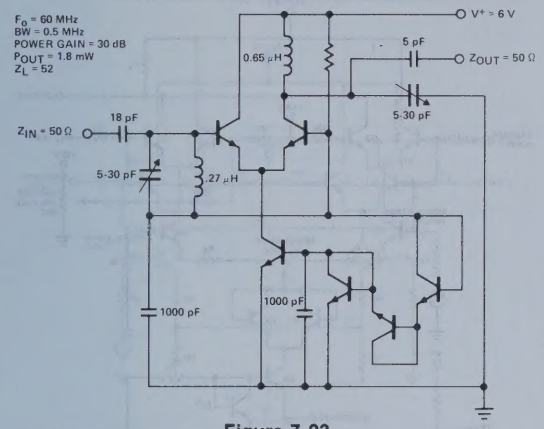
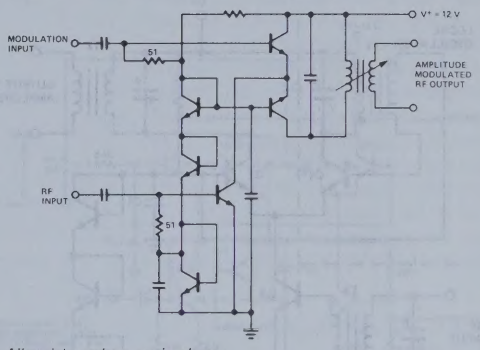


Figure 7-23

510 MODULATOR



All resistor values are in ohms

Figure 7-24

NARROW BAND 60MHz RF AMPLIFIER

The NE510/511 may be used for narrow band amplifiers with center frequencies well above 100MHz. As an example, an amplifier in the common collector—common base configuration, Figure 7-23, was designed with the following design objectives:

a. Power Gain—maximize
b. Center frequency—60MHz
c. Bandwidth (3dB)—0.5MHz
d. Power supply—+6 volts
e. Input impedance—50 ohms
f. Output impedance—50 ohms

The Y parameters for 60MHz, as read from the curves in the Appendix, are as follows:

$Y_{11} = 0.36 + j1.5 = 1.54 \angle 76.5°$
$Y_{22} = .03 + j1.1 = 1.1 \angle 88.5°$
$Y_{21} = 3.6 + j9.9 = 10.5 \angle 160°$
$Y_{12} = j0.02 = 0.02 \angle -90°$

With the help of the Linvill technique input and output networks to achieve maximum power gain were calculated. The bandwidth of the amplifier is determined by the output network, since the input network has a relatively broad bandwidth.

The following parameters were measured on a breadboard amplifier:

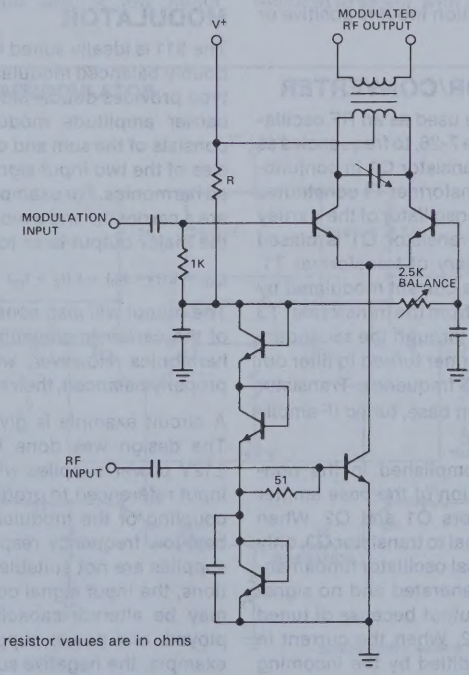
1) power gain—30dB
2) bandwidth (3dB)—0.5MHz
3) noise figure—7dB
4) maximum output swing—300 millivolts RMS across 50 ohms

Because of the very small feedback capacitance of the amplifier, tuning is easily accomplished and input adjustments have very little effect on the output impedance matching and vice versa.

MODULATORS

Returning to the curve of transadmittance of the 510 versus the differential input voltage, Figure 7-10, it may be seen that if a modulating signal instead of an AGC voltage is applied to the control input, the transconductance of the output transistor and the output current vary in a like manner. Figure 7-24 is a modulator circuit. This circuit has been operated with a carrier frequency of 50MHz and a modulating bandwidth of 4MHz. A modification of the circuit of 7-24 is the balanced modulator circuit of Figure 7-25. The constant current generator is modulated by the RF input. When the balance

BALANCED MODULATOR (SUPPRESSED CARRIER)



All resistor values are in ohms

Figure 7-25

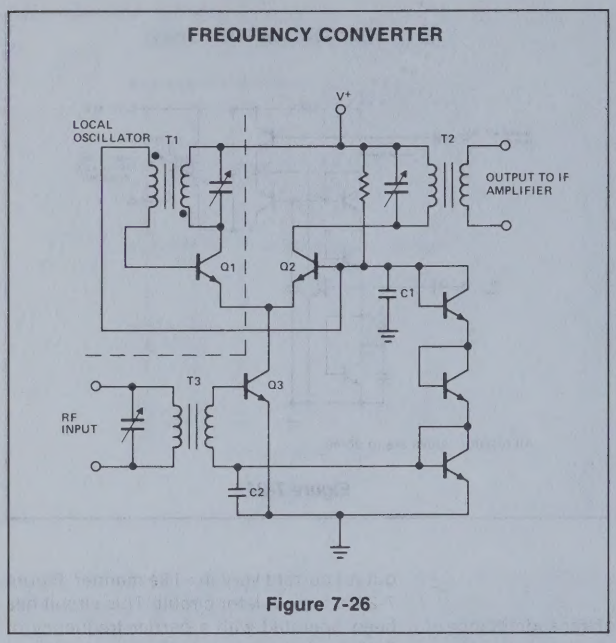


Figure 7-26

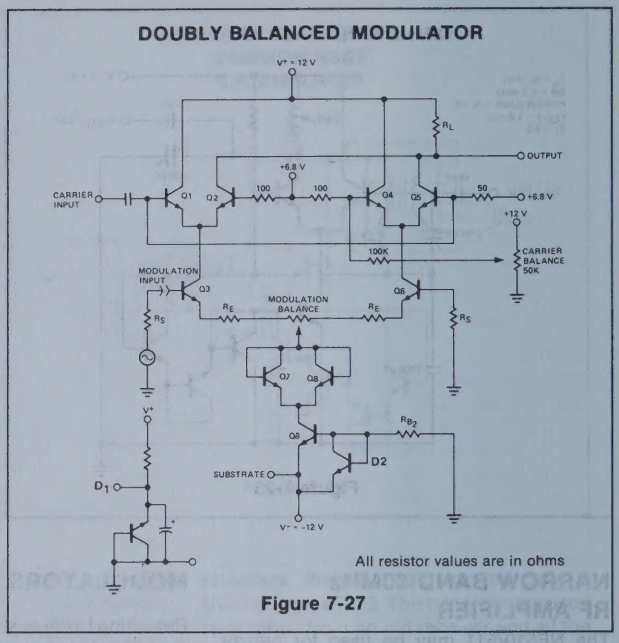


Figure 7-27

resistor is properly adjusted and with no modulation input, no carrier will be present at the output. When a modulation signal is impressed, the collector RF currents of the differential pair of transistors will be unbalanced and a RF signal will be present at the output, the phase of which will depend upon whether the modulation input is positive or negative.

RF OSCILLATOR/CONVERTER

The 510/511 may be used as an RF oscillator/converter, Figure 7-26, to frequencies as high as 100MHz. Transistor Q1 in conjunction with a tuned transformer T1 constitutes a variable frequency oscillator of the Hartley type. The base of transistor Q1 is biased through the secondary of transformer T1. Transistor Q3 has its current modulated by the incoming signal from the transformer T3 and obtains its bias through the secondary of T3. T2 is a transformer turned to filter out all but the desired IF frequency. Transistor Q2 acts as a common base, tuned IF amplifier.

Conversion is accomplished in the nonlinear operating region of the base emitter junction of transistors Q1 and Q2. When there is no input signal to transistor Q3, only harmonics of the local oscillator fundamental frequency are generated and no signal can appear at the output because of tuned filter transformer T2. When the current in transistor Q3 is modified by the incoming signal, beat frequencies are generated between the local oscillator frequency and the incoming signal frequencies and their sum and difference frequencies appear in the currents of transistor Q2. Transformer T2 selects the desired sum or difference frequency for amplification in an IF amplifier.

DOUBLY BALANCED MODULATOR

The 511 is ideally suited for application as a doubly balanced modulator. A circuit of this type provides double sideband suppressed carrier amplitude modulation. Its output consists of the sum and difference frequencies of the two input signals and their related harmonics. For example, when the inputs are a carrier (f_c) and a modulating signal (f_m) the major output is as follows:

$$f_{out} = k(f_c - f_m) + k(f_c + f_m) \qquad 7\text{-}12$$

The output will also contain small amounts of the carrier, modulating signal and their harmonics. However, when the circuit is properly balanced, their effects are minimal.

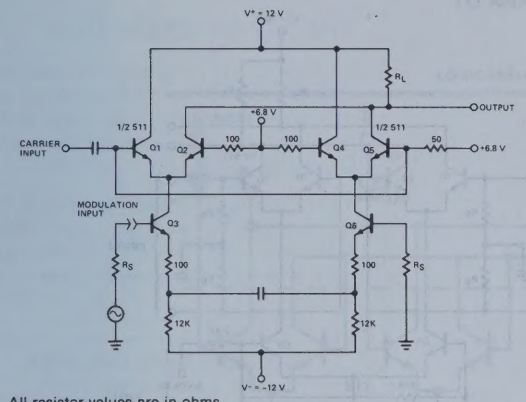
A circuit example is given in Figure 7-27. The design was done for operation with ±12V power supplies with the modulation input referenced to ground to permit direct coupling of the modulation signal for the best low frequency response. If the power supplies are not suitable for some applications, the input signal coupling techniques may be altered; capacitive coupling employed, and power supplies modified. For example, the negative supply input may be grounded, the modulation input may be capacitively coupled and biased at +4V leaving the remainder of the circuit configuration unchanged. The lower half of a 5 i 1 is merely a current source. It may be replaced with a current source constructed from a discrete transistor or if differential modulation input is available, a resistor.

R_E and the modulation balance potentiometer are selected to provide the desired dynamic range capabilities of the modulation input. The voltage developed by the emitter currents across the two R_E's and the modulation balance potentiometer should be approximately equal to the modulating signal peak-to-peak amplitude minus 100mV. Modulating signals exceeding this level will cause distortion. The modulation balance potentiometer is adjusted for minimum modulation signal in the output. In addition to this potentiometer, a carrier balance potentiometer is shown. It should be adjusted to minimize the presence of the carrier in the output. The circuit of Figure 7-28 is a variation of the circuit for Figure 7-27. It eliminates all potentiometers. Carrier and modulation feedthough will not be as small as the circuit of Figure 2-27, but will be quite useful where circuit adjustments must be kept at a minimum. The capacitor between the emitters of Q2 and Q6 should be selected to have a low reactance at the lowest modulating frequency.

DEMODULATOR

The 511 may be used in demodulator applications also. As an example, the FM stereo demodulator circuit of Figure 7-29 is pre-

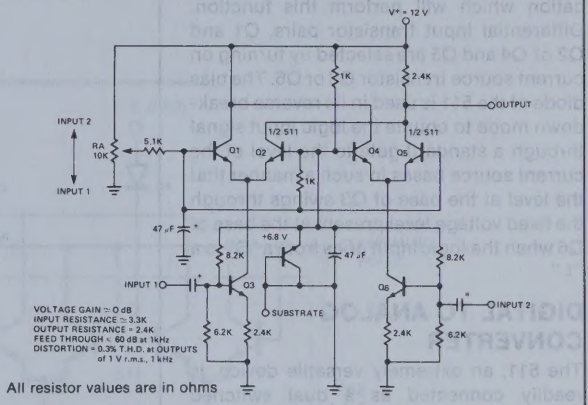
DOUBLY BALANCED MODULATOR, SELF-BALANCING



All resistor values are in ohms

Figure 7-28

ISOLATION AMPLIFIER WITH REMOTELY SELECTED INPUTS AND REMOTELY CONTROLLED GAIN



All resistor values are in ohms

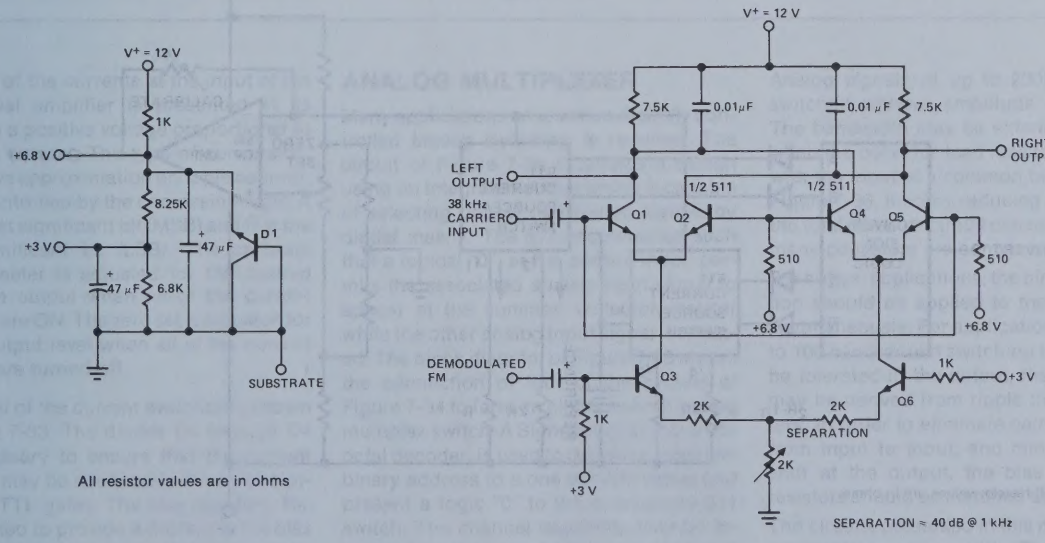
Figure 7-30

sented. The demodulator FM information is applied to the base of Q3. The collector current of Q3 is switched alternately, by the 38KHz sub-carrier local oscillator, from the left output load to the right output load. Transistors Q4 and Q5 are driven out of phase with transistors Q1 and Q2 from the 38KHz local oscillator so as to cancel the 38KHz component in the outputs. The separation is optimized by applying a small portion of the input signal to the emitter Q6 to cancel unwanted out-of-channel information. For maximum separation, the 38KHz sub-carrier local oscillator signal should have a minimum second harmonic content. Ideally its waveform should be square with a 50% duty cycle and have an amplitude of approximately 1V peak-to-peak.

Although doubly balanced modulators are not normally used for audio applications, this type of circuit with a few minor modifications may prove extremely useful. The isolation amplifier with remotely selected inputs is shown in Figure 7-30. The level adjust/mixing control (R_A) may be located at a remote location and the distance is limited only by the noise which may be picked up. Feedthrough from the OFF channel is negligible. Bandwidth is limited only by the capacitive load on the output.

Applications occasionally arise where it is required to select, with a logic signal, one of

STEREO DEMODULATOR



All resistor values are in ohms

Figure 7-29

two inputs to an analog system; for example, sense amplifiers for magnetic tape or disc readout or other memory systems. The circuit of Figure 7-31 illustrates a 511 application which will perform this function. Differential input transistor pairs, Q1 and Q2 or Q4 and Q5 are selected by turning on current source transistor Q3 or Q6. The bias diode of the 511 is used in its reverse breakdown mode to couple the logic input signal through a standard gate to the level of the current source bases in such a manner that the level at the base of Q3 swings through the fixed voltage level present at the base of Q6 when the logic input goes from a "O" to a "1."

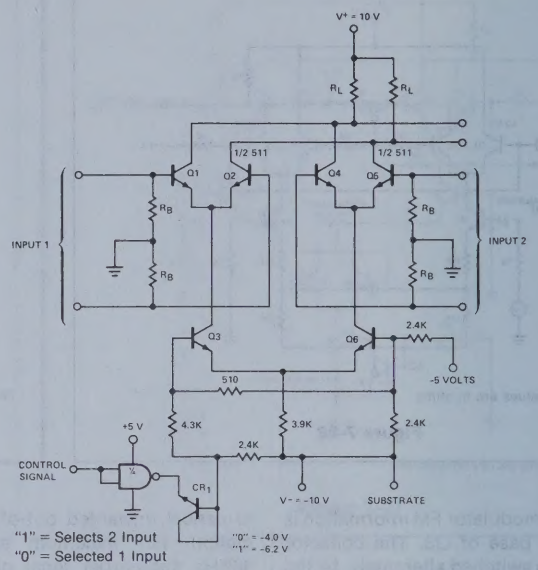
DIGITAL TO ANALOG CONVERTER

The 511, an extremely versatile device, is readily connected as a dual switched current source. When a number of 511's are connected as current sources, with each current properly scaled, a digital to analog converter may be constructed, as in Figure 7-32. The currents are scaled such that:

$$I_n = \frac{I_1}{2^{n-1}} \qquad 7\text{-}13$$

and are summed in a very low impedance provided by the virtual ground present at the inverting input of the operational amplifier.

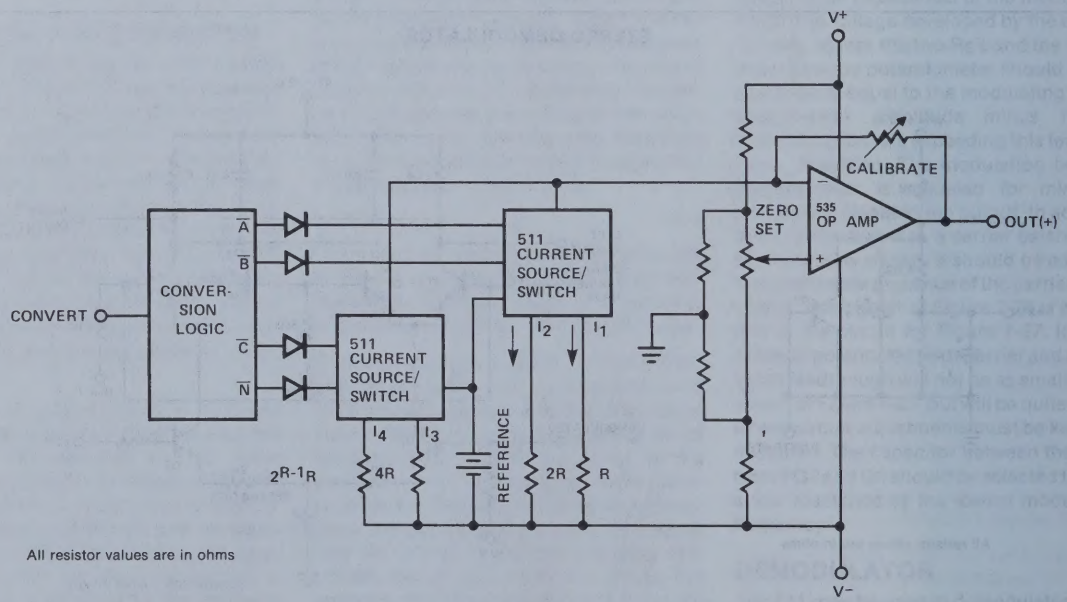
2-INPUT, DIGITALLY SELECTED DIFFERENTIAL PREAMPLIFIER



All resistor values are in ohms

Figure 7-31

BLOCK DIAGRAM—D/A CONVERTER (4-BIT—16 LEVEL)



All resistor values are in ohms

Figure 7-32

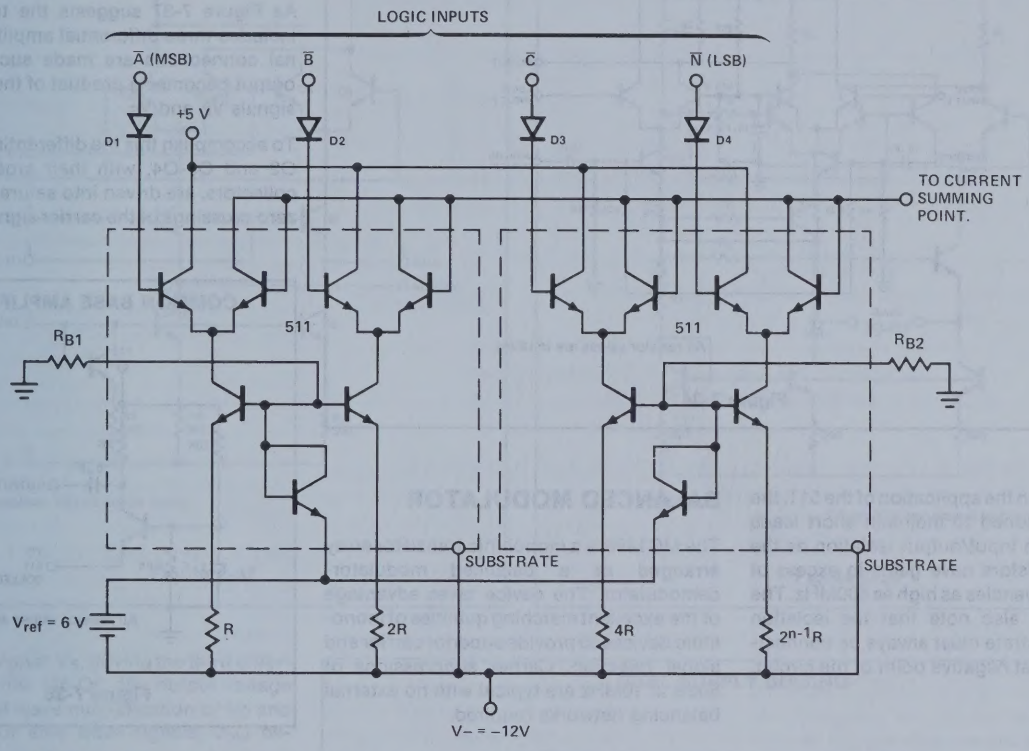


Figure 7-33

The sum of the currents at the input of the operational amplifier is presented at its output as a positive voltage proportional to the input current. The type of conversion, successive approximation or ripple counter, etc., is controlled by the conversion logic. $\overline{A}$ is the most significant bit (MSB) and $\overline{N}$ is the least significant bit (LSB). The calibrate potentiometer is adjusted for the desired maximum output when all of the current switches are ON. The zero set is adjusted for a zero output level when all of the current sources are turned off.

The detail of the current switches is shown in Figure 7-33. The diodes D1 through D4 are necessary to ensure that the current switches may be adequately driven by typical DTL/TTL gates. The bias resistors, R_b, are selected to provide a current in the bias compensating diodes equal to 75% of the current in the most significant of the two current sources of each 511.

ANALOG MULTIPLEXER

Many applications arise where digitally controlled analog switching is required. The circuit of Figure 7-34 illustrates a design using an integrated circuit which is capable of selecting one of two analog signals by digital means. The 511 is connected such that a logical "0", at the control input, permits the associated analog input signal to appear at the common collector resistor while the other analog input signal is rejected. The block diagram of Figure 7-35 shows the connection of four of the circuits of Figure 7-34 to form an eight channel analog multiplex switch. A Signetics 8250, binary to octal decoder, is used to convert a three line binary address to a one of eight signal and present a logic "0" to the appropriate 511 switch. The channel capability may be increased by the use of additional 511's and 8250's with the D (inhibit) input of the 8250's being used to control the groups of eight.

Analog signals of up to 200KHz may be switched without amplitude degradation. The bandwidth may be extended to 2MHz when the collector load resistor is replaced with the input of a common base amplifier, Figure 7-36, thereby reducing the effects of the total parasitic circuit capacitances when many collectors are connected in parallel.

For critical applications, the binary information should be applied to the 8250 inputs simultaneously. For applications where a 50 to 100 nanosecond switching transient may be tolerated in the output, the 8250 inputs may be derived from ripple through counters. In order to eliminate gain differences, from input to input, and minimize the dc shift at the output, the bias and emitter resistors should be matched at 1% or better.

The circuits presented in this memo are but a few of the many possible. The component values shown are not necessarily optimum and should be modified to fit each specific

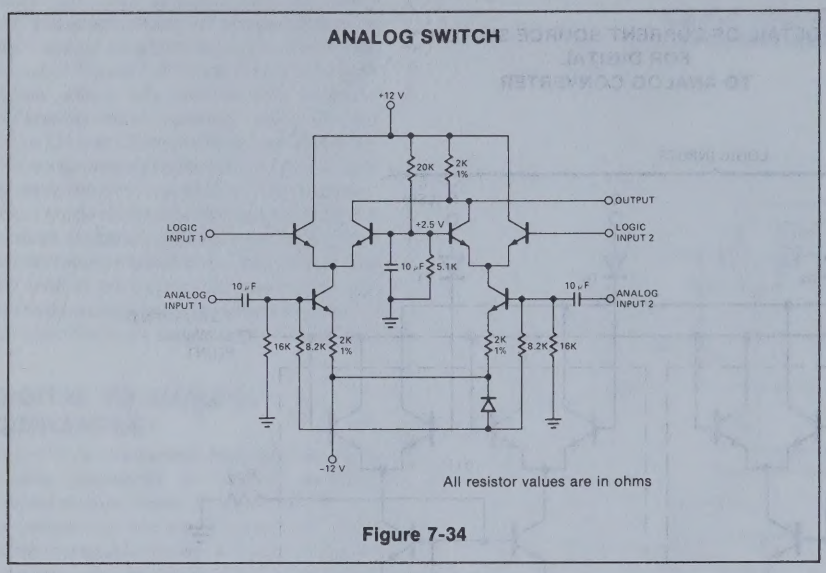


Figure 7-34

application. In the application of the 511, the user is cautioned to maintain short leads and maintain input/output isolation as the circuit transistors have gains in excess of unity at frequencies as high as 500MHz. The user should also note that the isolation contact substrate *must* always be connected to the most negative point of the circuit.

BALANCED MODULATOR

The MC1496 is a monolithic transistor array arranged as a balanced modulator-demodulator. The device takes advantage of the excellent matching qualities of monolithic devices to provide superior carrier and signal rejection. Carrier suppressions of 50dB at 10MHz are typical with no external balancing networks required.

Applications include AM and suppressed carrier modulators, AM and FM demodulators, and phase detectors.

THEORY OF OPERATION

As Figure 7-37 suggests the topography includes three differential amplifiers. Internal connections are made such that the output becomes a product of the two input signals V_C and V_S.

To accomplish this the differential pairs Q1-Q2 and Q3-Q4, with their cross coupled collectors, are driven into saturation by the zero crossings of the carrier signal V_C. With

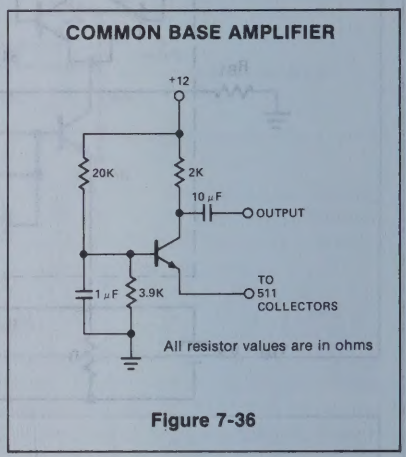


Figure 7-36

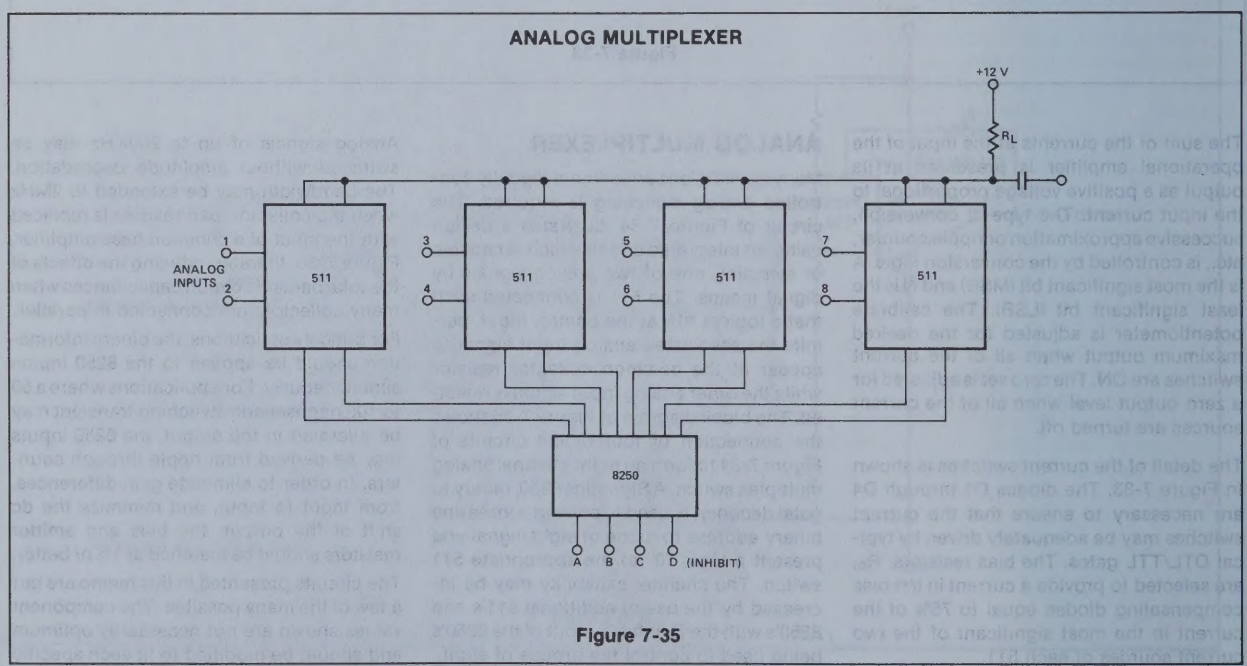


Figure 7-35

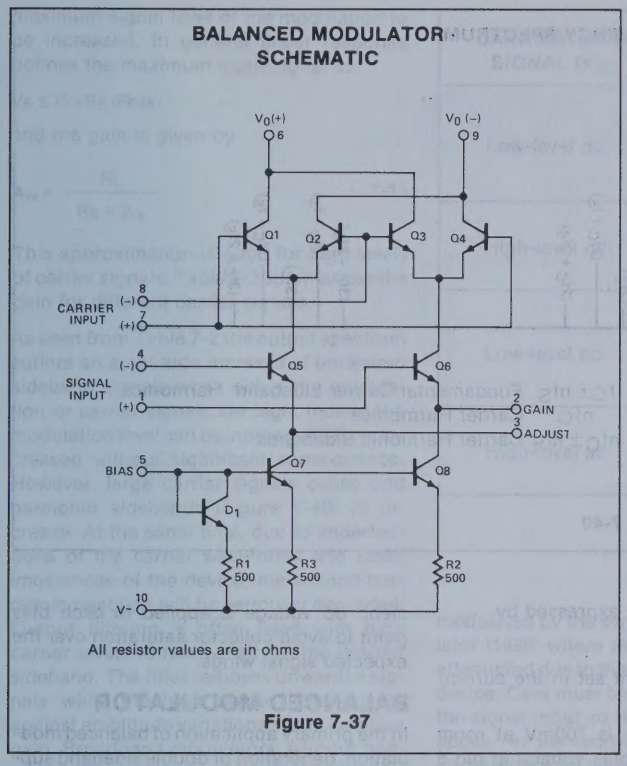


Figure 7-37

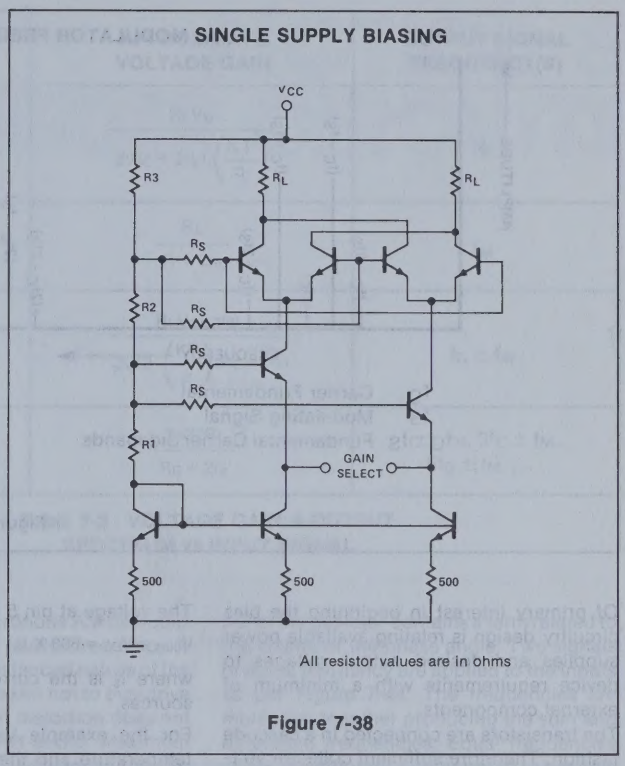


Figure 7-38

a low level signal, V_S, driving the third differential amplifier Q5-Q6, the output voltage will be a full wave multiplication of V_C and V_S. Thus for sine wave signals, V_{out} becomes:

$$V_{out} = E_X E_Y [\cos(\omega_X + \omega_Y)\, t + \cos(\omega_X - \omega_Y)\, t] \quad 7\text{-}14$$

From equation 7-21 the output voltage will contain the sum and difference frequencies of the two original signals. In addition, with the carrier input ports being driven into saturation, the output will contain the odd harmonics of the carrier signals.

BIASING

Since the MC1496 was intended for a multitude of different functions as well as a myriad of supply voltages, the biasing techniques are specified by the individual application. This allows the user complete freedom to choose gain, current levels, and power supplies. The device can be operated with single ended or dual supplies.

Internally provided with the device are two current sources driven by a temperature compensated bias network. Since the transistor geometries are the same and since V_{BE} matching in monolithic devices is excellent, the currents through Q7 and Q8 will be identical to the current set at pin 5. Figure 7-38 and 7-39 illustrate typical biasing arrangements from split and single ended supplies respectively.

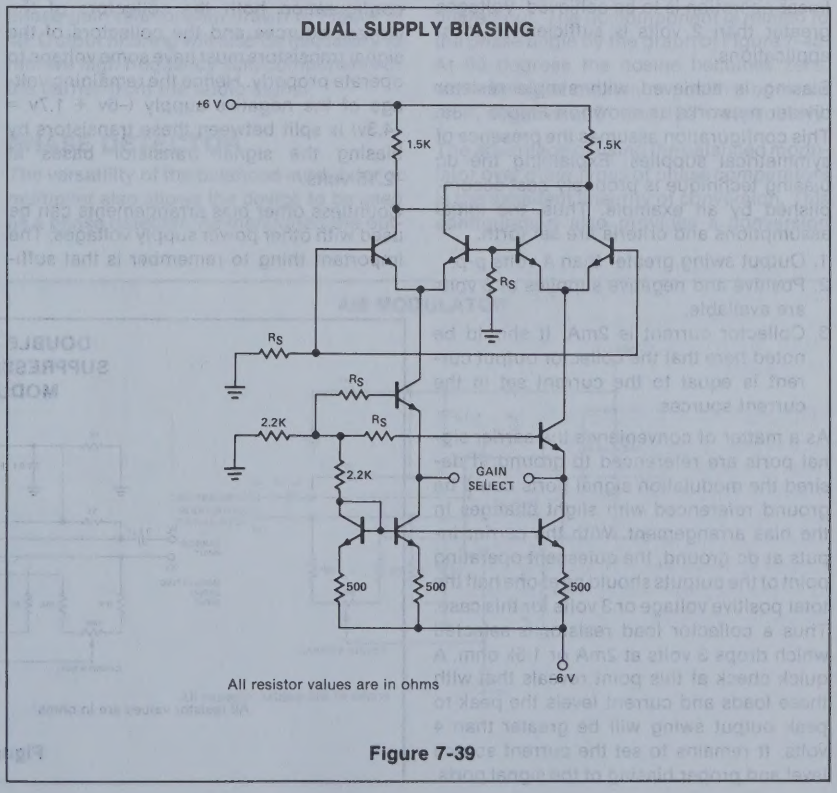


Figure 7-39

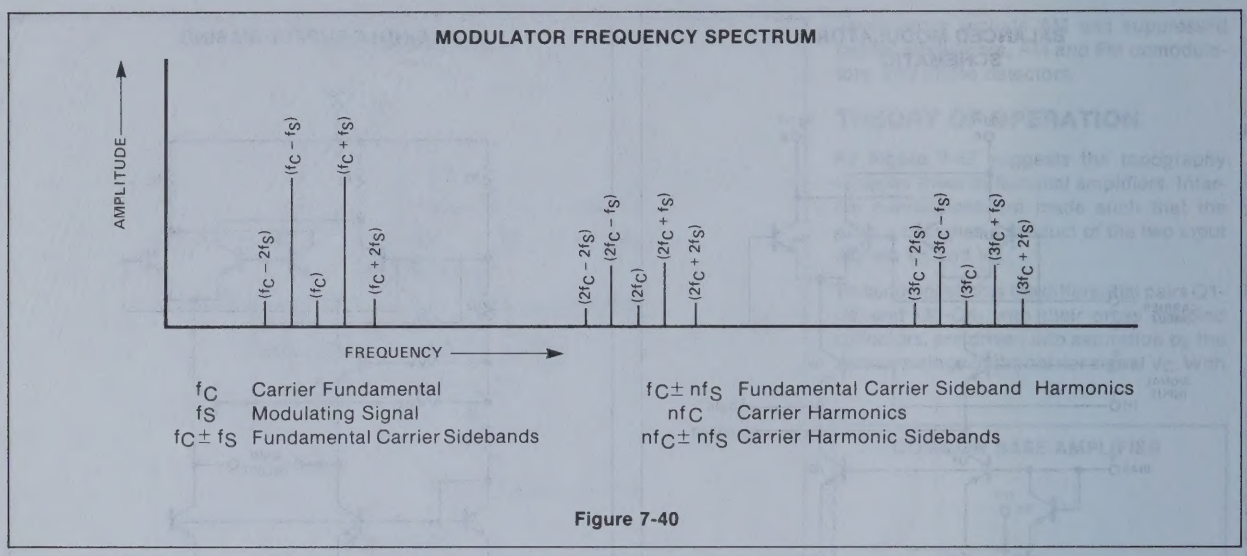


Figure 7-40

Of primary interest in beginning the bias circuitry design is relating available power supplies and desired output voltages to device requirements with a minimum of external components.

The transistors are connected in a cascode fashion. Therefore sufficient collector voltage must be supplied to avoid saturation if linear operation is to be achieved. Voltages greater than 2 volts is sufficient in most applications.

Biasing is achieved with simple resistor divider networks as shown in Figure 7-39. This configuration assumes the presence of symmetrical supplies. Explaining the dc biasing technique is probably best accomplished by an example. Thus, the initial assumptions and criteria are set forth:

1. Output swing greater than 4 volts p-p.
2. Positive and negative supplies of 6 volts are available.
3. Collector current is 2mA. It should be noted here that the collector output current is equal to the current set in the current sources.

As a matter of convenience the carrier signal ports are referenced to ground. If desired the modulation signal ports could be ground referenced with slight changes in the bias arrangement. With the carrier inputs at dc ground, the quiescent operating point of the outputs should be at one half the total positive voltage or 3 volts for this case. Thus a collector load resistor is selected which drops 3 volts at 2mA or 1.5k ohm. A quick check at this point reveals that with these loads and current levels the peak to peak output swing will be greater than 4 volts. It remains to set the current source level and proper biasing of the signal ports.

The voltage at pin 5 is expressed by

$V_{bias} = V_{BE} = 500 \times I_S$

where I_S is the current set in the current sources.

For the example V_{BE} is 700mV at room temperature and the bias voltage at pin 5 becomes 1.7 volts. Because of the cascode configuration both the collectors of the current sources and the collectors of the signal transistors must have some voltage to operate properly. Hence the remaining voltage of the negative supply (-6v + 1.7v = -4.3v) is split between these transistors by biasing the signal transistor bases at -2.15 volts.

Countless other bias arrangements can be used with other power supply voltages. The important thing to remember is that sufficient dc voltage is applied to each bias point to avoid collector saturation over the expected signal wings.

BALANCED MODULATOR

In the primary application of balanced modulation, generation of double sideband suppressed carrier modulation is accomplished. Due to the balance of both modulation and carrier inputs the output, as mentioned, contains the sum and difference frequencies while attentuating the fundamentals. Upper and lower sideband signals are the strongest signals present with harmonic sidebands being of diminishing amplitudes as characterized by Figure 7-40.

Gain of the 1496 is set by including emitter degeneration resistance located as R_E in Figure 7-41. Degeneration also allows the

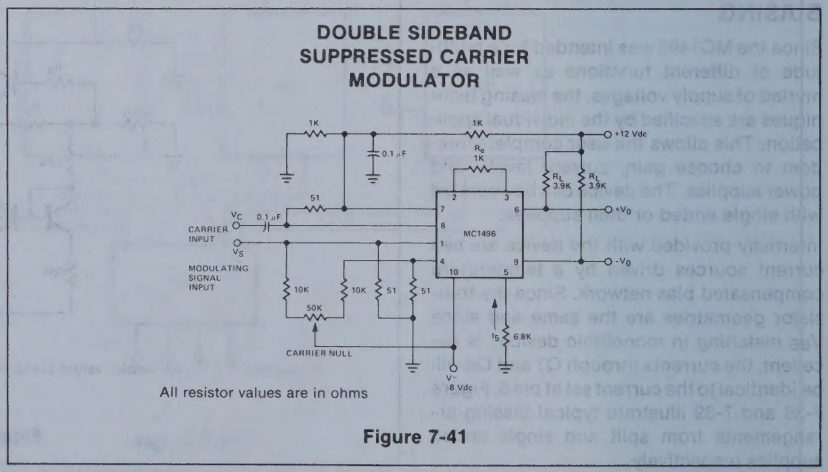


Figure 7-41

maximum signal level of the modulation to be increased. In general linear response defines the maximum input signal as

$V_S \leq I5 \bullet R_E$ (Peak)

and the gain is given by

$$A_{vs} = \frac{R_L}{R_E + 2r_e} \qquad 7\text{-}15$$

This approximation is good for high levels of carrier signals. Table 7-2 summarizes the gain for different carrier signals.

As seen from Table 7-2 the output spectrum suffers an amplitude increase of undesired sideband signals when either the modulation or carrier signals are high. Indeed the modulation level can be increased if R_E is increased without significant consequence. However, large carrier signals cause odd harmonic sidebands (Figure 7-40) to increase. At the same time, due to imperfections of the carrier waveforms and small imbalances of the device, the second harmonic rejection will be seriously degraded. Output filtering is often used with high carrier levels to remove all but the desired sideband. The filter removes unwanted signals while the high carrier level guards against amplitude variations and maximizes gain. Broadband modulators, without benefit of filters, are implemented using low carrier and modulation signals to maximize linearity and minimize spurious sidebands.

CARRIER INPUT SIGNAL (V_C)	APPROXIMATE VOLTAGE GAIN	OUTPUT SIGNAL FREQUENCY(S)
Low-level dc	$\frac{R_L V_C}{2(R_E + 2r_E)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\frac{R_L}{R + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$....

Table 7-2 VOLTAGE GAIN & OUTPUT SPECTRUM vs INPUT SIGNAL

AM MODULATOR

The basic current of Figure 7-41 allows no carrier to be present in the output. By adding offset to the carrier differential pairs, controlled amounts of carrier appear at the output whose amplitude becomes a function of the modulation signal or AM modulation. As shown the carrier null circuit is changed from Figure 7-41 to have a wider range so that wider control is achieved. All connections are shown in Figure 7-42.

AM DEMODULATION

As pointed out in equation 7-41, the output of the balanced mixer is a cosine function of the angle between signal and carrier inputs. Further, if the carrier input is driven hard enough to provide a switching action the output becomes a function of the input amplitude. Thus the output amplitude is maximum when there is 0° phase difference as shown in Figure 7-43.

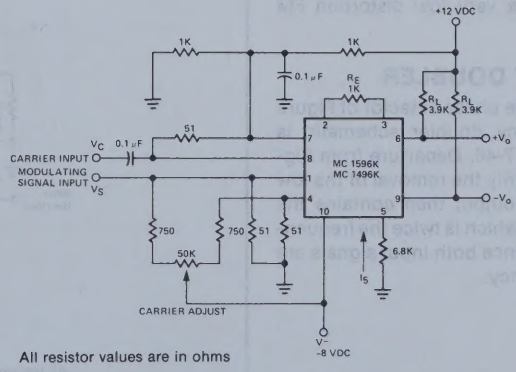
Amplifying and limiting of the AM carrier is accomplished by the ULN2209. Providing 55dB of gain, the 2209 also provides symmetrical limiting above 400μ volts. The limited carrier is then applied to the detector at the carrier ports to provide the desired switching function. The signal is then demodulated by the syncronous AM demodulator (1496) where the carrier frequency is attenuated due to the balanced nature of the device. Care must be taken not to overdrive the signal input so that distortion does not appear in the recovered audio. Maximum conversion gain is reached when the carrier signals are in phase as indicated by the phase-gain relationship drawn in Figure 7-43. Output filtering will also be necessary to remove high frequency sum components of the carrier from the audio signal.

PHASE DETECTOR

The versatility of the balanced modulator or multiplier also allows the device to be used as a phase detector. As mentioned the output of the detector contains a term related to the cosine of the phase angle. Two signals of equal frequency are applied to the inputs as per Figure 7-44. The frequencies are multiplied together producing the sum and difference frequencies. Equal frequencies cause the difference component to become dc while the undesired sum component is filtered out. The dc component is related to the phase angle by the graph of Figure 7-45. At 90 degrees the cosine becomes zero, while being at maximum positive or maximum negative at 0° and 180° respectively.

The advantage of using the balanced modulator over other types of phase comparators is the excellent linearity of conversion. This configuration also provides a conversion

AM MODULATOR



All resistor values are in ohms

Figure 7-42

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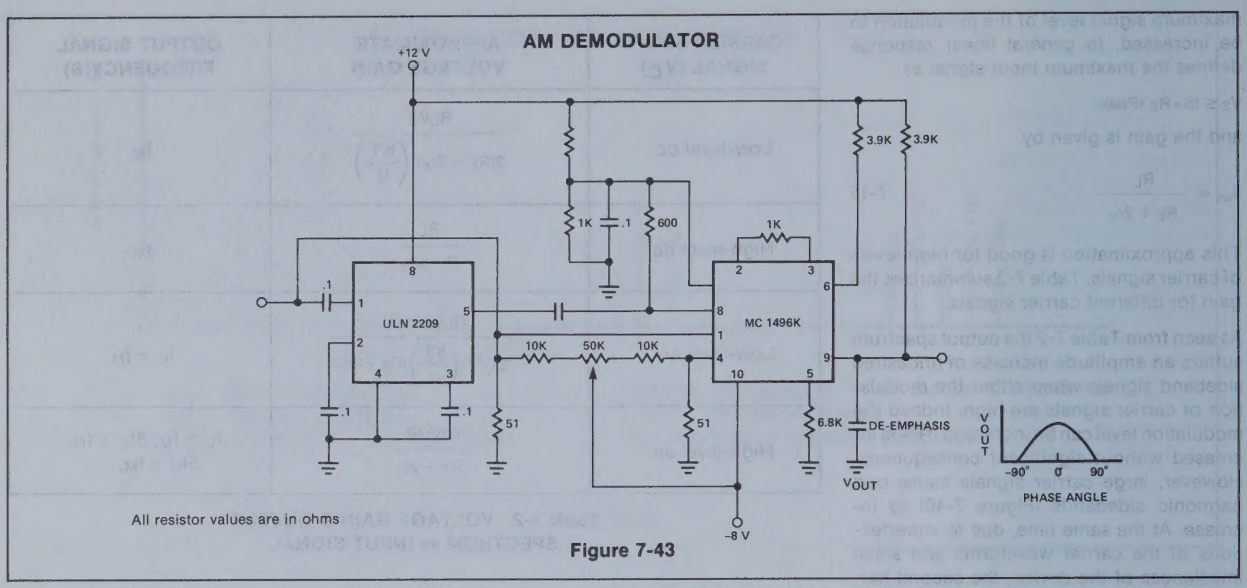


Figure 7-43

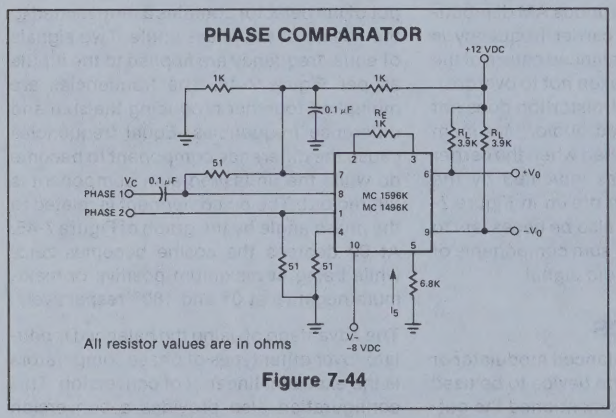


Figure 7-44

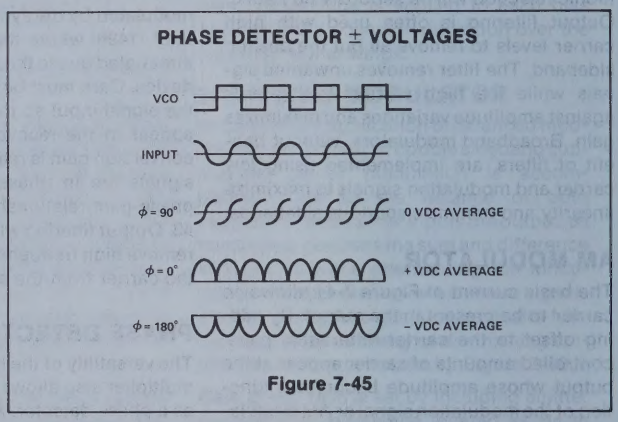


Figure 7-45

gain rather than a loss for greater resolution. Used in conjunction with a phase locked loop for instance, the balanced modulator provides a very low distortion FM demodulator.

FREQUENCY DOUBLER

Very similar to the phase detector of Figure 7-44, a frequency doubler schematic is shown in Figure 7-46. Departure from Figure 7-44 is primarily the removal of the low pass filter. The output then contains the sum component which is twice the frequency of the input since both input signals are the same frequency.

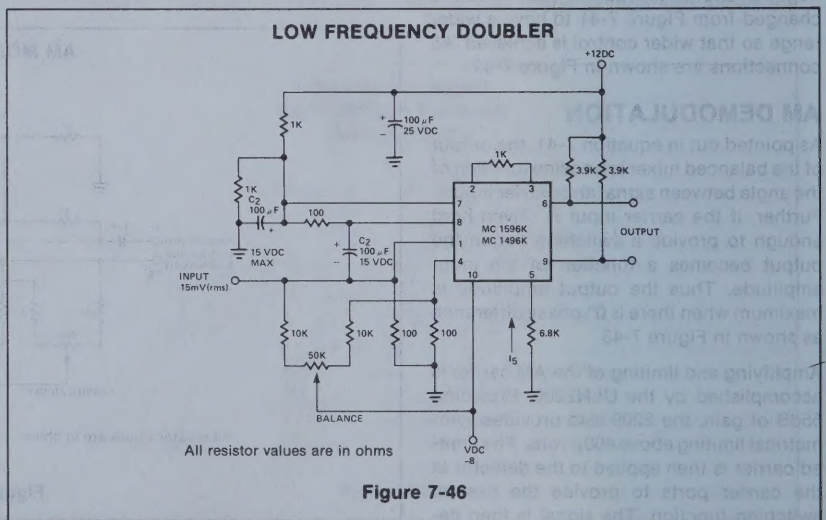
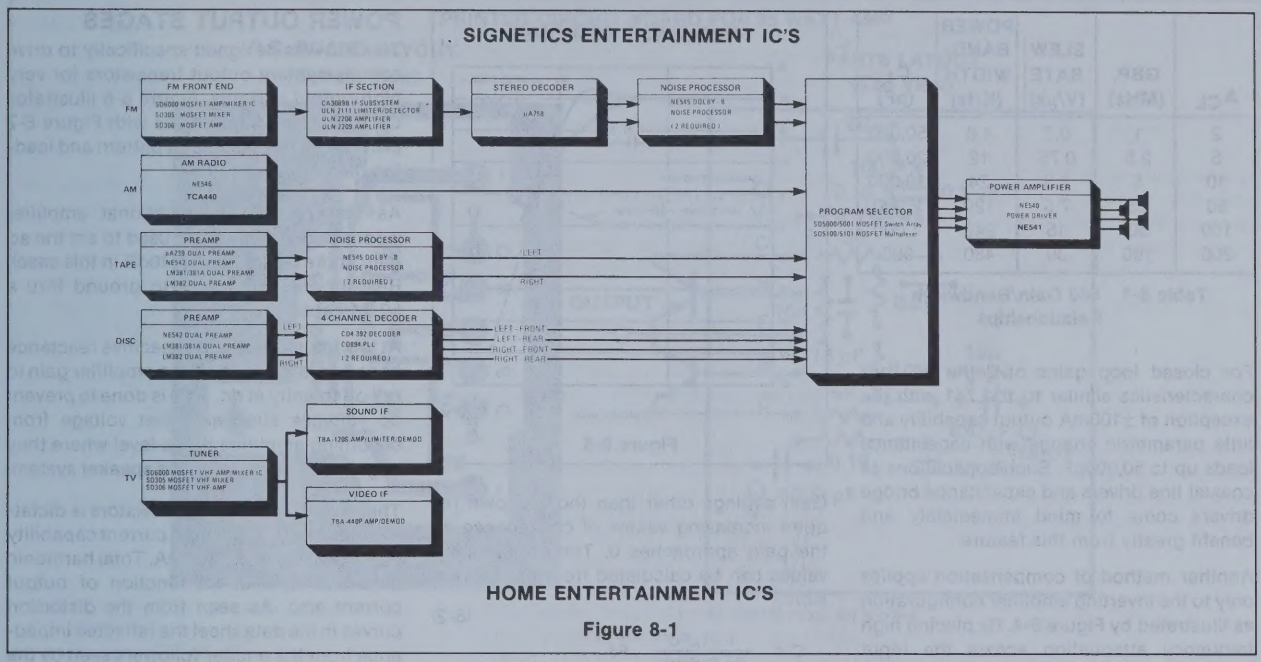


Figure 7-46

SECTION 8
CONSUMER CIRCUITS



HOME ENTERTAINMENT IC'S

Figure 8-1

INTRODUCTION

The ever increasing voracity of the consumer electronics marketplace has led to a host of integrated circuits which replace discrete devices and simplify the old methods of doing things. For instance home entertainment systems now enjoy the use of integrated power amplifiers, pre-amplifiers, and IF systems on a single chip. More recent advancements have added the Dolby circuit and the CD-4 four channel stereo decoder in monolithic form. The following chapter will cover in detail the numerous benefits of using the new generation of consumer I.C.'s.

POWER AMPLIFICATION

Optimized for high quality and low distortion the 540 power driver is designed to drive a pair of complementary output transistors.

It features low standby current, 100mA output capability, low bias current, external current and power limiting, wide power bandwidth and a power supply operating range from ±5V to ±25V.

The 540 power driver is in essence a transconductance amplifier with an extremely linear output current swing of ±100mA with a transconductance of 3.3 Amps/Volt. The input stage converts the differential input voltage into current and the remaining circuitry is basically a current amplifier in a class B configuration. Operating in class B allows the device to drive large currents with a minimum of internal power dissipation while using current gain rather than voltage gain increases bandwidth.

COMPENSATION

Most designs utilizing the 540 should be limited to gains higher than 40dB for simplicity of compensation. At this gain level a simple capacitance to ground and a small lead network in the feedback path provide excellent stability and wide bandwidth.

OPEN LOOP FREQUENCY RESPONSE

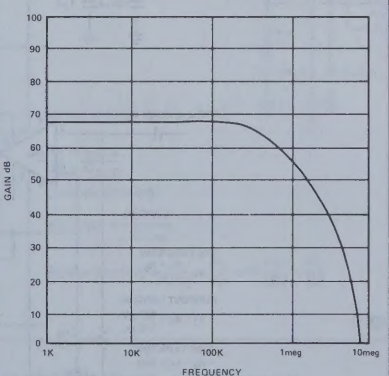


Figure 8-2

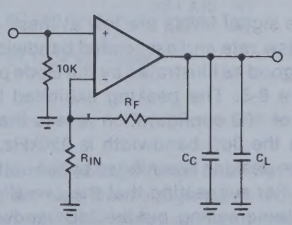
Because the 540 does possess many op amp features the compensation techniques for lower gains are also of interest. In order to simplify the precedure the current gain or transconductance is related to voltage gain. The output impedance of the 540 is 5kohms in parallel with 100pF. Therefore, the equivalent open loop voltage gain is equal to

$$A_o = g_m \times R_o = 3.3 \times 5 \times 10^3 = 16.5k \quad (8\text{-}1)$$

Where $g_m = 3.3$ mho

The frequency response is given in Figure 8-2. Two methods of compensation can be used although one method allows only the inverting configuration. Figure 8-3 shows the lower gain configurations, which is valid for both inverting or noninverting configurations. As shown, by increasing the load capacitance the amplifier becomes more stable. Table 8-1 relates the necessary compensation capacitance to the required gain. Changes in bandwidth and slew rate are also given.

CIRCUIT FOR GAINS LESS THAN 100



All resistor values are in ohms

Figure 8-3

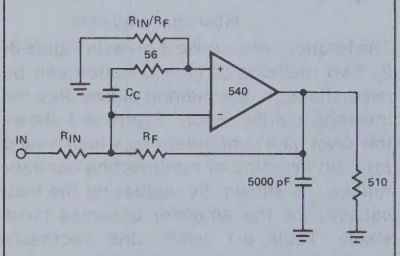
A_{CL}	GBP. (MHz)	SLEW RATE (V/μs)	POWER BAND-WIDTH (KHz)	C_L (pF)
2	1	0.3	4.8	50,000
5	2.5	0.75	12	20,000
10	5	1.5	24	10,000
50	25	7.5	120	2,000
100	50	15	240	1,000
200	100	30	480	500

Table 8-1 540 Gain/Bandwidth Relationships

For closed loop gains of 2 the 540 has characteristics similar to the 741 with the exception of ±100mA output capability and little parametric change with capacitance loads up to 50,000pF. Such applications as coaxial line drivers and capacitance bridge drivers come to mind immediately and benefit greatly from this feature.

Another method of compensation applies only to the inverting amplifier configuration as illustrated by Figure 8-4. By placing high frequency attenuation across the input terminals the loop gain is reduced sufficiently to avoid oscillations even at unity gain.

ALTERNATE METHOD OF INPUT COMPENSATION



All resistor values are in ohms

Figure 8-4

Since signal levels are low at these points the slew rate and associated bandwidth are very good as illustrated by the Bode plots of Figure 8-5. The peaking exhibited by the gain of 100 configuration is less than 2dB while the 3dB bandwidth is 850kHz. More severe peaking is exhibited by the unity gain amplifier suggesting that the overall phase shift is increasing, but the 3dB bandwidth is over 2MHz.

FREQUENCY RESPONSE

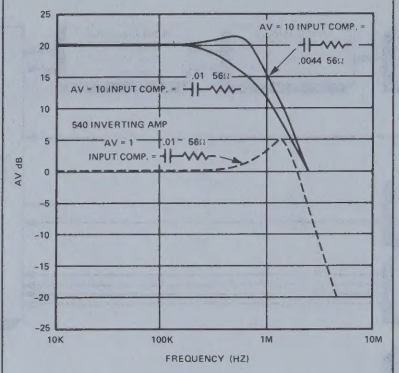


Figure 8-5

Gain settings other than those shown require increasing values of capacitance as the gain approaches 0. The approximate values can be calculated from the expression

$$C = \frac{0.01\mu Fd}{R_F \text{ (kohms)}} \quad \mu Fd \qquad (8\text{-}2)$$

where $R_{series} = 56$ohms and R_F is expressed in kohms.

Although 56 ohms was found to be adequate in most cases, slightly less resistance may be beneficial at unity gain while higher values will be satisfactory at higher gains. The formula of Equation 8-2 is only approximate and will depend upon the series resistance used and the capacitance loading present at the amplifier output.

POWER OUTPUT STAGES

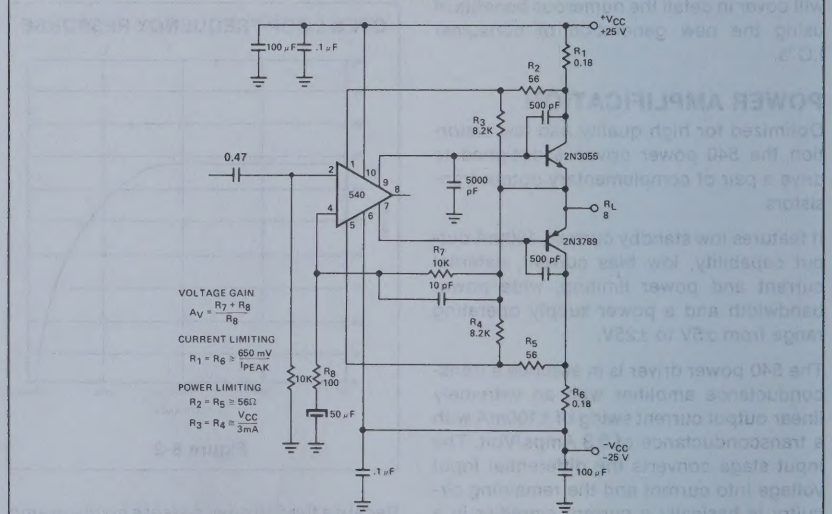
The 540 was designed specifically to drive complementary output transistors for very high output currents. Figure 8-6 illustrates the necessary connections with Figure 8-7 providing a printed circuit pattern and loading diagram.

As shown, typical operational amplifier feedback techniques are used to set the ac gain at the desired point (40dB in this case). Resistor R8 is returned to ground thru a 50μfd capacitor.

At low frequencies the capacitive reactance becomes large causing the amplifier gain to roll off to unity at dc. This is done to prevent dc voltages such as offset voltage from becoming amplified to the level where they might be detrimental to the speaker system.

The selection of power transistors is dictated primarily by the output current capability of the 540 which is ±100mA. Total harmonic distortion is a direct function of output current also. As seen from the distortion curves in the data sheet the reflected impedance from the emitter followers seen by the 540 should be as high as possible if minimum harmonic and intermodulation distortion is to be realized. Transistor types having betas greater than 50 at 3 amps of current are excellent choices. Such transistor types as the 2N3055, or the 2N5877 npn types and the 2N3789 or 2N5879 pnp types are good choices because their betas are specified at 4 amps and they are relatively inexpensive.

35 WATT POWER AMPLIFIER



All resistor values are in ohms.

Figure 8-6

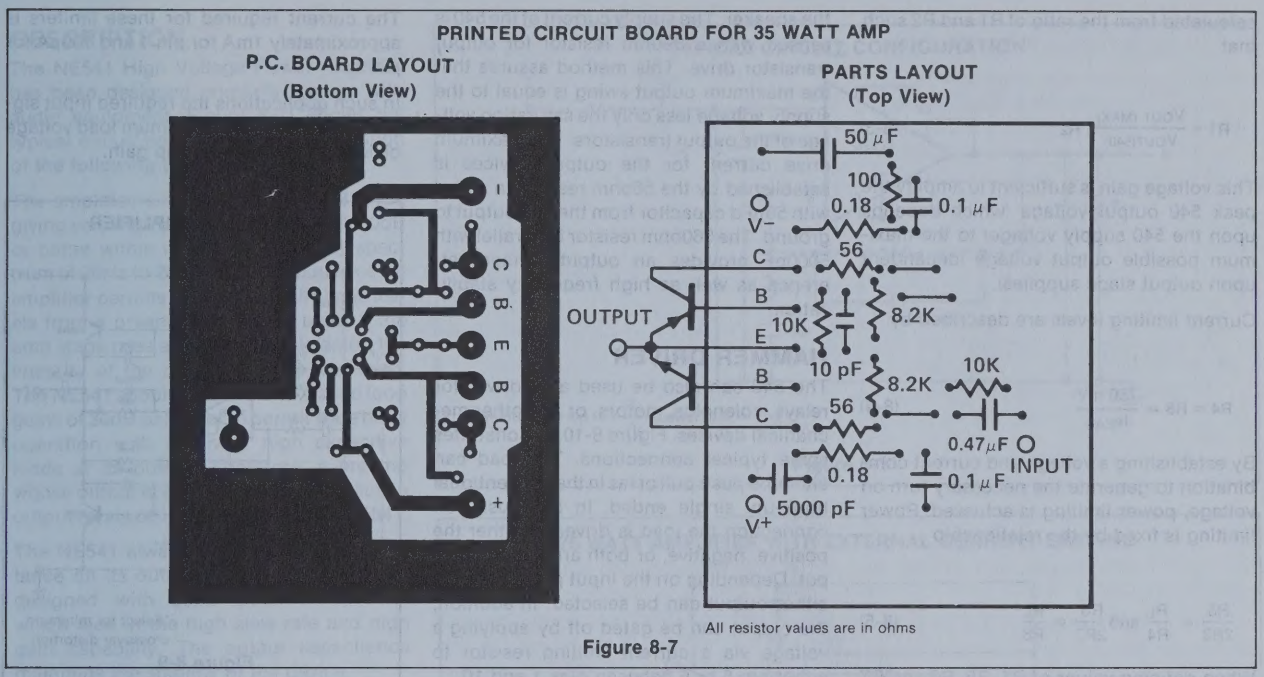


Figure 8-7

At high frequencies additional phase shifts up to 90 degrees can be contributed by the output transistors. Total phase margin in these cases reduces to less than 45 degrees which can cause instability. Miller capacitors of 500pF should be added from base to collector as shown in Figure 8-6. Close physical leads should be incorporated to assure low lead inductance.

POWER LIMITING

Power limiting is achieved by placing a resistor network around the output stage as shown in Figure 8-6. R1 and R6 are current sensing resistors with R3 and R4 being voltage sensing resistors. It is the purpose of R2 and R5 to establish a voltage just below the V_{BE} of the current limiter transistor. Only a small additional current through the output devices is necessary to increase the voltage drop sufficiently to activate the current limiters. However, as long as a load is present at the output, the voltage across resistors R3 and R4 will be reduced proportionally to the voltage developed across the load resistor allowing higher currents to be developed only under safe load limits. Typical V_{BE}/I_B curves for the limiter devices can be found in the data sheet. Power dissipation internally to the 540 can become quite high. Especially with maximum power supply voltages it is a good idea to use a clip on heat sink. For example at ±25 volts the device quiescent current is 20mA maximum. Therefore internal dissipation is 1W—in excess of package ratings without the use of a clip on radiator.

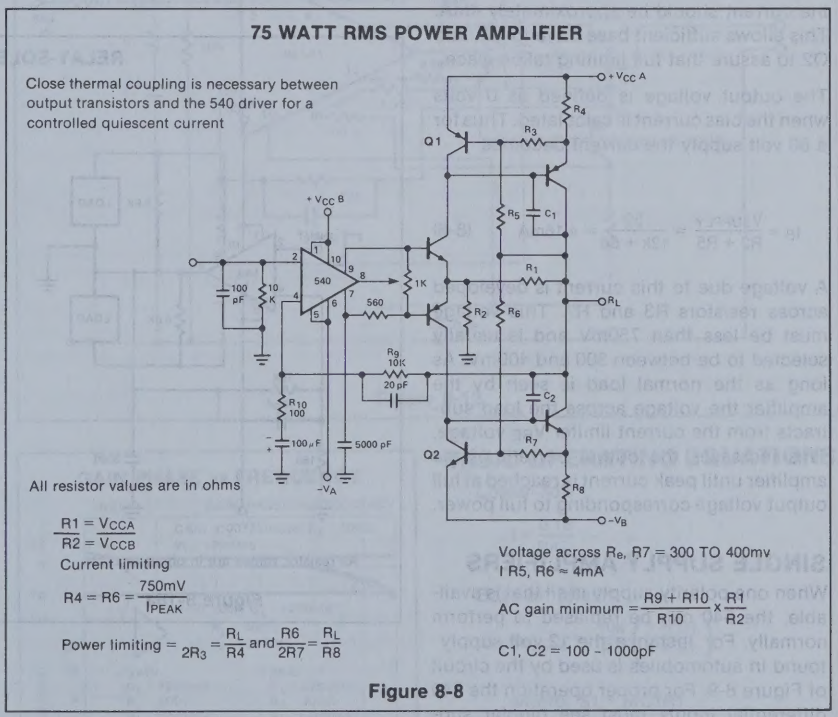


Figure 8-8

HIGH POWER AMPLIFIER

Figure 8-8 shows a hook-up of the 540 driving an output stage capable of swinging 95 volts peak-to-peak. Given a 16ohm load the output rms power is then greater than 72W.

The extended voltage range is achieved by driving the load from a high current output stage which has voltage gain and which is operating from a higher supply voltage. Q1 and Q2 provide current and power limiting for the output stage. Output stage gain is

calculated from the ratio of R1 and R2 such that

$$R1 = \frac{V_{OUT\ (MAX)}}{V_{OUT(540)}} \cdot R2 \qquad (8\text{-}3)$$

This voltage gain is sufficient to amplify the peak 540 output voltage (which depends upon the 540 supply voltage) to the maximum possible output voltage (dependent upon output stage supplies).

Current limiting levels are described by

$$R4 = R8 = \frac{750\ mV}{I_{PEAK}} \qquad (8\text{-}4)$$

By establishing a voltage and current combination to generate the necessary turn on voltage, power limiting is achieved. Power limiting is fixed by the relationship

$$\frac{R5}{2R3} = \frac{R_L}{R4} \text{ and } \frac{R6}{2R7} = \frac{R_L}{R8} \qquad (8\text{-}5)$$

When defining values of R3, R5, R6 and R7 the current should be approximately 4mA. This allows sufficient base drive to Q1, and Q2 to assure that full limiting takes place.

The output voltage is defined as 0 volts when the bias current is calculated. Thus for a 50 volt supply the current becomes

$$I_B = \frac{V_{SUPPLY}}{R3 + R5} = \frac{50}{12k + 56} = 4.16mA \qquad (8\text{-}6)$$

A voltage due to this current is developed across resistors R3 and R7. This voltage must be less than 750mV and is usually selected to be between 300 and 400mV. As long as the normal load is seen by the amplifier the voltage across the load subtracts from the current limiter V_{BE} voltage. This increases the output current of the amplifier until peak current is reached at full output voltage corresponding to full power.

SINGLE SUPPLY AMPLIFIERS

When one polarity supply is all that is available, the 540 can be rebiased to perform normally. For instance the 12 volt supply found in automobiles is used by the circuit of Figure 8-9. For proper operation the 540 differential inputs must see bipolar supplies. To achieve this the inputs are returned to one half of the available supply or 6 volts. All circuitry is otherwise basic with the exception of the load. The amplifier output will be 6 volts dc since the amplifier has a dc gain of one. The load must be ac coupled in order to block this voltage from the speaker. The supply current of the 540 is sensed with a 39ohm resistor for output transistor drive. This method assures that the maximum output swing is equal to the supply voltage less only the saturation voltage of the output transistors. The maximum drive current for the output devices is established by the 56ohm resistor in series with 50μFd capacitor from the 540 output to ground. The 560ohm resistor in parallel with 5000pF provides an output voltage reference as well as high frequency stabilization.

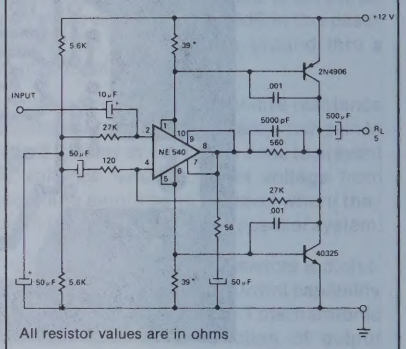
HAMMER DRIVER

The 540 can also be used as a driver for relays, solenoids, motors, or any other mechanical devices. Figure 8-10 demonstrates some typical connections. The load can either be push pull or (as in the conventional hook-up) single ended. In the push-pull connection the load is driven in either the positive, negative, or both arms of the output. Depending on the input pulse polarity, either output can be selected. In addition, the output can be gated off by applying a voltage via a current limiting resistor to either pin 5 or 6 between pins 1 and 10.

The current required for these limiters is approximately 1mA for pin 1 and 100μA for pin 5.

In such applications the required input signal is defined by the maximum load voltage divided by the closed loop gain.

CAR RADIO AMPLIFIER

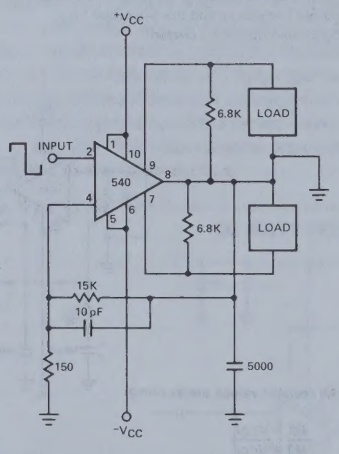


All resistor values are in ohms

*Select for minimum crossover distortion

Figure 8-9

RELAY-SOLENOID DRIVER



All resistor values are in ohms

Figure 8-10a

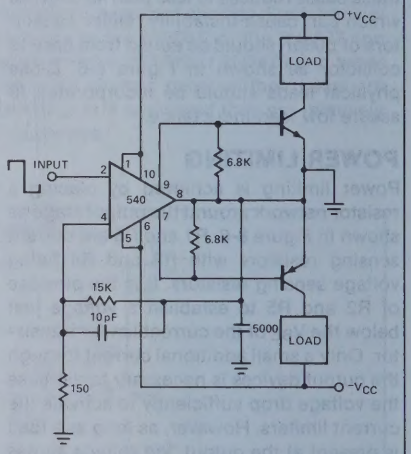


Figure 8-10b

DESCRIPTION

The NE541 High Voltage Power Amplifier has been designed primarily for use with audio equipment. Figure 8-11 shows the typical circuit configuration for evaluation of the following parameters.

The amplifier is basically a class AB1 type giving very high current gain (typically 90dB or better within the audio frequency spectrum of 20Hz to 20kHz). The high gain of the amplifier permits relatively small signal levels from a preamp stage to be used. If the amp stage uses a large feedback factor, the linearity of the preamp can be improved. The NE541 should operate with closed loop gains of 30dB or higher to permit wide band operation with relatively high capacitive loads at its output. Therefore, a preamp whose output is 200-300mVrms will result in output levels of 10-20Vrms from the NE541.

The NE541 always requires some capacitance on its output. The device has been designed with some positive feedback which aids in the high slew rate and high gain capability. The output capacitance maintains the stability of the device.

The NE541 has built-in short circuit protection. A sensing resistor in series with the output drivers turns on a base current shunt when the output current goes too high. This limit is set to approximately 100mA typically, but will have variations due to processing and manufacturing tolerances. In addition to the built-in short circuit protection, the current can be limited by use of external circuitry as shown in Figure 8-12.

The wide band operation of the device as seen in Figure 8-13 plus the nominal low offset voltages inherent to the amplifier (V_{OS} and I_{OS}) will permit the usage of the device in several other areas, such as instrumentation amplifiers, servo drivers and power regulators.

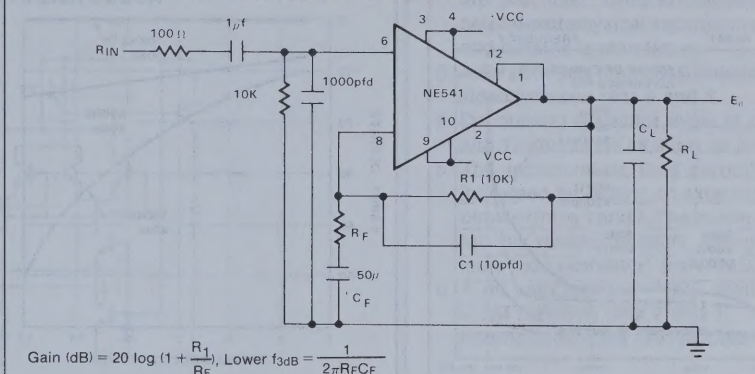
Several input configurations can be incorporated to add either bass or treble boost to the system. These configurations should be evaluated by the designer to best fit his needs. For high power systems additional speaker compensation can be included.

FM DETECTOR—LIMITER

The ULN2111 was designed primarily for FM and TV sound IF applications. This circuit is comprised of a three stage limiting amplifier with a voltage gain of 60dB and a balanced quadrature phase detector as shown in Figure 8-17.

Comprised of three identical differential amplifier stages, the amplifier—limiter is directly coupled thru emitter followers. The direct coupling is possible by using an

TYPICAL CIRCUIT CONFIGURATION



Gain (dB) = 20 log $(1 + \frac{R_1}{R_F})$, Lower $f_{3dB} = \frac{1}{2\pi R_F C_F}$

Figure 8-11

75 WATT AMPLIFIER WITH EXTERNAL CURRENT LIMITING

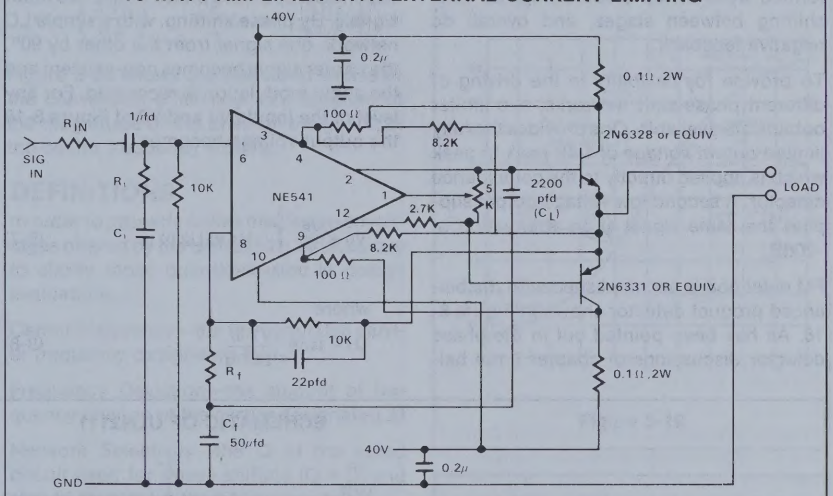


Figure 8-12

GAIN PHASE vs FREQUENCY

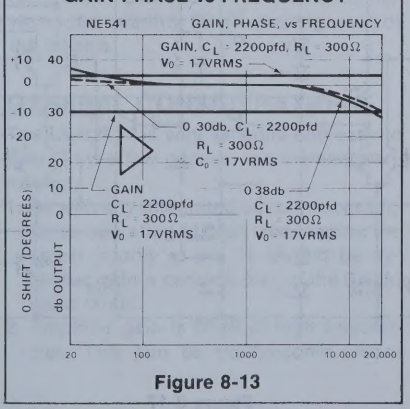


Figure 8-13

BASIC OPERATING EQUATIONS

Lower 3dB

$$f = \frac{0.16}{R_f C_f}$$

Bass Emphasis

$$e_{in\ pin\ 6} = \frac{10k}{R_{in}}\left(\frac{1+S1}{1+S2}\right)$$

where: $S1 = jwC1R1$

$S_2 = jwC1\ (R1 + R2)$

Amplifier Gain (Midband)

$$A_{CL} = 20 \log_{10} \frac{10k + R_f}{R_f}\ R_f \text{ in } k\Omega$$

Loop gain ≈ 90dB − A_{CL}

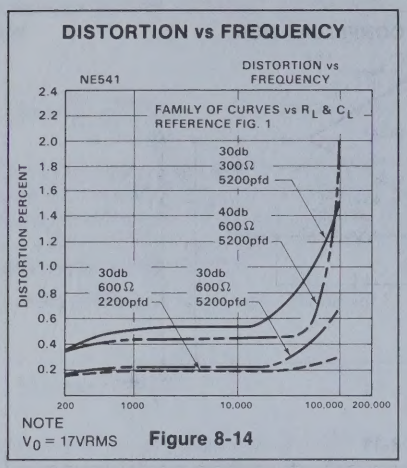


Figure 8-14

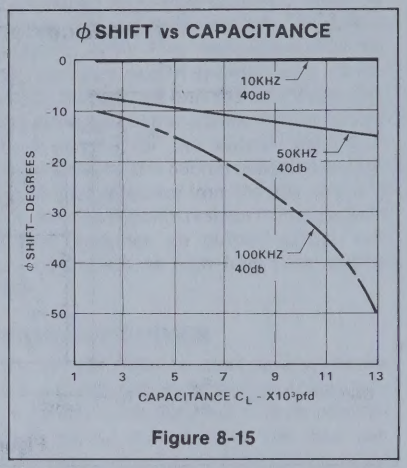


Figure 8-15

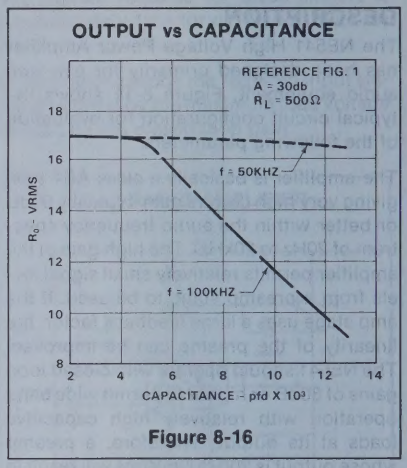


Figure 8-16

internally generated voltage reference formed by a series diode string, dc level shifting between stages, and overall dc negative feedback.

To provide for flexibility in the driving of different phase-shift networks, two limiter outputs are available. One provides the fully limited output voltage of 1.4V peak to peak which is applied directly to the coincidence detector. A second low voltage output supplies the same signal at an attenuation of -20dB.

FM detection is accomplished with the balanced product detector shown in Figure 8-18. As has been pointed out in the phase detector discussions of chapter 7 the balanced product detector produces an output dependent upon the phase of the two input signals. By phase shifting, with a simple LC network, one signal from the other by 90°, the carrier signal becomes non-existent and the audio modulation is recovered. For any level of the inputs V1 and V2 of Figure 8-18 the output voltage becomes

$$Vo = \frac{V_R}{t} \int_0^t U1\,(t)\,U2\,(t)\,dt \qquad (8\text{-}7)$$

where

$$U_1 = \tanh \frac{V1\,(t)}{2kT/q} \qquad (8\text{-}8)$$

$$U2 = \tanh \frac{V2\,(t)}{2kT/q} \qquad (8\text{-}9)$$

and

$$V_R = \frac{I_O R}{2} \qquad (8\text{-}10)$$

Equation 8-7 shows that the output is proportional to the product of the two input functions U(t).

The U function accounts for any symmetrical limiting in the base-emitter junctions and can be approximated for linear opera-

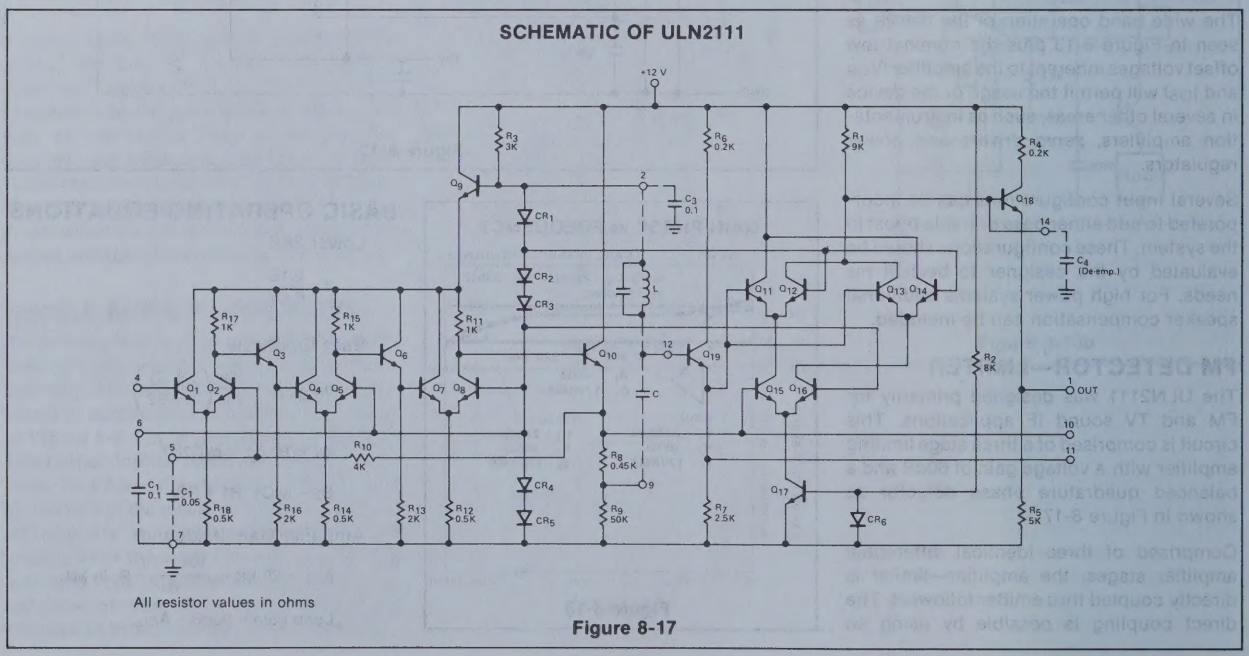


Figure 8-17

MONOLITHIC MULTIPLIER BLOCK

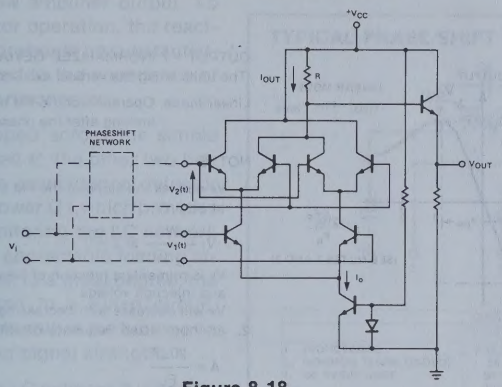


Figure 8-18

tion and hard-limiting by the input voltage itself or by switching function, respectively.

There are two modes of operation: high level switching and low level switching. The frequency-transfer characteristics for each operating mode are given by:

$$\frac{V_o}{V_R} = \frac{2}{\pi} \arctan a \text{ (high level)} \quad (8\text{-}11)$$

$$\frac{V_o}{V_R} = \frac{2}{a}\left(\frac{|V1|_o}{2kT/q}\right)\frac{a}{1+a^2} \text{ (low level)} \quad (8\text{-}12)$$

where

$$A = 2Q\frac{\Delta F}{F_o} = \text{normalized frequency deviation} \quad (8\text{-}13)$$

and

$|V1|_o$ is the magnitude of V1 at the center frequency.

Equation 8-17 and 8-18 are plotted in Figure 8-19. For low level operation, the amplitude of the bell-shaped response of the tuned circuit provides the response fall-off on either side of the center frequency, and the familiar S-shaped transfer function is obtained. The peak-to-peak separation of the source is directly related to the 3dB bandwidth of the tuned circuit. For high-level operation and within a large range of frequency deviations, the amplitude response of the network transfer function is eliminated, and the response is directly that of the phase-shift properties of the LC network.

The conversion efficiency, V_F defined as the slope of the transfer characteristic at the center frequency, can be shown to be:

$$V_F = \left(\frac{d\,Vo}{d\,a}\right)_{a=0} = \frac{2}{\pi} V_R \tanh\frac{|V1|_o}{2kT/q} \quad (8\text{-}14)$$

Figure 8-20 shows the measured values of the conversion efficiency as a function of the magnitude of the driving voltage V1, at the center frequency 4.5MHz.

DEFINITIONS

In order to properly utilize the design advantages offered by the ULN2111 it is necessary to clarify those quantities used in design evaluations.

Center Frequency—the fm modulated carrier frequency designated by f_o.

Frequency Deviation—the amount of frequency change of the carrier designated Δf

Network Selectivity—the Q of the tuned circuit used for phase shifting ($Q = \frac{fo}{BW}$ and should be greater than 10)

Conversion Efficiency—the slope of the fm "S" curve specified by $(dV_{OUT}/d\theta) = VOLTS$ per radian.

Normalized Deviation—For simple LC networks the quantity $2Q\frac{\Delta F}{fo}$ is designated by the letter a.

GENERAL CONSIDERATIONS

The ULN2111 is very versatile and easy to use. Only a few general requirements are needed.

1. As with any integrated circuit, especially those operating at high frequencies, the power supply at pin 13 should be bypassed with a ceramic disc of the 0.5μfd value range.
2. Amplifier gain is 60dB at high frequencies. This can be troublesome unless good high frequency layout techniques are practiced. Ground planes are very helpful and physical separation of inputs and outputs is mandatory.
3. A dc path less than 300Ω should be provided between pins 4 and 6.
4. Decoupling capacitor leads at pins 5, 6, and 12 should be as short as possible.
5. The maximum ac load current can be increased by adding an external resistor between pins 1 and 7. The minimum value for this resistor is 800Ω, giving a minimum load current of 4mA RMS.
6. A dc path less than 100Ω shall be provided between pins 2 and 12. No other biasing provisions are required.

CALCULATED TRANSFER CHARACTERISTICS FOR HIGH AND LOW LEVEL CASES

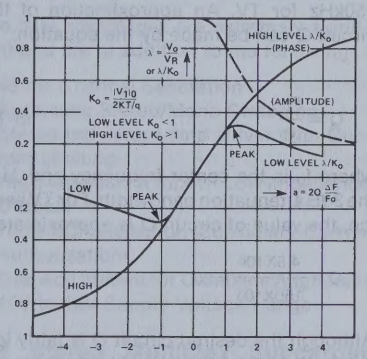


Figure 8-19

MEASURED CONVERSION EFFICIENCY OF THE MONOLITHIC FM DETECTOR

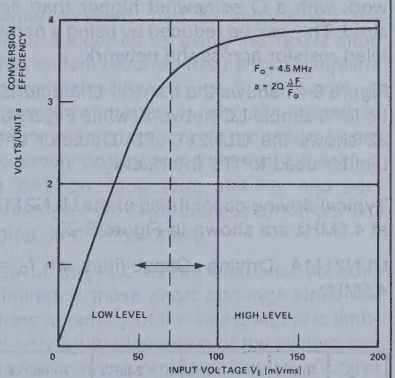


Figure 8-20

PERFORMANCE

In an FM detector and limiter, the major figures of merit include recovered audio amplitude, dynamic range, and total harmonic distortion.

Audio recovery is affected primarily by the resonant LC network and the injection level at the detector input.

To obtain a proper value for audio recovery, specific characteristics of the S curve are recommended. A choice of slope of the S curve gives a specified value for dV/dF, which is the basic expression of audio recovery. A choice of a peak-to-peak separation desired and a choice of peak-to-peak voltage required at the nodes of the S curve determine the Q of the LC resonant network and injection level.

The peak-to-peak separation is usually defined by the service for which the system is intended. This value is 550kHz for FM and 150kHz for TV. An approximation of the circuit Q can be made by the equation:

$$Q = \frac{F_o}{\Delta f} \qquad (8\text{-}15)$$

where f_o is the center frequency and Δf is the 3dB attenuation bandwidth. For TV service, the value of circuit Q is approximately

$$Q = \frac{4.5X10^6}{150X10^3} = 30$$

Although the desired circuit Q is fairly low (indicating a high-L network), it is desirable to use a high-C network. The input to the detector introduces some variable capacitance. This can be minimized through the use of at least 100pF as the C part of the resonant circuit. Inductor choice, along with this capacitance value, yields a network with a Q somewhat higher than desired. This can be reduced by using a paralleled resistor across the network.

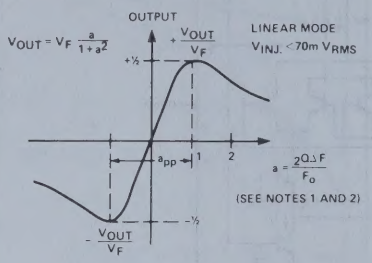
Figure 8-21 shows the transfer characteristic for a simple LC network, while Figure 8-22 shows the ULN2111 FM Detector and Limiter used for TV interfacing.

Typical driving capabilities of the ULN2111 at 4.5MHz are shown in Figure 8-23.

ULN2111A Driving Capabilities at f_o = 4.5MHz

Fig.	$R_L(\Omega)$	Δf = 7.5kHz	Δf = 24kHz	Remarks
A	2000	220	650	No Clipping
B	200	130	400	No Clipping
C	200	220	650	Clipping at V_o = 500Vrms

TRANSFER CHARACTERISTICS FOR A SIMPLE LC NETWORK



OUTPUT = f (NORMALIZED DEVIATION)
(The units along the vertical axis are arbitrary units.)

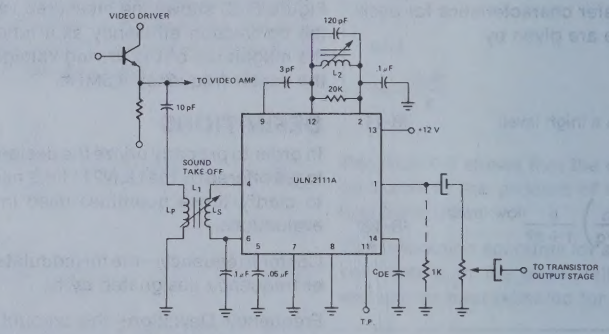
Linear mode: Operation of the FM detector with no limiting after the phase shift network.

NOTES

1. V_F defines the slope of the FM transfer characteristic, at origin:
$$V_f = \frac{dV_{out}}{da} \text{ at } a = 0$$
V_F is primarily a function of bias current in the detector and injection voltage.
V_F will decrease with decreasing V_{CC} or V_{inj}.
2. a = normalized frequency deviation:
$$A = \frac{20\Delta F}{F_o}$$
a = 1 for peak deviation

Figure 8-21

TV INTERFACING



All resistor values are in ohms

Figure 8-22

ULN2111A DRIVING CAPABILITIES AT f_o = 4.5 MHz

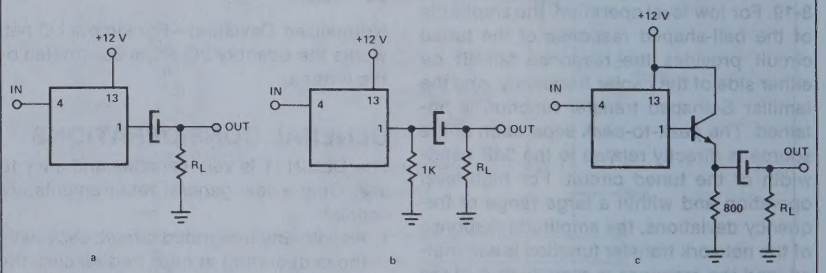


Fig.	R_L (Ω)	Δf = 7.5 kHz	Δf = 24 kHz	Remarks
A	2000	220	650	No Clipping
B	200	130	400	No Clipping
C	200	220	650	Clipping at V_o = 500 mV rms

All resistor values are in ohms

Figure 8-23

The final component required is a small decoupling capacitor placed between the network and the low amplifier output. To insure linear detector operation, the reactance of this capacitor should be substantially large, as compared to the impedance of the tuned circuit at resonance.

The voltage developed across the simple tank circuit is applied to the other two balanced gates of the coincidence detector through emitter follower Q1,which provides a capability for monitoring the LC network tuning without any appreciable loading effects. It also reduces, to a great degree, the capacitance reflected to a tuned circuit, leading to a negligible shift in the tuning as a function of incoming signal strength.

When designing the LC network it is necessary to provide the following requirements:

1. Capacitively drive the network from low impedance (pins 9 or 10).
2. Pins 2 and 12 should see a dc path less than 100 ohms.
3. The required V_2 (Figure 8-18) must be supplied at pin 12 by the network.
4. The phase of the network at fo must be $\pi/2$ or an odd multiple thereof.
5. To minimize output distortion a maximum normalized deviation (a) of less than .3 should be used.

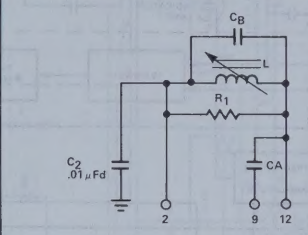
Figure 8-24 gives the recommended networks for use at 10.7MHz and 4.5MHz.

	COMPONENT VALUE	
	TV 4.5MHz	Fm 10.7MHz
L Inductance	7-14μH	1.5-3μH
L Nominal Q (unloaded)	50	50
L DC Resistance	50Ω	50Ω
C_A	3pF	4.7pF
C_B	120pF	120pF
R1	20k	3.0K
Network Q	30	20

The other factor governing audio output is the injection value at the input to the detector. The optimum value is 60mVrms at the resonant frequency of the network. Figure 8-20 shows a normalized plot of V_{inj} as a function of V_f, where V_f represents a normalized output for any single LC network. Note that the output (V_f) has a linear relationship to V_{inj} up to approximately 50mV. Above this value, the function breaks into a curve, then flattens out, indicating that the detector is in a switching mode.

Figures 8-25 and 8-26 demonstrate the detector operation in the linear (low injection) mode and the switching (high injection) mode. Note that in the linear mode, a greater portion of the S curve is linear, thus producing lower distortion than in the switching mode. For best operation, the low injection mode is recommended where V_{inj} is set as high as possible. The optimum injection value is 60mVrms.

TYPICAL PHASE SHIFT NETWORKS



	COMPONENT VALUE	
	TV 4.5 MHz	FM 10.7 MHz
L INDUCTANCE	7-14 μH	1.5 – 3μH
L NOMINAL Q (UNLOADED)	50	50
L DC RESISTANCE	50Ω	50Ω
C_A	3pF	4.7pF
C_B	120pF	120pF
R_1	20K	3.0K
NETWORK Q	30	20

Figure 8-24

FM TRANSFER CHARACTERISTICS LOW Vij OPERATION

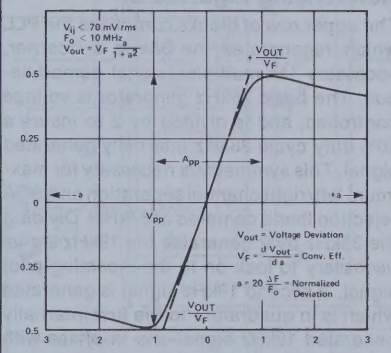


Figure 8-25

FM TRANSFER CHARACTERISTICS HIGH Vij OPERATION

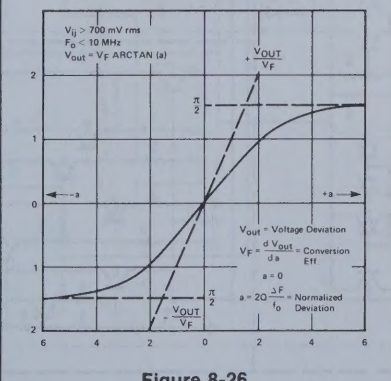


Figure 8-26

STEREO DECODER

Introduction

The phase locked loop (PLL) has been used for many years in consumer equipment. Due to the nature of FM STEREO MULTIPLEX SYSTEMS, where prime importance is the channel separation, discrete systems lacked the tracking ability over wide temperature and voltage ranges to be done economically.

The development of the monolithic PLL and improvements in IC processing has made the Phase Locked Loop FM Stereo Multiplexer Decoder a reality.

Major Advantages

The economic advantages in using the PLL multiplex decoding system are not only cost reduction, by eliminating peripheral components, but the man hour cost reduction by eliminating turning coils, thereby eliminating tedious alignment procedures.

The cost advantages are extremely signifcant and are in addition to the following:

- 45 dB Channel Separation
- Automatic Stereo/Mono Switching
- Stereo Indicator Lamp Driver With Current Limiting
- High Impedance Input—Low Impedance Outputs
- 70dB SCA Rejection (Subsidiary Carrier Authorization)
- One Adjustment for Complete Alignment
- 10V to 16V Supply Voltage Range

FM Stereo Multiplex Subcarrier and Pilot

The two (2) basic signals differentiating an FM stereo multiplex signal from an FM monaural signal are the 19kHz pilot and the 38kHz subcarrier. The frequency and phase relationship of these signals is well defined.

Earlier systems had to reconstruct the 38kHz subcarrier by using the 19kHz pilot. This system required frequency multipliers and selective filters (coils). Since maximum channel separation is directly related to proper phasing, alignment procedures were extremely critical and therefore expensive. In addition, long term stability and performance were degraded due to component aging, and temperature.

Use of the PLL as the multiplex decoder eliminated these short comings since the phase accuracy of the 38kHz signal is limited only by the loop gain of the system and the free running oscillator stability. Both of these parameters are easily controlled, providing easy, rapid adjustment and excellent long term stability.

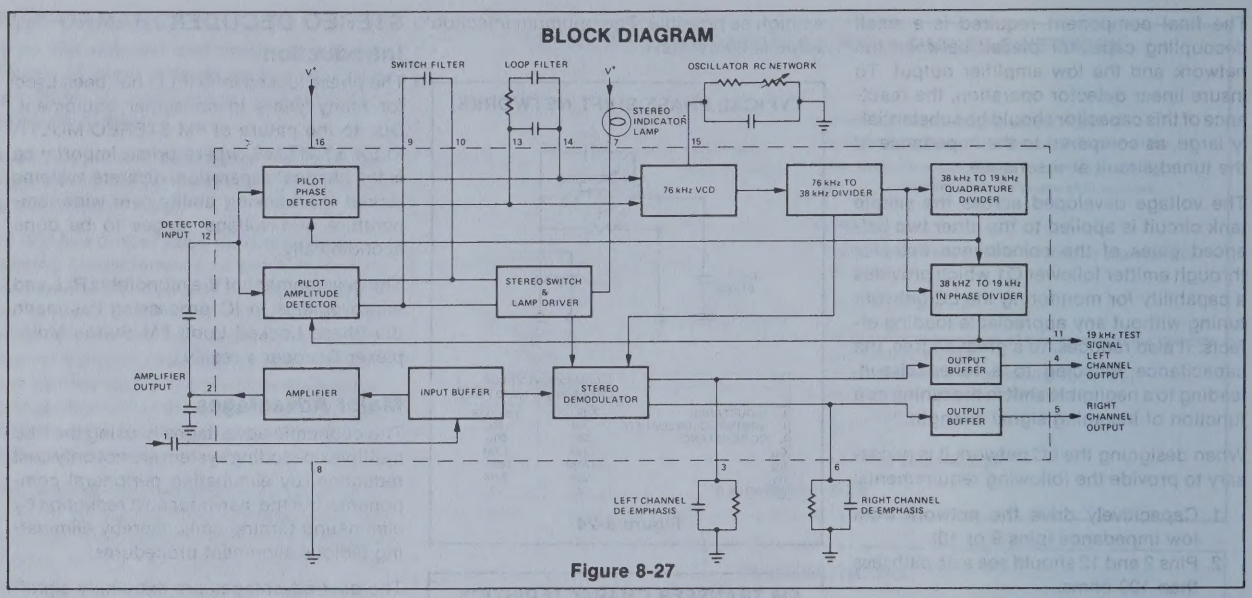


Figure 8-27

General Description

The μA758 is a monolithic Phase Locked Loop FM Stereo Multiplex decoder using the 16-LEAD Dip AA Package. This integrated circuit decodes an FM Stereo Multiplex Signal into Right and Left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. Internal functions include automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a wide supply voltage range and uses a low number of external components. It has only one control to adjust a potentiometer to set oscillator frequency. No external coils are required. The μA758 is suitable for all line-operated and automotive FM Stereo Receivers.

Referencing Figure 8-27

The upper row of blocks comprises the PLL which regenerates the 38kHz subcarrier, necessary for multiplex signal demodulation. The basic 76kHz generator is voltage controlled, and is divided by 2 to insure a 50% duty cycle 38kHz internally generated signal. This symmetry is necessary for maximum left/right channel separation and SCA rejection (band centered at 67kHz). Dividing the 38kHz by 2 generates the 19kHz signal necessary to lock on to the incoming pilot signal. A second 19kHz signal is generated which is in quadrature to the first internally generated 19kHz signal and in phase with the pilot. This second 19kHz is mixed in a quadrature (synchronous) phase detector to operate the stereo switch and lamp driver circuitry.

When a stereo signal is present, the stereo switch enables the stereo demodulator and when a stereo signal is not present the demodulator is disabled allowing the system to reach optimum noise performance.

Functional Operation

To aid in understanding the system operation, the μA758 equivalent circuit has been broken down into subsections as follows. Reference Figure 8-28.

I Buffer Amplifier and Bias Supplies
II Demodulator
III Stereo Switch and Lamp Driver
IV Voltage Controlled Oscillator
V Frequency Dividers
VI Pilot Phase and Amplitude Defectors

SIGNETICS LINEAR INTEGRATED CIRCUITS • μA758
Equivalent Circuit

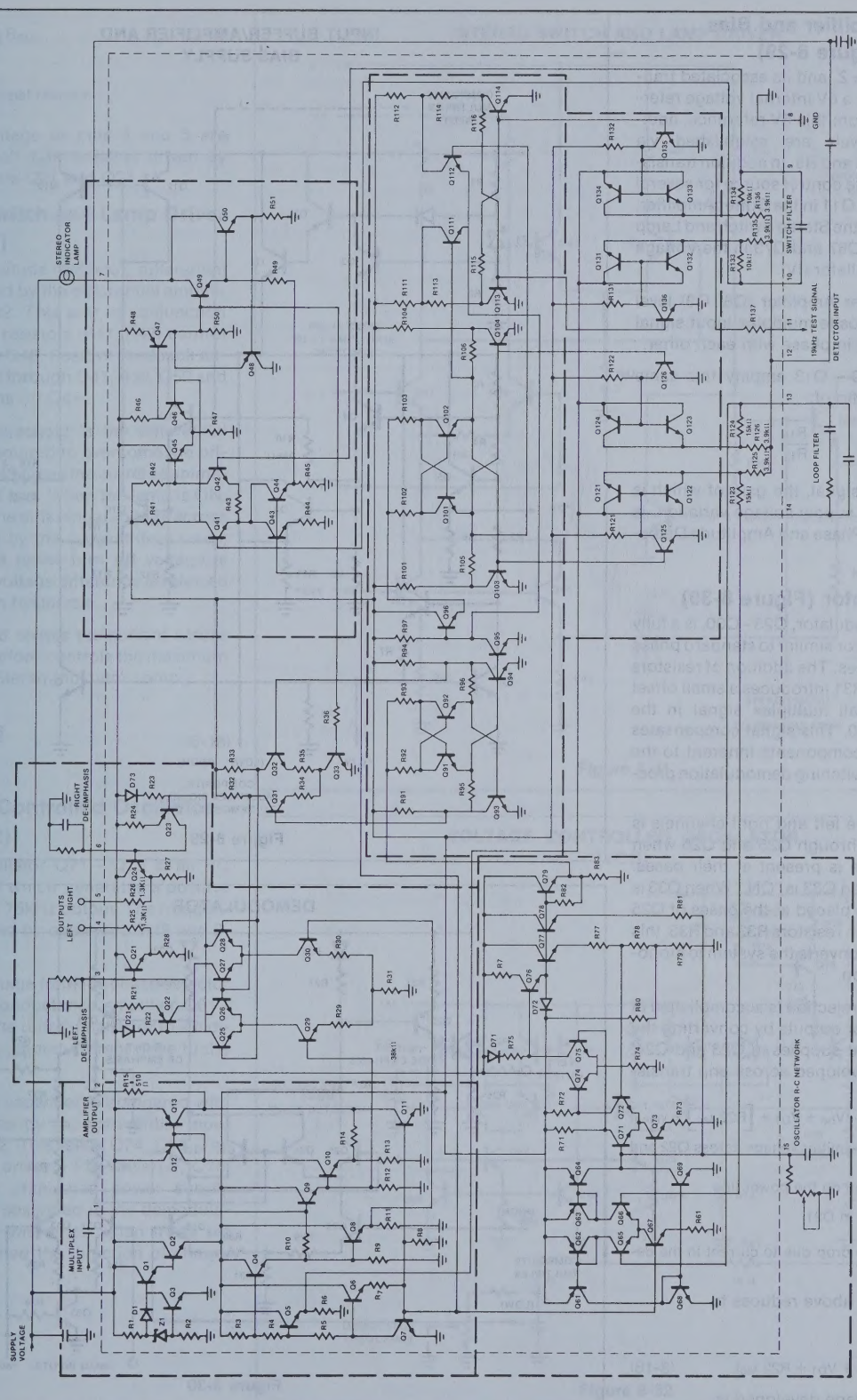


Figure 8-28

I Buffer Amplifier and Bias Supplies (Figure 8-29)

The zener diode Z, and its associated transistors generate a 6V internal voltage reference source. From this 6V reference, additional bias levels are established via resistors R3, R4, and R5. In addition transistor Q7 acts as the control source for several current mirrors; Q11 in the Buffer Amplifier, Q43 and Q44 in the Stereo Switch and Lamp Driver (III) and Q67 and Q73 in the Voltage Controlled Oscillator (IV).

The input Buffer Amplifier (Q8, Q9) level shifts the composite multiplex input signal to 2 levels each in phase with each other.

Transistors Q10 - Q13 amplify this same signal by the ratio of:

$$A = \frac{R_{14}}{R_{13}}$$

This amplified signal, the gain of which is independent of supply voltage variation, is fed to the Pilot Phase and Amplitude Detectors (VI).

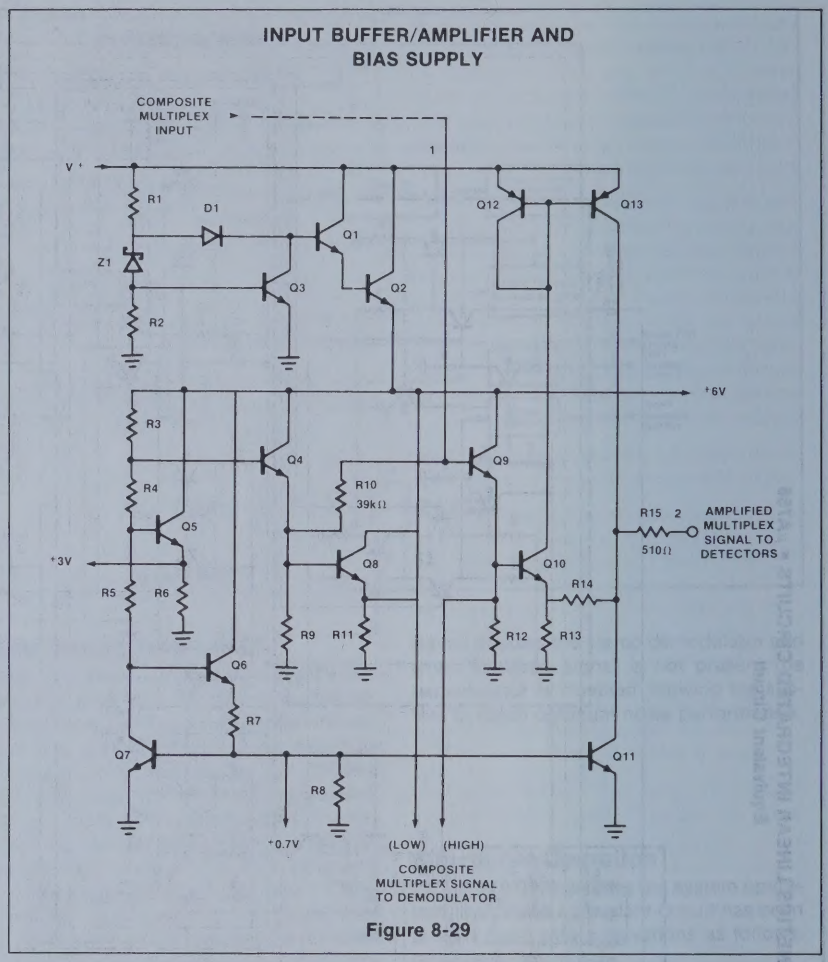


Figure 8-29

II Demodulator (Figure 8-30)

The basic demodulator, Q25 - Q30, is a fully balanced detector similar to standard phase locked loop types. The addition of resistors R29, R30, and R31 introduces a small offset to allow a small multiplex signal in the collector of Q30. This signal compensates the cross talk components inherent to the synchronous switching demodulation process.

Switching to the left and right channels is accomplished through Q25 and Q26 when the 38kHz drive is present at their bases. This occurs when Q33 is "ON." When Q33 is off, a dc bias is placed at the bases of Q25 and Q26 through resistors R32 and R33, this automatically converts the system to monophonic operation.

Supply voltage rejection is accomplished at the demodulator outputs by converting the audio to current supplies in Q23 and Q24. The voltage developed across pnp transistors is

$$V_e = (V^+ + v_{mod}) - (V_{be} + V_{D1} + \left[R22\ i_{ac}\right] + v_{mod})$$

where V_{be} = base-emitter voltage across Q22 and Q23

V_{mod} = modulation on the power line

V_{D1} = diode drop in D21

$(R22)i_{ac}$ = voltage drop due to current in the demodulator

Simplifying the above reduces to

$$V_e = V^+ - (V_{be} + V_{D1} + R22\ i_{ac}) \qquad (8\text{-}16)$$

The output voltage developed is

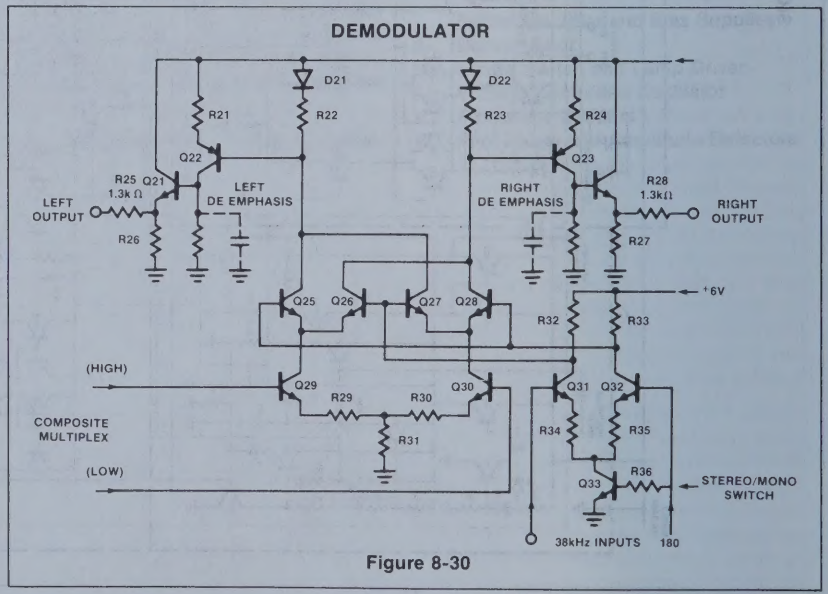


Figure 8-30

$$V_{out} = \left(\frac{V_e}{R21}\right) R_{ext} \qquad (8\text{-}17)$$

where R_{ext} = external resistor

The output voltage at pins 4 and 5 are provided through 1.3k resistors driven by Emitter Followers Q21 and Q24.

III Stereo Switch and Lamp Driver (Figure 8-31)

The pilot amplitude detector differential voltage is sensed by the differential amplifier Q41 and Q42. This pair in conjunction with their load resistors (R41, R42) control amplifiers Q45, Q46. Positive feedback action is achieved through Q47, R50, Q50 and R46 (which turns off Q44).

The turn on threshold is the differential input voltage required to overcome the offset voltage in R43 times the current summation of I_{R44} and I_{R45}. When the lamp is ON, Q44 is off and the differential voltage across R43 is reduced by the amount ($I_{R45} \times R_{43}$), which means a lower turn off voltage is required. This voltage difference is referred to as the switch hysteresis.

Transistors Q48 senses the current across R51 which therefore controls the maximum current in the Stereo Indicator Lamp.

$$I_{max} = \frac{V_{be\ Q48}}{R151} \qquad (8\text{-}18)$$

IV Voltage Controlled Oscillator (Figure 8-32)

The basic oscillator Q71 - Q79 is an RC relaxation type which generates a positive low duty cycle, 76kHz output. The frequency is established by equations 8-19 and 8-20.

The control voltage from the phase detector into the transconductance amplifier Q61 - Q69 converts the differential error to a bidirectional single ended current drive to the oscillator.

Voltage on the capacitor is compared with the set voltages by the differential input stage Q71, Q72. This feeds Q74, Q75. The output of Q75 drives a PNP inverter, Q76, (whose action eliminates power supply modulation as described in the demodulator section of this note), when these set limits are reached the direction of charge reverses.

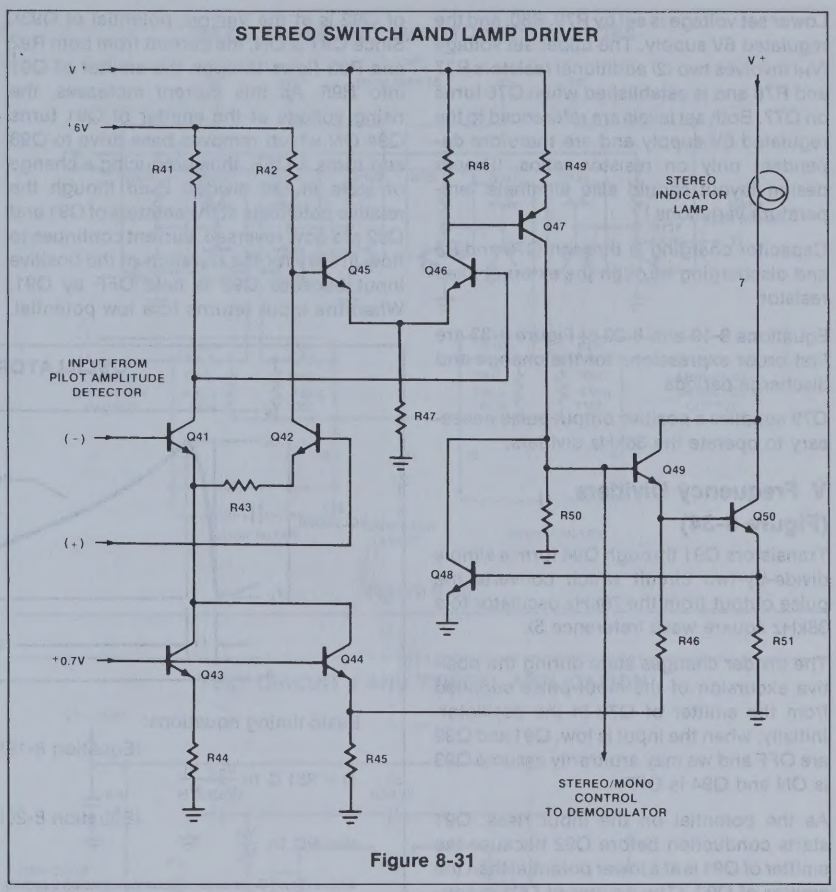


Figure 8-31

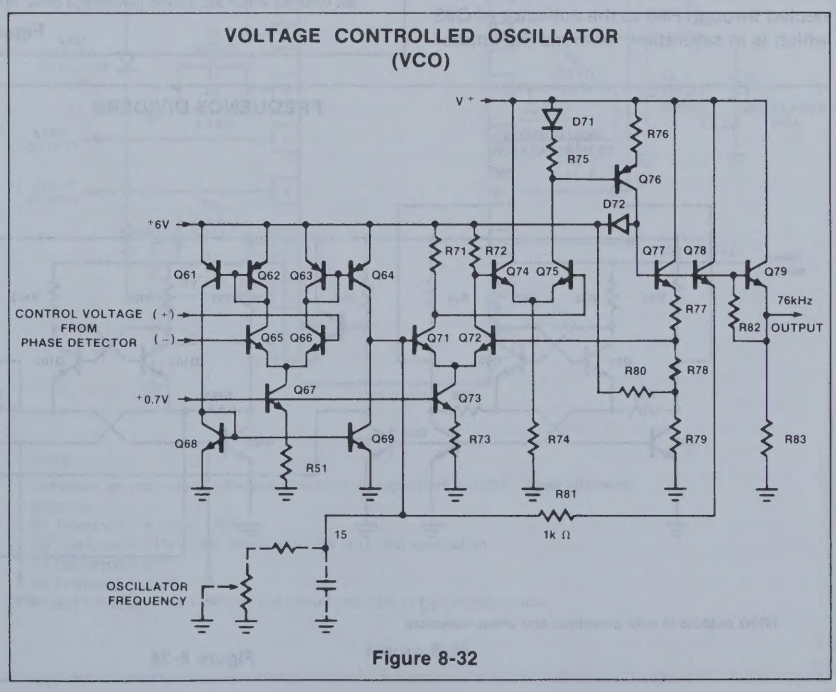


Figure 8-32

Lower set voltage is set by R79, R80, and the regulated 6V supply. The upper set voltage (V_H) involves two (2) additional resistors R77 and R78 and is established when Q76 turns on Q77. Both set levels are referenced to the regulated 6V supply and are therefore dependent only on resistor ratios. (Proper design layout should also eliminate temperature variations.)

Capacitor charging is through Q78 and R8 and discharging through the external fixed resistor.

Equations 8-19 and 8-20 of Figure 8-33 are first order expressions for the change and discharge periods.

Q79 supplies a positive output pulse necessary to operate the 38kHz dividers.

V Frequency Dividers (Figure 8-34)

Transistors Q91 through Q94 form a simple divide-by-two circuit which converts the pulse output from the 76kHz oscillator to a 38kHz square wave (reference 5).

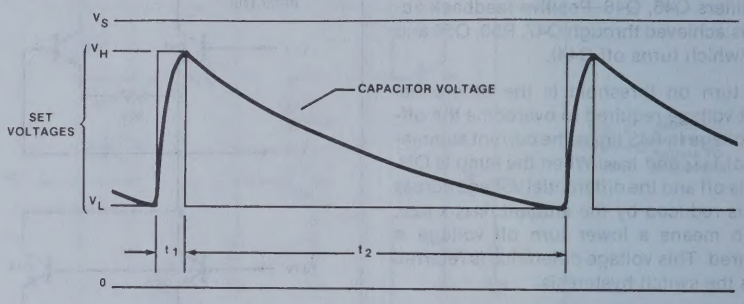
The divider changes state during the positive excursion of the input pulse supplied from the emitter of Q79 in the oscillator. Initially, when the input is low, Q91 and Q92 are OFF and we may arbitrarily assume Q93 is ON and Q94 is OFF.

As the potential on the input rises, Q91 starts conduction before Q92 because the emitter of Q91 is at a lower potential than the emitter of Q92. (The emitter of Q91 is connected through R95 to the collector of Q93 which is in saturation, whereas the emitter of Q92 is at the $V_{BE(ON)}$ potential of Q93). Since Q91 is ON, the current from both R92 and R93 flows through the emitter of Q91 into R95. As this current increases, the rising voltage at the emitter of Q91 turns Q94 ON which removes base drive to Q93 and turns it OFF, thus producing a change of state in the divider. Even though the relative potentials at the emitters of Q91 and Q92 are now reversed, current continues to flow in Q91 for the duration of the positive input because Q92 is held OFF by Q91. When the input returns to a low potential, Q91 turns OFF. The divider remains in its present state until driven by the next positive going input.

Oppositely phased 38kHz outputs to the demodulator are taken from the collectors of Q93 and Q94. Transistors Q95 and Q96 are used to drive the two 38kHz dividers.

The 38kHz Quadrature Divider has an identical configuration to the 76kHz divider. A change of state occurs with each positive excursion of the 38kHz input signal from the emitter of Q96.

OSCILLATOR WAVEFORMS



Basic timing equations:

(Equation 8-19)

$$t1 = R81\ C\ 1n\ \frac{V_S - V_L}{V_S - V_H}$$

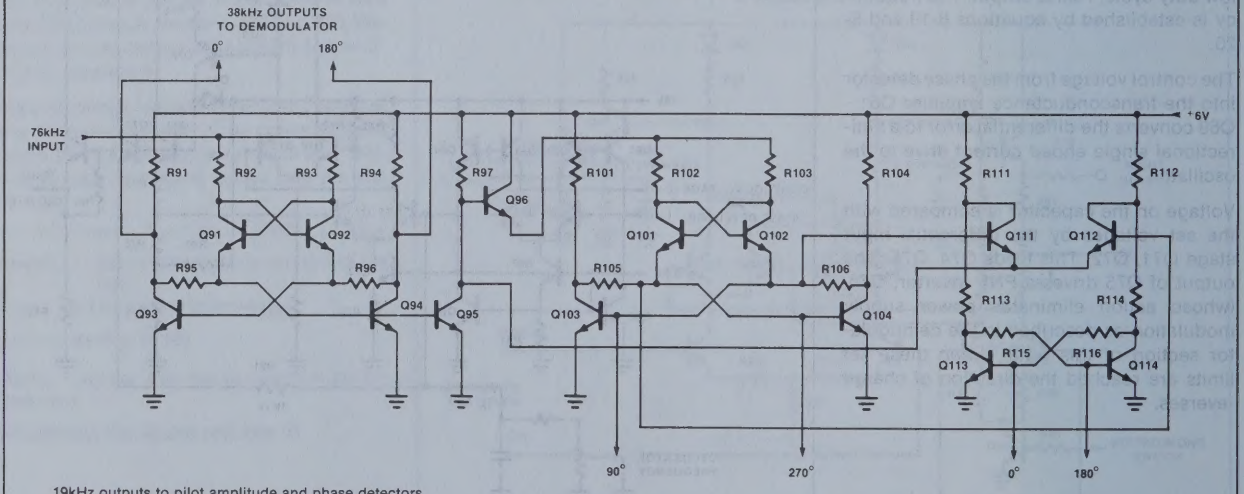
(Equation 8-20)

$$t2 = RC\ 1n\ \frac{V_H}{V_L}$$

where R and C are external components on Lead 15, R81 is on the chip, and V_H and V_L are set voltages which are a fixed percentage of V_S, the internally regulated 6 Volt supply.

Figure 8-33

FREQUENCY DIVIDERS



19kHz outputs to pilot amplitude and phase detectors.

Figure 8-34

The 38kHz In-Phase divider contains a bistable pair, Q113 and Q114, steered by inputs into Q111 and Q112, (a 38kHz input from the collector of Q95, and 19kHz inputs from the bases of Q103 and Q104). If the 19kHz input to the base of Q111 is high when the 76kHz divider turns Q95 ON, Q111 conducts and removes drive to Q114, changing the state of the bistable pair, Q113 and Q114. The bistable remains in this state until the next 38kHz turn on of Q95 which, this time, turns Q112 ON, removes drive to Q113 and resets the bistable pair. The resulting 19kHz output from Q113 and Q114 is at 90 degrees to the Quadrature Divider output with no ambiguity in phasing.

Pilot Phase and Amplitude Detectors

The pilot phase detector and pilot amplitude detector as shown in Figure 8-35 are synchronous, balanced chopper types which develop differential output signals across external filters. Back-to-back NPN transistor pairs are used for each switch to insure minimum drop regardless of signal polarity without reliance on inverse NPN beta characteristics.

The chopper transistors (Q121 through Q124), in the phase detector are driven from the 38kHz Quadrature Divider through transistors Q125 and Q126. The input signal is supplied from lead 12 through resistors R125 and R126. A differential output is developed across the loop filter, comprised of resistors R123 and R124 and the external R-C network between leads 13 and 14.

The pilot amplitude detector (Q131 through Q136), has an identical configuration to the phase detector. Since it operates with drive which is in phase with the pilot signal (90 degrees from the drive to the phase detector), its output is proportional to the amplitude of the pilot component of the multiplex signal. The differential output at leads 9 and 10 is filtered by the external capacitor on these two leads.

A reference 19kHz square wave signal is taken from the collector of drive transistor Q136 through resistor R137 to lead 11. It has the same phasing as the pilot contained in the multiplex input signal.

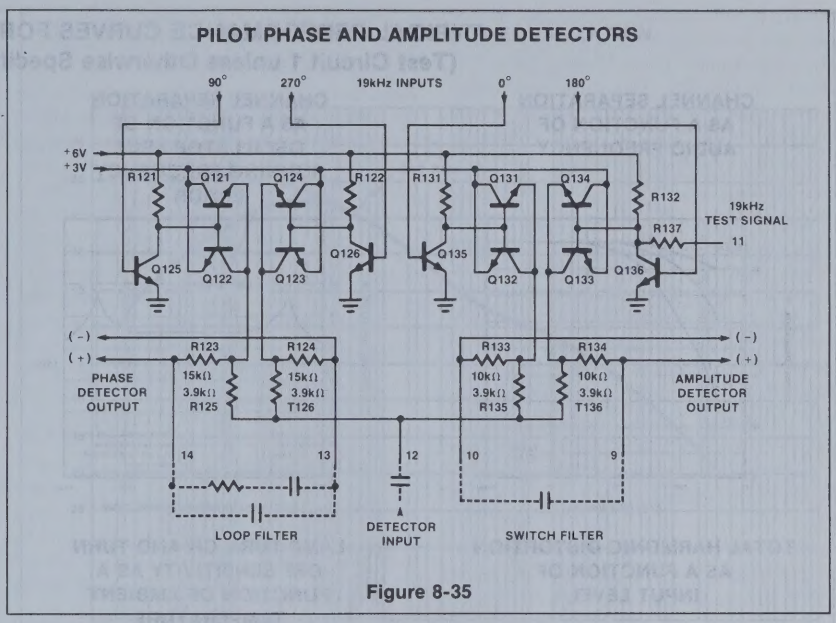
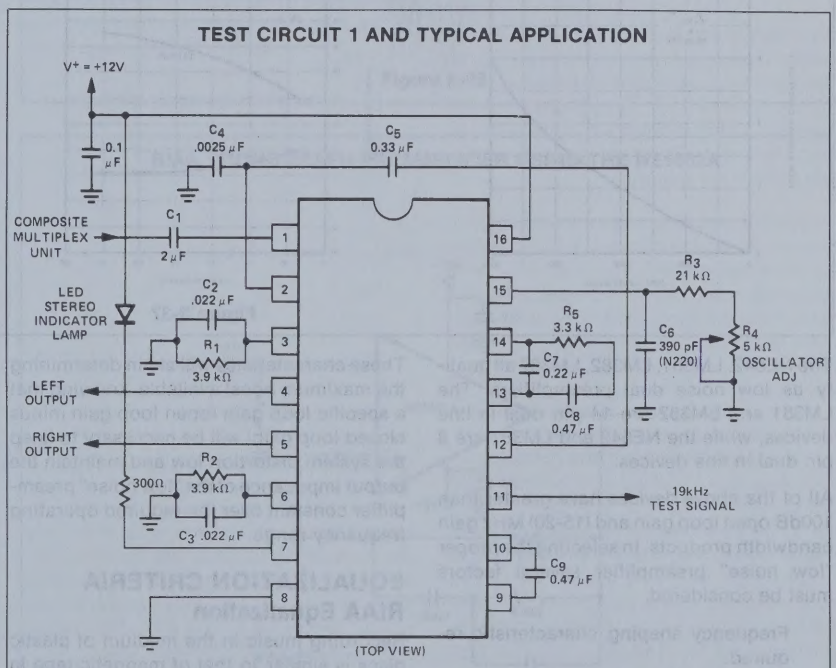


Figure 8-35



NOTE

Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified.
C1 Tolerance = + 100%, −20%
C6 Tolerance = ±1% in test circuit and ±5% in typical application
R3 Tolerance = ±1%
R4 Tolerance = ±10%
R1 and R2 Tolerances = ±1% in test circuit and ±5% in typical application.

Figure 8-36

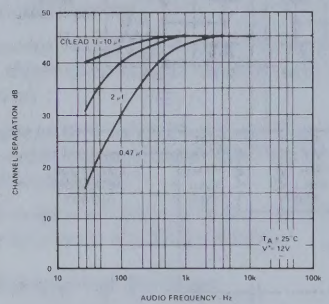
STEREO PREAMPLIFIERS

Introduction

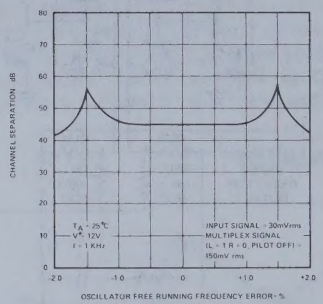
Stereo preamplifiers have come into greater and greater demand with the increased usage of tape recorders. With stereophonic recording systems, the need increased to have multiple devices in the same package to insure greater thermal tracking and packing density, without sacrificing performance.

TYPICAL PERFORMANCE CURVES FOR 758C
(Test Circuit 1 unless Otherwise Specified)

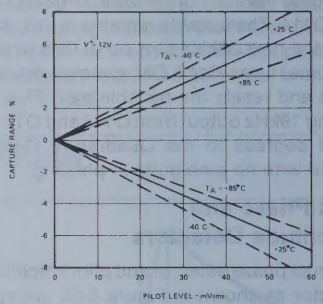
CHANNEL SEPARATION AS A FUNCTION OF AUDIO FREQUENCY



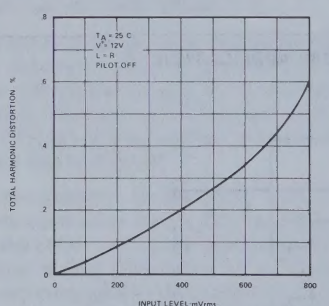
CHANNEL SEPARATION AS A FUNCTION OF OSCILLATOR FREE RUNNING FREQUENCY ERROR


CHANNEL SEPARATION - dB
T_A = 25°C
V⁺ = 12V
f = 1 KHz
INPUT SIGNAL = 30mVrms
MULTIPLEX SIGNAL
(L + R = 0, PILOT OFF) =
150mV rms
OSCILLATOR FREE RUNNING FREQUENCY ERROR - %

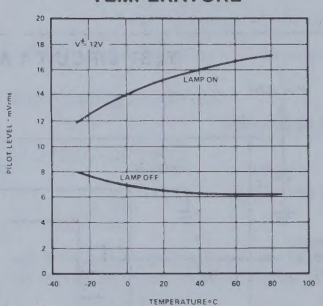
CAPTURE RANGE AS A FUNCTION OF PILOT LEVEL



TOTAL HARMONIC DISTORTION AS A FUNCTION OF INPUT LEVEL



LAMP TURN ON AND TURN OFF SENSITIVITY AS A FUNCTION OF AMBIENT TEMPERATURE



OSCILLATOR FREE RUNNING FREQUENCY ERROR AS A FUNCTION OF AMBIENT TEMPERATURE

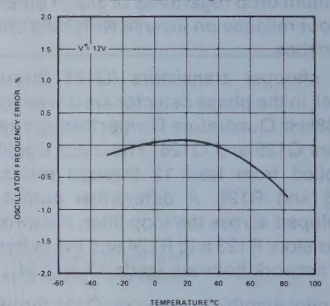


Figure 8-37

The NE542, LM381, LM382, LM387 all qualify as low noise dual preamplifiers. The LM381 and LM382 are 14 pin dual in line devices, while the NE542 and LM387 are 8 pin dual in line devices.

All of the above devices have greater than 100dB open loop gain and (15-20) MHz gain bandwidth products. In selecting the proper "low noise" preamplifier several factors must be considered.

I Frequency shaping characteristic required.
II Closed loop response with respect to a system reference level.
III Response of the record/playback head.
IV System distortion requirements.
V Response of the tape used.

The following will deal with items I, II, IV.

When approaching the design criteria of Item 2, the designer should be concerned with the open loop device characteristics. These characteristcs will aid in determining the maximum boost available, knowing that a specific loop gain (open loop gain minus closed loop gain) will be necessary to keep the system distortion low and maintain the output impedance of the "low noise" preamplifier constant over the required operating frequency range.

EQUALIZATION CRITERIA

RIAA Equalization

Recording music in the medium of plastic discs is similar to that of magnetic tape in that neither system exhibits a linear amplitude vs frequency response. Compensation is therefore necessary with records as it was with tape. The standard equalization is known as the RIAA curve and is shown in Figure 8-38, with its corner or turn over frequencies.

Many phono cartridges do not require preamplification. The ceramic and crystal types produce voltage larger than 100mV.

STANDARD RIAA EQUALIZATION CURVE

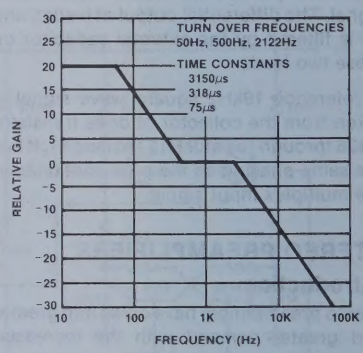


Figure 8-38

Magnetic types, however, produce small voltages in the neighborhood of 5mV and require preamplification.

RIAA standards call for a maximum recording velocity of 21cm/sec for stereo discs. This worst case velocity describes a bound for the preamplifier gain because the input signal at this velocity is maximum. The maximum undistorted output voltage of the PA239 is 1.25 volts rms. This voltage divided by the output voltage of the cartridge at 21cm/sec velocity defines the highest gain permissible without distortion. This maximum is assumed to be 40dB at 1kHz for the following example. As seen from Figure 8-36, the RIAA curve accounts for 20dB base boost from 50Hz to 500Hz and 20dB of treble out from 2122Hz to 21kHz.

RIAA EQUALIZATION AUDIO PREAMPLIFIER USING NE5532A

With the onset of new recording techniques along with sophisticated playback equipment, a new breed of low noise operational amplifiers was developed to complement the state-of-the-art in audio reproduction. The first ultra low noise op amp introduced by Signetics was called the NE5534A. This is a single operational amplifier with less than $4nV/\sqrt{Hz}$ input noise voltage. The NE5534A is internally compensated at a gain of three. This device has been used in many audio preamp and equalizer (active filter) applications since its introduction early last year.

Many of the amplifiers that are being designed today are dc coupled. This means that very low frequencies (2-15Hz) are being amplified. These low frequencies are common to turntables because of rumble and tone arm resonancies. Since the amplifiers can reproduce these sub-audible tones, they become quite objectionable because the speakers try to reproduce these tones. This causes non-linearities when the actual recorded material is amplified and converted to sound waves.

The RIAA has proposed a change in its standard playback response curve in order to alleviate some of the problems that were previously discussed. The changes occur primarily at the low frequency range with a slight modification to the high frequency range. (See Figure 8-39). Note that the response peak for the bass section of the playback curve now occurs at 31.5Hz and begins to roll off below that frequency. The rolloff occurs by introducing a fourth R/C network with a 7950μs time constant to the three existing networks that make up the equalization circuit. The high end of the equalization curve is extended to 20kHz, because recordings at these frequencies are achievable on many current discs.

PROPOSED RIAA PLAYBACK EQUALIZATION

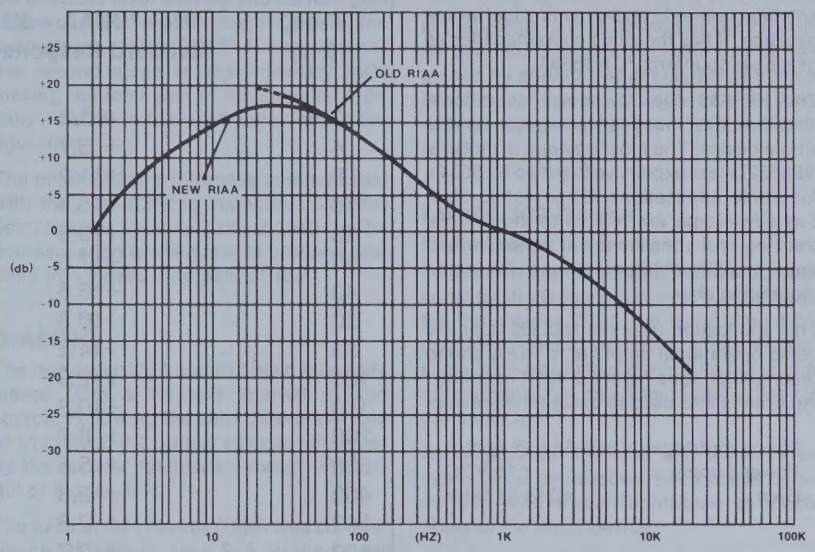
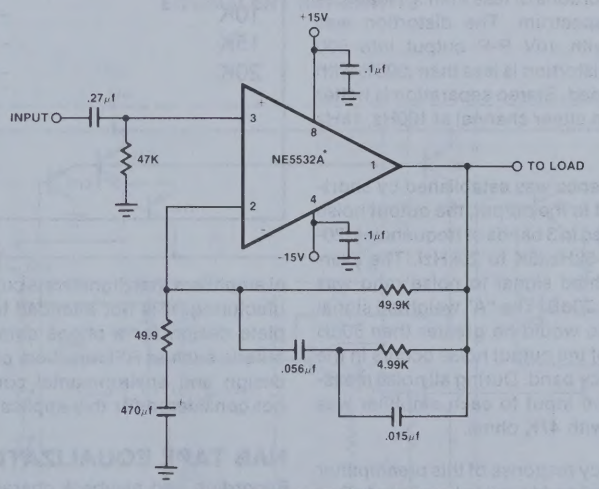


Figure 8-39

RIAA PHONOGRAPH PREAMPLIFIER USING THE NE5532A



* 1/2 OF DUAL OPERATIONAL AMPLIFIER

NOTE
All resistors are 1% metal film and are valued in ohms.

Figure 8-40

Signetics has recently introduced a new dual, low noise operational amplifier that is internally compensated to unity gain. It is called the NE5532. This dual operational amplifier comes in an 8-pin mini dual in-line package. It has the same characteristics as its single counterpart, NE5534.

The NE5532 dual low noise operational amplifier has many advantages over the single device. The most obvious is that one NE5532 is less expensive than two NE5534's for stereo applications. Some not so obvious advantages are related to the thermal tracking and consistency of parameters of both amplifiers integrated on the same monolithic chip.

This application uses the NE5532 dual low noise operational amplifier in RIAA phono preamplifier. (See Figure 8-40). The following criteria was used to design the preamp:

Phono cartridge output	5mv @ 5cm/S
Power Supply	±15 VDC
Gain	40dB @ 1kHz

The RIAA recording characteristic establishes a maximum recording velocity of 25cm/S; therefore the maximum input to the preamp is 25mV RMS. Since the NE5532A is internally compensated for unity gain, at least 34dB of feedback exists for a 10MHz gain bandwidth product.

Laboratory measurements of this preamp showed distortions of less than .01% across the audio spectrum. The distortion was measured with 10V P-P output into 600 ohms. The distortion is less than .005% with a 10K ohm load. Stereo separation is better than 70dB on either channel at 100Hz, 1kHz and 10kHz.

After a reference was established by shorting the input to the output, the output noise was measured in 3 bands of frequencies (20-500Hz) (500-5kHz)(5K to 20kHz). The average unweighted signal to noise ratio was greater than 70dB. The "A" weighted signal to noise ratio would be greater than 80dB since most of the output noise occurs in the first frequency band. During all noise measurements, the input to each amplifier was terminated with 47K ohms.

The frequency response of this preamplifier was measured and found to be within 1dB of the new standard theoretical response. The measured and theoretical values are tabulated in Figure 8-41 of this report.

This application is intended to demonstrate the qualities of the new low noise operational amplifiers that Signetics is currently manufacturing. It is not intended to be a complete design for a phone amplifier. Other criteria such as RFI rejection, power supply design and environmental conditions are not considered for this application.

TABULATED MEASURED DATA

Freq. (Hz)	"New" RIAA - dB Standard Response	Measured Response(dB) Side A	Side B
2	- 0.2	+ 1.4	+ 1.0
4	+ 5.7	+ 4.8	+ 5.1
8	+11.2	+11.8	+11.6
16	+15.4	+15.8	+15.6
20	+16.3	+16.3	+16.2
30	+17.0	+16.6	+16.9
40	+16.8	+16.3	+16.2
50	+16.3	+15.7	+16.0
80	+14.2	+13.6	+13.9
100	+12.9	+12.3	+12.2
150	+10.3	+ 9.6	+ 9.7
200	+ 8.2	+ 7.9	+ 7.8
300	+ 5.5	+ 5.0	+ 5.1
400	+ 3.8	+ 3.5	+ 3.4
500	+ 2.6	+ 2.4	+ 2.3
800	+ 0.7	+ 0.7	+ 0.6
1K	0.0	0.0	0.0
1.5K	- 1.4	- 1.3	- 1.3
2K	- 2.6	- 2.6	- 2.5
3K	- 4.8	- 4.4	- 4.7
4K	- 6.6	- 6.2	- 6.3
5K	- 8.2	- 8.0	- 8.0
6K	- 9.6	- 9.2	- 9.4
8K	-11.9	-11.5	-11.8
10K	-13.7	-13.4	-13.2
15K	-17.2	-16.6	-17.0
20K	-19.6	-19.0	-19.1

Figure 8-41

NAB TAPE EQUALIZATION

Recording and playback characteristics of magnetic tape and record/playback heads are not flat but exhibit a loss at high frequencies and a boost at lower frequencies. To obtain an overall flat frequency response and improved signal to noise ratio, the audio signals are equalized by boosting the higher frequencies in amplitude before recording. Playback amplifiers must exhibit bass boost to remove the effects of pre-emphasis for an overall flat response.

Known as the NAB equalization curve, the standard deemphasis employs attenuation from the turnover frequency of 50Hz to the turnover frequency of 3180Hz for 7 1/2 Ips recording. The slower recording speed of 3.75 Ips employs turnover frequencies of 50Hz and 1326Hz. These curves are shown in Figure 8-37. A reference level of 800μV head sensitivity at 1kHz is also used by the NAB.

STEREO PREAMPLIFICATION

The voltage level appearing at the output of tape playback heads and some phono cartridges are too small to be useful without a large amount of low noise preamplification. In addition to providing low noise amplification, the preamplifier should possess enough open loop gain so that the RIAA and NAB equalization curves can be produced in the feedback networks of the amplifier. The following paragraphs describe the characteristics and applications of the 542, LM381/382 and the PA239. These devices provide a matched pair of amplifiers which have been specifically designed to minimize amplifier noise and maximize signal to noise ratio.

542 DEVICE DESCRIPTION

The NE542 is a dual low noise amplifier with 104dB open loop gain produced by two stages of voltage gain followed by one stage of current gain.

In the design of low noise devices special attention must be focused on the input stage. If differential topography is used, the stage should be designed so that one of the differential transistors is turned off. This reduces the noise contribution by a factor of 1.4 since only one transistor is producing noise. Current sources and mirrors cannot be used for biasing loads because active elements will contribute more noise.

Implementing these observations, the first gain stage of the 542 is pictured with the complete schematic by Figure 8-43.

Although the differential input configuration degrades the noise performance slightly, using differential inputs has the advantages of higher input impedance, allowing smaller capacitors and larger resistors to be used to achieve the RIAA and NAB curves.

TAPE EQUALIZATION CURVES

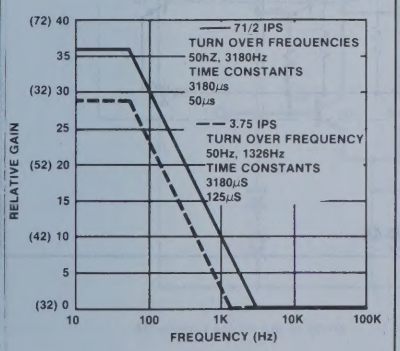


Figure 8-42

The second stage is a common-emitter amplifier (Q5) with a current source load (Q6). The Darlington emitter-follower Q3-Q4 provides level shifting and current gain to the common-emitter stage (Q5) and the output current sink (Q7). The voltage gain of the second stage is approximately 2000 making the total gain of the amplifier typically 160,000 in the differential input configuration.

The preamplifier is internally compensated with the pole-splitting capacitor, C1. This compensates to unity gain at 15MHz. The compensation is adequate to preserve stability to a closed loop gain of 10.

BIASING

The non-inverting input has been internally biased from a 1.4 Volt internal voltage source. Following the zero differential rule of amplifiers, the output voltage will be set by the resistor feedback network (R4 and R5) of Figure 8-44.

The base of Q2 requires 0.5μA bias current. Hence R5 should pass 5μA minimum for stability, for an output dc voltage of $\frac{V_{CC}}{2}$ the values of R4 and R5 are:

$$R5 = \frac{2\ V_{BE}}{10\ I_B} = 240K\ \text{Max.} \qquad (8\text{-}19)$$

$$R4 = \left(\frac{V_{CC}}{2.8 - 1}\right) R5 \qquad (8\text{-}20)$$

DC amplifier gain is defined by the ratio of R4 and R5. Open loop ac gain can be regained by adding a shunt capacitor across R5. The low frequency 3dB corner is then defined by the capacitor-resistor break point.

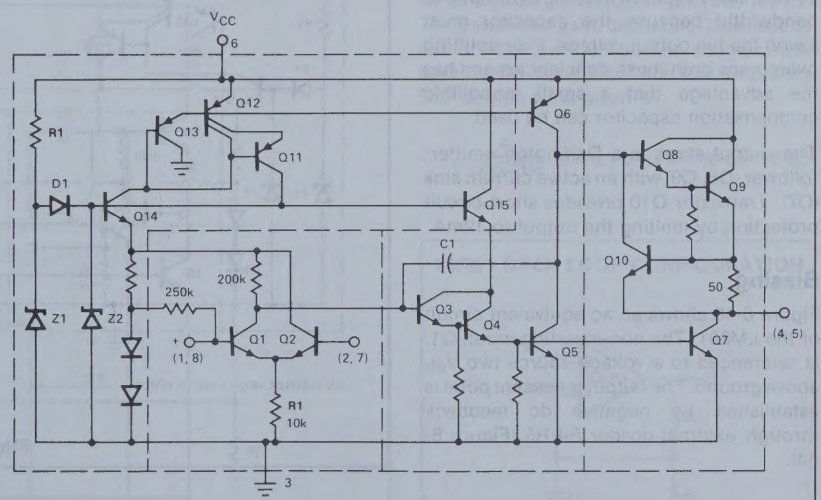
LM381/382 Device Description

To achieve low noise performance, special consideration must be taken in the design of the input stage. First, the input should be capable of being operated single ended; since both transistors contribute noise in a differential stage degrading input noise by the factor $\sqrt{2}$.

Secondly, both the load and biasing elements must be resistive; since active components would each contribute as much noise at the input device.

The basic input stage, Figure 8-45, can operate as a differential or single ended amplifier. For optimum noise performance Q2 is turned OFF and feedback is brought to the emitter Q1.

EQUIVALENT SCHEMATIC



All resistor values are in ohms

Figure 8-43

In applications where noise is less critical, Q1 and Q2 can be used in the differential configuration. This has the advantage of higher impedance at the feedback summing point, allowing the use of larger resistors and smaller capacitors in the one control and equalization networks.

The schematic diagram of Figure 8-45 is divided into the first and second voltage gain stages, the current gain stage, and the bias regulator.

The second stage is a common-emitter amplifier (Q5) with a current source load (Q6). The Darlington emitter-follower Q3-Q4 provides level shifting and current gain to the common-emitter stage (Q5) and the output current sink (Q7). The voltage gain of the second stage is approximately 2000 making the total gain of the amplifier typically 160,000 in the differential input configuration.

The preamplifier is internally compensated with the pole-splitting capacitor, C1. This compensates to unity gain at 15MHz. The compensation is adequate to preserve stability to a closed loop gain of 10. Compensation for unity gain closure may be provided with the addition of an external capacitor in parallel with C1.

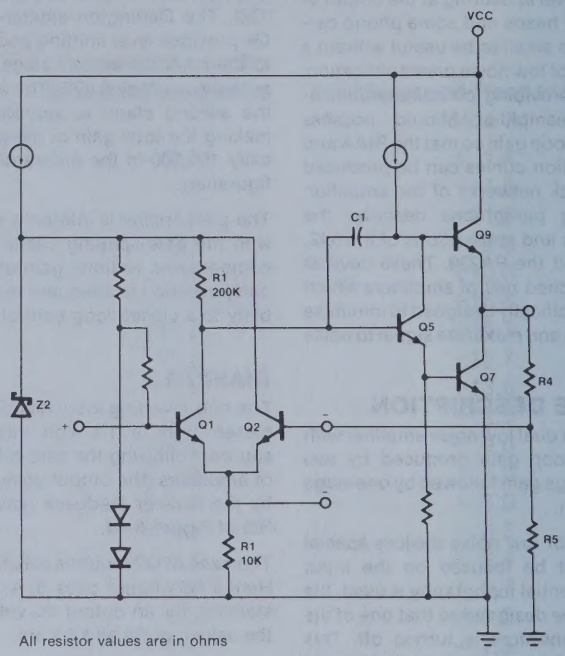
Three basic compensation schemes are possible for this amplifier; first stage pole, second stage pole and pole-splitting. First stage compensation will cause an increase in high frequency noise because the first stage gain is reduced, allowing the second stage to contribute noise. Second stage compensation causes poor slew rate (power bandwidth) because the capacitor must swing the full output voltage. Pole-splitting overcomes both these deficiencies and has the advantage that a small monolithic compensation capacitor can be used.

The output stage is a Darlington emitter-follower (Q8, Q9) with an active current sink (Q7). Transistor Q10 provides short-circuit protection by limiting the output to 12mA.

Biasing

Figure 8-46 shows an ac equivalent circuit of the LM381. The non-inverting input, Q1, is referenced to a voltage source two V_{BE} above ground. The output quiescent point is established by negative dc feedback through external divider R4/R5 (Figure 8-44).

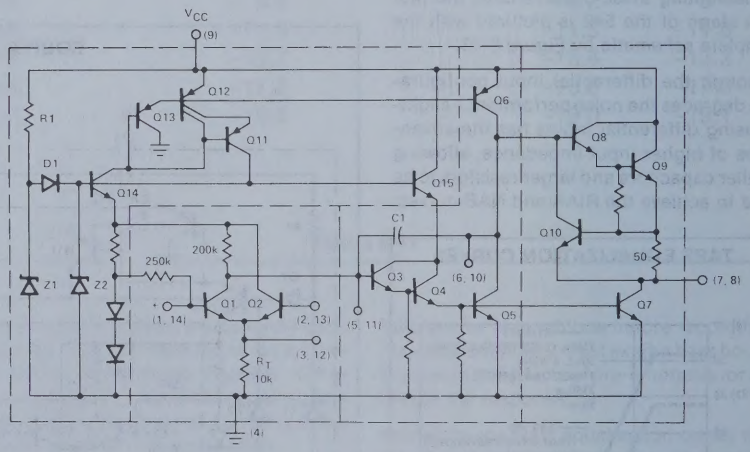
DIFFERENTIAL INPUT BIASING



All resistor values are in ohms

Figure 8-44

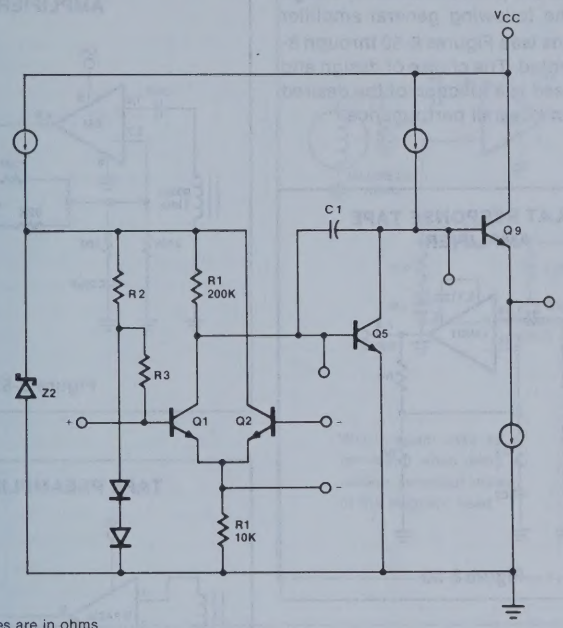
LM381 SCHEMATIC DIAGRAM



All resistor values are in ohms

Figure 8-45

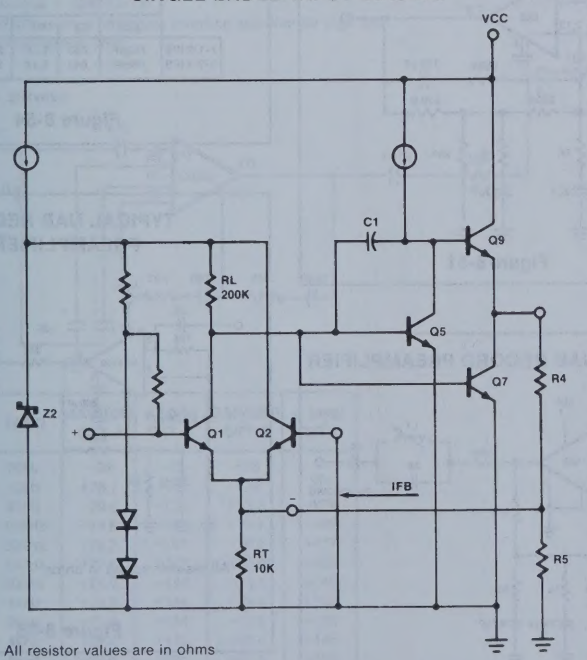
AC EQUIVALENT CIRCUIT



All resistor values are in ohms

Figure 8-46

SINGLE ENDED INPUT BIASING



All resistor values are in ohms

Figure 8-47

For bias stability, the current through R5 is made ten times the input current of Q2 (≈0.5μA). Then, for the differential input, resistors R5 and R4 are:

$$R5 = \frac{2V_{BE}}{10\ I_{Q2}} = \frac{1.2}{5 \times 10^{6}} = 240k\Omega \text{ MAX.} \quad (8\text{-}21)$$

$$R4 = \left(\frac{V_{CC} - 1}{2.4}\right) R5 \quad (8\text{-}22)$$

When using the single ended input, Q2 is turned OFF and dc feedback is brought to the emitter of Q1 (Figure 8-41). The impedance of the feedback summing point is now two orders of the magnitude lower than the base of Q2 (≈ 10kΩ).

Therefore, to preserve bias stability, the impedance of the feedback network must be decreased. In keeping with reasonable resistance values, the impedance of the feedback voltage source can be 1/5 the summing point impedance.

The feedback current is less than 100μA worst case. Therefore, for single ended input, resistors R5 and R4 are:

$$R5 = \frac{V_{BE}}{5\ I_{FB}} = \frac{0.6}{5 \times 10^{4}} = 1200\Omega\text{MAX.} \quad (8\text{-}23)$$

$$R4 = \left(\frac{V_{CC} - 1}{1.2}\right) R5 \quad (8\text{-}24)$$

The circuits of Figures 8-44 and 8-47 have an ac and dc gain equal to the ratio R4/R5. To open the ac gain, capacitor C2 is used to shunt R5 (Figure 8-48). The ac gain now approaches open loop. The low frequency 3dB corner, f_o, is given by:

$$f_o = \frac{A_0}{2\pi C2R4} \text{ where: } A_0 \text{ open loop gain} \quad (8\text{-}25)$$

LM381 OPEN LOOP CONFIGURATION

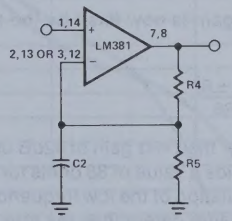


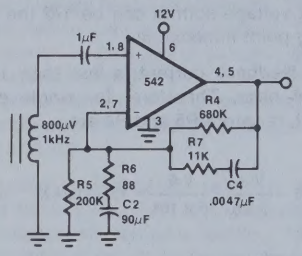
Figure 8-48

NAB Tape Preamplifier

Design of a preamplifier begins by determining the gain and output signal amplitudes in reference to the standard 800μV input signal level. For the following design example, we will use the 542 to achieve a 100mV output level at 1kHz following the 7-1/2 Ips NAB equalization curve. The graph of Figure 8-42 has been calibrated both in absolute gain for this example and relative gain for general use.

From the given parameters, the closed loop gain becomes 32dB at the highest frequency of interest. The NAB response is achieved by adding frequency selective ac feedback as depicted by Figure 8-49. Resistors R4 and R5 select the dc gain as defined by Equations 8-19 and 8-20. Placing a value of 200K upon R5, Equation 8-20 yields a value of 680K ohms.

NAB RESPONSE AMPLIFIER



All resistor values are in ohms

Figure 8-49

The lower corner frequency is determined next by the reactance of C4 and R4 such that:

$$f_1 = \frac{.159}{C4\ R4} \qquad (8\text{-}26)$$

Solving for C4 yields a value of .0047μfd.

The upper corner frequency, f_2, is similarly fixed by the reactance of C4 and R7.

$$f_2 = \frac{.159}{C4\ R7} \qquad (8\text{-}27)$$

Then solving Equation 8-27 for R7 defines a value of 11k ohms.

Midband gain is now fixed by the relationship.

$$A = \frac{R6 + R7}{R6} \qquad (8\text{-}28)$$

Solving for the 1kHz gain of 42dB using 11k for R7 yields a value of 88 ohms for R6. The final calculation of the low frequency cut off of the preamp determines the size of C2.

$$C2 = \frac{.159}{f_{CUTOFF}\ R6} \qquad (8\text{-}29)$$

Typical Applications

In addition to the previous detailed design examples, the following general amplifier configurations (see Figures 8-50 through 8-59) are presented. The choise of design and the device used is a function of the desired complicity and overall performance.

FLAT RESPONSE TAPE AMPLIFIER

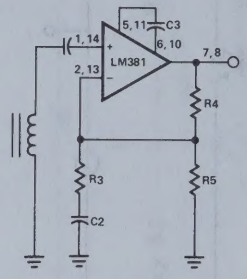


Figure 8-50

TWO-POLE FAST TURN-ON NAB TYPE PREAMP

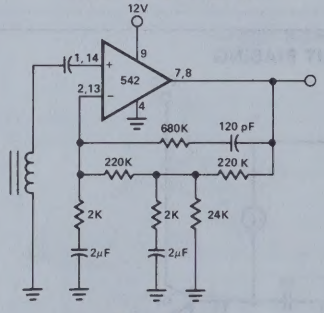
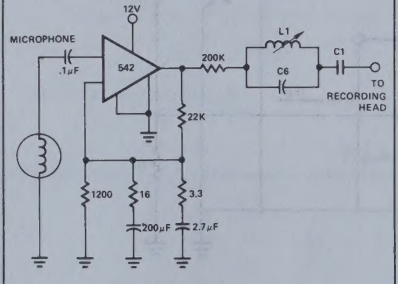


Figure 8-51

TYPICAL NAB RECORD PREAMPLIFIER



All resistor values are in ohms

Figure 8-52

TYPICAL TAPE PLAYBACK AMPLIFIER

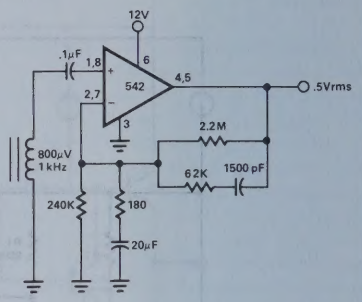
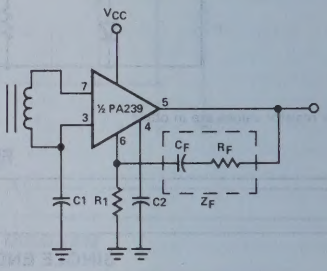


Figure 8-53

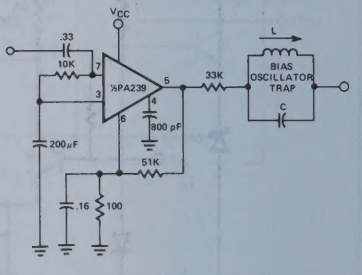
TAPE PREAMPLIFIER



	C2	CF	RF	R1
7-1/2 IPS	750pF	.033	1.5K	22Ω
3-3/4 IPS	750pF	.047	2.4K	33Ω

Figure 8-54

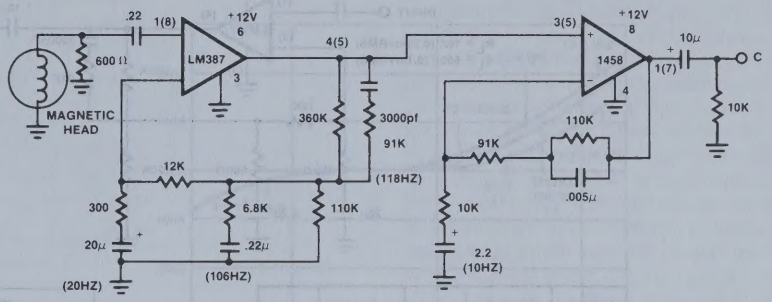
TYPICAL NAB RECORD PREAMPLIFIER



All resistor values are in ohms

Figure 8-55

CASSETTE PREAMPLIFIER SINGLE CHANNEL



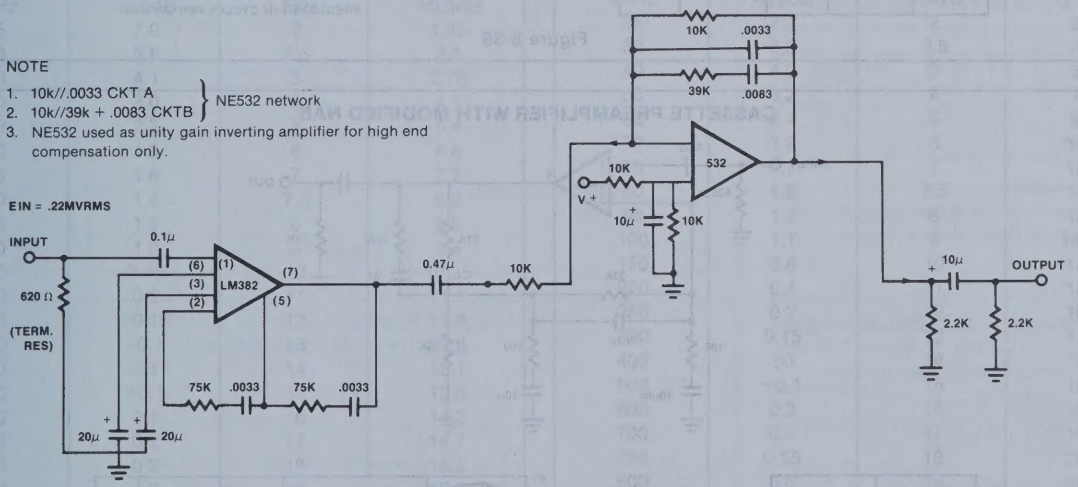
*600Ω resistor used as a terminator when using a voltage generator instead of the magnetic head.

Figure 8-56

CASSETTE PREAMPLIFIER USING LM382 and NE532

NOTE

1. 10k//.0033 CKT A
2. 10k//39k + .0083 CKTB } NE532 network
3. NE532 used as unity gain inverting amplifier for high end compensation only.



FREQ	GAIN(dB) CKT A	φ (deg) CKT A	GAIN(dB) CKT B	φ (deg) CKT B
20Hz	+68	-15	+68	
40Hz	+76.1	-76	+76	-77
80Hz	+79.4	-135	+79.3	-134
100Hz	+79.8	-147	+79.7	-148
200Hz	+79.7	-187	+79.5	+177
400Hz	+77.6	+157	+76.9	+155
800Hz	+74.6	+144	+73.3	+149
1kHz	+73.9	+144	+72.4	+150
2kHz	+71.8	+134	+70.6	+152
4kHz	+69.2	+110	+69.4	+145
8kHz	+63.9	+76	+67.4	+132
10kHz	+61.5	+65	+66.5	+126
20kHz	+54	-4.0	+62.2	+107

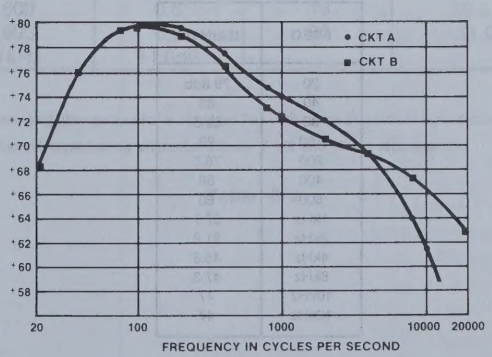
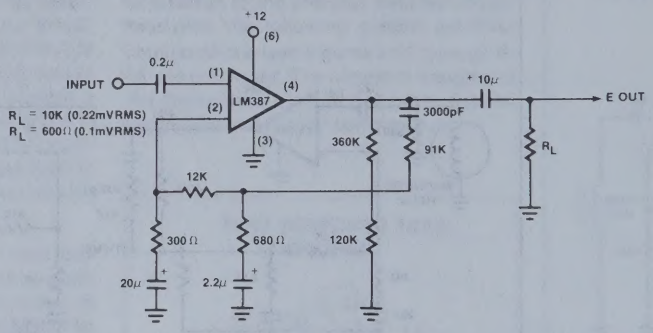


Figure 8-57

CASSETTE PREAMP USING LM387



FREQ	GAIN DB RL = 10K	φ deg	GAIN dB RL = 600	φ deg
20	69		64	
40	76.3		72.4	+115
80	80.4		77.8	+46.3
100	81		78.4	+33
200	80.2		77.8	-0.3
400	77.2		74.9	-18
800	74.8		72.4	-19.8
1kHz	74.2		72.1	-19.3
2kHz	73.3		71.1	-20.4
4kHz	72.3		70	-29.4
8kHz	70.1		68	-44.6
10kHz	69.1		67	-51.1
20kHz	65		62.4	-67.7

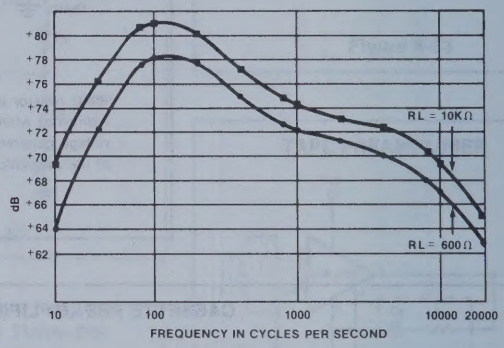
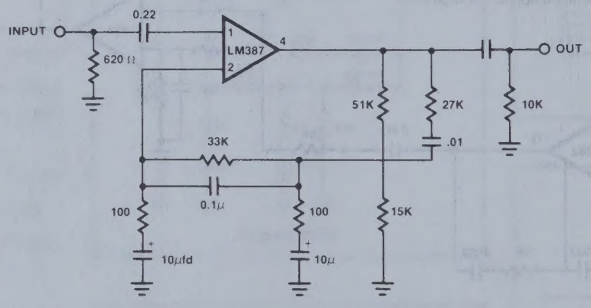


Figure 8-58

CASSETTE PREAMPLIFIER WITH MODIFIED NAB



FREQ	GAIN dB
20	79.8db
40	83
80	82.5
100	82
200	76.5
400	68
800	60
1kHz	57.7
2kHz	51.8
4kHz	48.8
8kHz	47.3
10kHz	47
12kHz	47

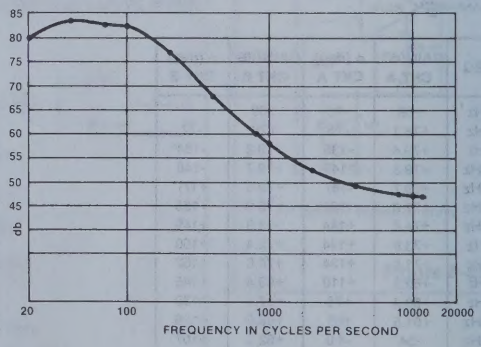


Figure 8-59

CONSTANT FLUX RESPONSE

Equalization criteria discussed earlier has made reference to RIAA Equalization for plastic discs (records) and for NAB Equalization for magnetic tapes. The NAB characterization should be carried further to discuss the Constant Flux Response.

The earlier discussion encompassed the voltage gain (in dB) vs frequency response of NAB amplifiers. In this section we will deal with the Constant Flux Response.

The Constant Flux Response accounts for the frequency characteristics of the record/playback heads of the tape (or cassette) machine employed and the effects of tape speed on Standard NAB Constant Flux Response.

Figure 8-60 indicates the circuitry for using two (2) IC's for a NAB response amplifier. Specific care should be taken to terminate the input *only* when using a voltmeter. When using the magnetic head, the terminating resistor should be removed.

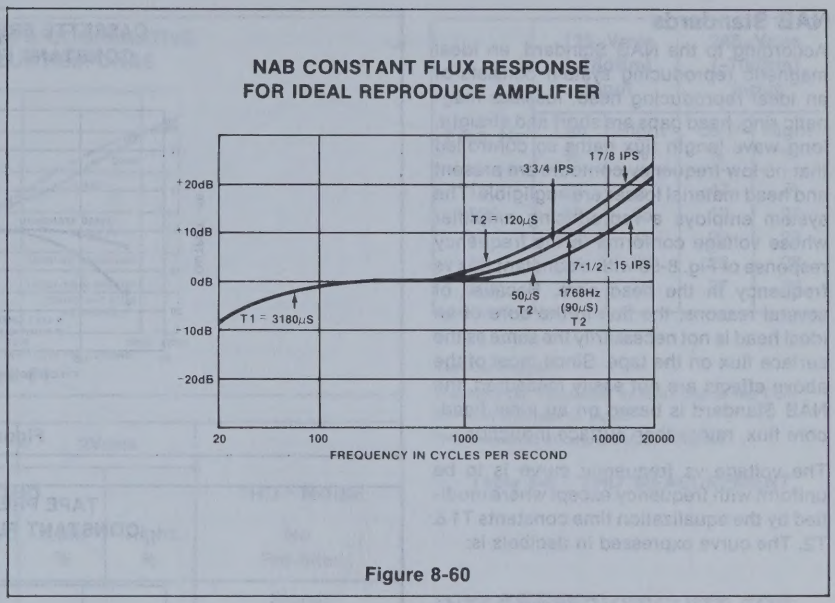


Figure 8-60

Frequency	Response	Frequency	Response
20Hz	-8.6dB	1.5kHz	+0.9dB
25	7.0	2	1.45
30	5.8	2.5	2.1
40	4.1	3	2.75
50	3.0	4	4.1
60	2.3	5	5.4
70	1.8	6	6.6
75	1.6	7	7.7
80	1.4	7.5	8.2
90	1.2	8	8.6
100	1.0	9	9.5
150	0.45	10	10.35
200	0.2	11	11.1
250	0.1	12	11.8
300	-0.1	13	12.5
400	±0	14	13.1
500	+0.1	15	13.6
600	0.1	16	14.2
700	0.2	17	14.7
750	0.2	18	15.2
800	0.2	19	15.6
900	0.3	20	+16.1
1kHz	+0.4dB		

NOTES
Reproducer amplifier output for a constant flux in the core of an ideal reproducing head.
NAB Standard reproducing characteristics for 1 7/8 and 3 3/4 ips tape speeds.

Table 8-2

Frequency	Response	Frequency	Response
20Hz	-8.8dB	1.5kHz	+2.2dB
25	7.2	2	3.4
30	5.9	2.5	4.6
40	4.2	3	5.7
50	3.2	4	7.7
60	2.4	5	9.4
70	1.9	6	10.8
75	1.7	7	12.1
80	1.6	7.5	12.6
90	1.3	8	13.2
100	1.1	9	14.15
150	0.6	10	15.0
200	0.4	11	15.8
250	0.2	12	16.6
300	0.15	13	17.2
400	±0	14	17.9
500	+0.1	15	18.5
600	0.3	16	19.0
700	0.5	17	19.6
750	0.55	18	20.0
800	0.6	19	20.5
900	0.8	20	+21.0
1kHz	+1.0dB		

NOTES
Reproducer amplifier output for a constant flux in the core of an ideal reproducing head.
NAB Standard reproducing characteristic for 7 1/2 and 15-ips tape speeds.

Table 8-3

NAB Standards

According to the NAB Standard, an ideal magnetic reproducing system consists of an ideal reproducing head, lossless magnetic ring, head gaps are short and straight, long wave length flux paths so controlled that no low frequency contours are present and head material losses are negligible. The system employs a reproducing amplifier whose voltage conforms to the frequency response of Fig. 8-59 with a constant flux vs frequency in the head core. Because of several reasons, the flux in the core of an ideal head is not necessarily the same as the surface flux on the tape. Since most of the above effects are not easily measured, the NAB Standard is based on an ideal head-core flux, rather than surface induction.

The voltage vs frequency curve is to be uniform with frequency except where modified by the equalization time constants T1 & T2. The curve expressed in decibels is:

$$N_{dB} = 20 \log 10\ WT1^{*} \sqrt{\frac{1 + (WT2)^2}{1 + (WT1)^2}} \qquad (8\text{-}30)$$

where $W = 2\pi f$, with f in Hz.

T1 & T2 are time constants given below:

Tape Speed	T1	T2
15 ips**	3180μsec	50 - μsec
7.5 ips	3180μsec	50 - μsec
3.75 ips	3180μsec	90 - μsec
1.875 ips	3180μsec	90 - μsec

Head Gap Losses:

The approximate head-gap losses vs frequency may be calculated using the expression:

$$\text{Gap loss} = -20 \log 10 \frac{\text{Sin } (180^{\circ}\ d/\lambda)}{\pi d/\lambda} \qquad (8\text{-}31)$$

where,

d = the null wavelength,
λ = the wavelength of the frequency at which the gap is calculated.

Null wavelength is determined by finding the recorded wavelength at which the reproducing-head output voltage reaches a distinct minimum of at least 20dB below maximum output. This measurement may be made using speeds of one-half and one-quarter the normal speed, using a tuned-voltmeter with no greater than one-third octave bandwidth. To reach a 20-dB null, the head gap edges must be sharp, straight, and parallel.

NOTES

*WT is:
ω = Omega
τ = Tau
** ips = inches per second

CASSETTE PREAMP LM387-1458
CONSTANT FLUX RESPONSE

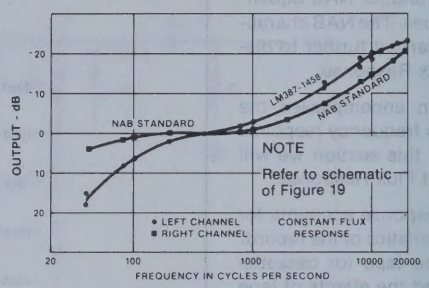
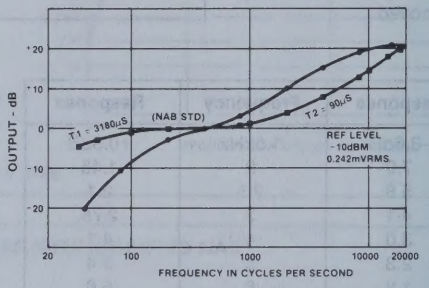


Figure 8-61

TAPE PREAMP LM387
CONSTANT FLUX RESPONSE

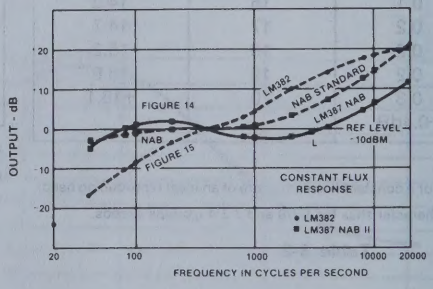


NOTE

Refer to schematic of Figure 13

Figure 8-62

CASSETTE PREAMP LM382 & LM387 (NAB)
CONSTANT FLUX RESPONSE



NOTE

Refer to schematic of Figure 14 & 15

Figure 8-63

CASSETTE PREAMPS COMPARATIVE CONSTANT FLUX RESPONSE

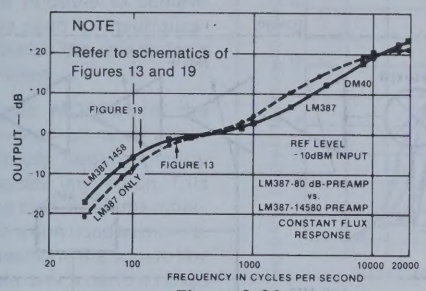


Figure 8-64

FILTER BANDWIDTH			1Vrms		2Vrms		THD + NOISE
			THD				
$f_{(Hz)}$	$f_{L\,(Hz)}$	$f_{H\,(Hz)}$	Left %	Right %	Left %	Right %	No Pre-filter
							Signal 1Vrms
500	400	2500	.28	.28	.29	.27	2.5%
1k	900	4k	.28	.26	.32	.28	2.5%
10k	9900	40k	1.3	1.4	.68	.7	2.4%

Test Conditions: V_{CC} = 12V

ST1700A THD Analyser oscillator signal coupled to reproduce head through constant flux loop. Output signal fed back to ST1700 through Kronhite 3203 filter.

Table 8-4 CASSETTE PREAMP 'THD' MEASUREMENTS WITH REPRO HEAD

Freq (Hz)	Output		
	Left dBM	Right dBM	
20		-35	
40	-27.5	-26	
80	-18	-18	
100	-16	-16	
200	-12	-12	
400	-10	-10.5	
800	-8	-8	
1k	-7	-7	"0" dB reference level @ -10dBm
2k	-2.5	-2.2	
4k	+2	+3.2	
8k	+8	+9	
10k	+9.5	+10.8	
12k	+11.2	+11.8	
14k	+12	+12.3	
16k	+12.6	+12.5	
20k	+13	+13	

Test Conditions:

HP651A Test Oscillator 600ohm output coupled through constant flux loop to reproduce head. Output recorded from preamp across 10k load ac. V.M.

Table 8-5 CASSETTE PREAMP CONSTANT FLUX RESPONSE

Freq. Hz	125μVrms (-76dBm) input		245μVrms (-70dBm) input	
	Left %	Right %	Left %	Right %
100	.37	.5	.47	.7
500	.35	.35	.19	.23
1k	.42	.43	.22	.23
5k	.54	.54	.26	.28
10k	.73	.75	.37	.38

Test Conditions:

Preamp input terminated in 600Ω. Signal fed from ST1700A Analyser to input.

THD measured at output across 10kΩ load.

Table 8-6 'THD' MEASUREMENT

INTEGRATED CIRCUITS FOR CITIZENS BAND TRANSCEIVERS

Introduction

Recent advancements in integrated circuits have made it possible to greatly simplify the design of citizens band transceivers. A complete multi-channel radio can be built using integrated circuits for all the required functions with the exception of the RF power output stage. A simplified block diagram of such a transceiver is shown in Figure 8-65.

This applications report will further describe a typical version of such a transceiver using several newly developed integrated circuits.

The growing popularity of CB radio is making it necessary to improve the performance characteristics of the CB receiver. The crowded channel and noise problems inherent in this type of communication system demand high performance system design. A dual conversion receiver is desirable to aid in meeting this goal.

RF AMPLIFIER/1ST MIXER

The RF amplifier and 1st mixer used in this radio are implemented using an SD6000. The SD6000 is a dual enhancement mode MOSFET integrated RF amplifier/mixer intended for use up to 150MHz. The advantages of using MOSFETs in receiver "front end" designs have been realized for several years by manufacturers of FM and television tuners. Using a linear device such as a MOSFET, it is possible to achieve improvements in cross-modulation, intermodulation distortion and in general a much wider dynamic range than possible using conventional bipolar transistors.

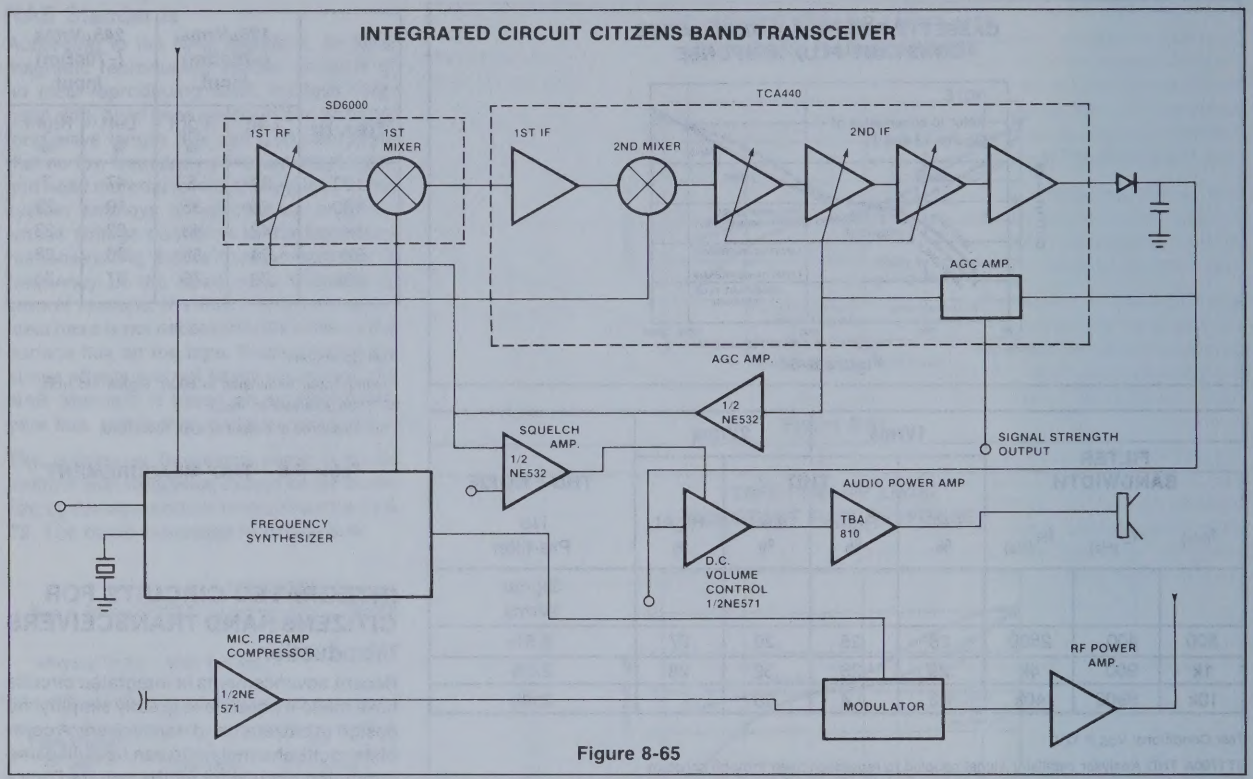


Figure 8-65

The SD6000 is ideally suited for this application for several reasons. The RF section is essentially a low noise, high gain dual gate MOSFET. The relatively high input impedance of this device makes it convenient to use high Q tuned circuits which reduce the possibility of out of band spurious responses. The AGC range of the RF amplifier is greater than 50dB at 27MHz and because of the low parasitic capacitances associated with this device there is no skewing of the center frequency of the tuned circuits as a function of AGC voltages. The RF amplifier input circuit can be roughly approximated as shown below in Figure 8-66.

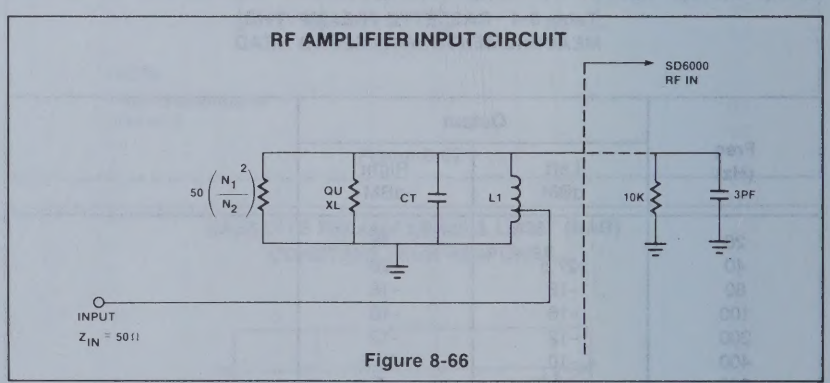


Figure 8-66

L1 consists of 24 turns of #32 wire tapped 4 turns from the ground side on a Micro-Metals T44-10 core. This gives an inductance of 1.6μh ($X_C = 270\Omega$ @ 27MHz) and an unloaded Q of 150.

The input circuit can be further simplified as shown in Figure 8-67.

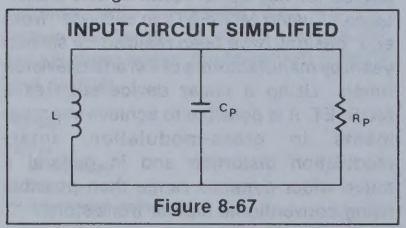


Figure 8-67

C_P is made up of the D-MOS input, and a fixed parallel capacitor. The required C_P is given by

$$C_P = \frac{1}{w2L} \qquad (8\text{-}32)$$

C_P at 27MHz is therefore equal to 22pf. A portion of C_P is made tunable in this design. This would not be necessary in a design using a slug tuned inductor. It should be noted that the position of the tap is such that the reflected antenna impedance does not match the RF amplifier input impedance. This was done intentionally to improve the large signal (2Vrms) handling capability of this receiver. The MOS front end has sufficient gain to compensate for this loss.

The bandwidth of the RF input circuit can be found knowing the total parallel resistance (R_P) and parallel capacitance

$$BW_{-3dB} = \frac{1}{2\pi RC} \qquad (8\text{-}33)$$

At 27MHz the RF input bandwidth is approximately 4MHz. In a more optimum design this could be made narrower by tapping the input coil closer to ground.

The design of the RF output circuit is very similar to that of the input. The only difference is a different value of fixed capacitance to take into account the RF amplifier output and mixer input capacitance.

Dual gate Signetics D-MOS transistors are exceptionally stable RF devices because of their low feedback capacitance (typically .02pf). This makes it possible to achieve high gain without the need for neutralization. Low feedback is also the reason for a wide dynamic AGC range.

The second dual gate MOSFET is the SD6000 which is designed for mixer applications. It is a relatively large geometry device with a wide square law region. This design overcomes the bias problems inherent in most MOSFETs when used as mixers. In other MOSFETs biasing in the square law region is only possible over a narrow range of drain current. In the SD6000 mixer the conversion gain is essentially constant from 5 to 10mA drain current thus simplifying the bias circuit design.

The 1st oscillator is injected into gate 2 and the RF signal into gate 1. Injecting the oscillator into gate 2 provides the highest isolation between the oscillator and RF input. This isolation is important to prevent radiation of the oscillator signal through the receiver antenna.

The mixer is biased to operate in the most linear portion of the forward transconductance curves. Figures 8-68 and 8-69 show the transconductance curves for the SD6000 are linear in a relatively wide operating region. Non-linearities in these curves indicate that third order (and higher) terms would be present if the device was biased in these regions. These higher order terms contribute only to undesired responses. As the transconductance curves become linear, the higher order terms disappear and conversion gain increases. Figure 8-68 shows that the gate 1 transconductance curves is almost a straight line for gate 2 bias voltage between 2.0 and 6.0 volts. Figure 8-69 shows a linear region for gate 2 transconductance with gate 1 bias from 2.5 to 3.5 volts.

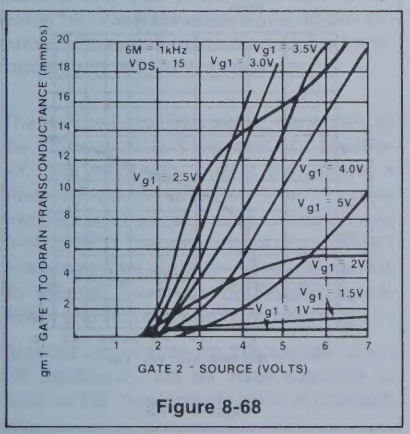


Figure 8-68

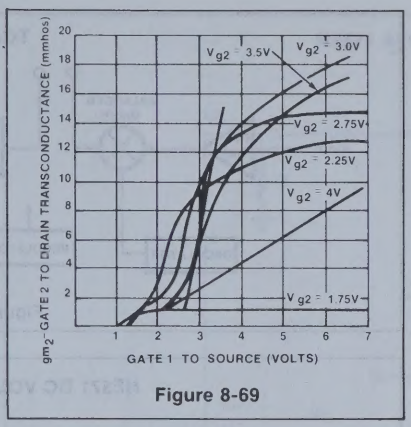


Figure 8-69

By definition the transconductance, gm is the partial derivative of drain current, i_d, with respect to the input voltage e_s. The total drain current of the mixer can be expressed by

$$i_d = gm1\ V_{g1} + gm2\ V_{g2} \qquad (8\text{-}34)$$

where gm1 = transconductance gate 1 to drain.
gm2 = tranconductance gate 2 to drain.

From Figure 8-68 the gate 1 tranconductance, gm1 can be expressed as:

$$gm1 = -17.6 + 8.2\ (V_{g2} + V_{g2})\ \text{(mmhos)}$$

for V_{g2} = 2V to 6V

From Figure 8-68 we get the following expression for gm2

$$gm2 = -23.7 + 10.2\ (V_{g1} + V_{g1})\ \text{(mmhos)}$$

for V_{g1} = 2.5V to 3.5V

If the dc bias points are chosen, for example V_{g1} = 3.5 and V_{g2} = 3.5, the following expressions are derived from gm1 and gm2 using the previous equations

$$gm1 = 11.1 + 8.2\ V_{g2}\ \text{(mmhos)}$$

$$gm2 = 8.9 + 10.2\ V_{g1}\ \text{(mmhos)}$$

Substituting these equations into the expression for the total drain current, i_d, we get

$$i_d = 11.1\ V_{g1} + 8.9\ V_{g2} + 18.4\ V_{g1}\ V_{g2}$$

The last term in this equation is the one that will contain the IF frequency we desire. If we let V_{g1} and V_{g2} equal a sinusoidal voltage, V_{g1} is the input signal voltage and V_{g2} is the local oscillator, we obtain

$$V_{g1} = E_s \sin \omega_{LO} + \omega_s t$$

$$V_{g2} = E_{LO} \sin \omega_{LO} t$$

Substituting V_{g1} and V_{g2} into the equation for i_d gives

$$i_d = 18.4\ E_S\ E_{LO}\ 1/2 \cos (\omega_{LO} + \omega_S)t + 1/2 \cos (\omega_{LO} - \omega_S)t$$

The $(\omega_{LO} - \omega_S)$ term is the 10.7MHz IF we want. Dividing both sides of the equation by E_S we obtain

$$\frac{i_d}{E_s} = gm_c = 9.2\ E_{LO}\ \text{(peak)} \qquad (8\text{-}35)$$

$$= 13\ E_{LO}\ \text{(rms) mmhos}$$

This exercise shows that relatively high conversion gains can be achieved using the SD6000. It can be seen that the conversion transconductance will also be a function of the local oscillator level.

In actual practice, good performance can be achieved with both gates biased at the same dc voltage. The bias voltage is chosen to give a drain current of 5 to 10mA.

For bias stability, some form of dc feedback should be incorporated to reduce the drain current variations that would occur in production where variations in the device threshold voltages will be encountered. In the SD6000, the mixer and RF amplifier substrates and RF amplifier source are connected internally so precautions must be taken to assure that the RF amplifier source voltage is less than or equal to the mixer source voltage. In this design the RF amplifier source is grounded so it can never be positive with respect to the mixer source. Figure 8-69 shows a simplified bias circuit of the RF amplifier.

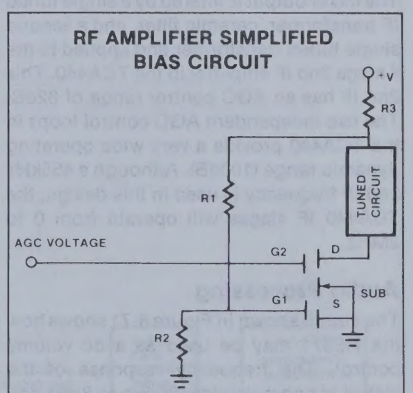


Figure 8-70

This bias circuit provides dc feedback without using a source resistor. R3 is made large enough so that there is a significant voltage drop across it with normal operating drain current (10-15mA). This voltage drop means a lower drain to source voltage (V_{DS}). A lower V_{DS} does not affect the RF amplifier gain since the transconductance is constant with V_{DS} from 5 to 20 volts. If variations in threshold voltage were to cause a higher drain current, the voltage drop across R3 would increase thereby decreasing the gate 1 voltage derived from R1 and R2. This decreased gate 1 voltage tends to decrease

the drain current and will result in a stable operating point.

The mixer is biased using the same technique with the addition of a bypassed source resistor to provide even greater stability.

The mixer output is coupled through a 10.7MHz IF transformer to a 10.7MHz crystal filter. The output of the filter is terminated with a 2.2k resistor in parallel with the TCA440 input (2K/5pf).

1st IF/2nd Mixer/2n IF

A block diagram of the TCA440 is shown in Figure 8-70.

This integrated circuit is intended for AM receivers up to 50MHz. It has several features making it well suited for citizens band receiver applications. The RF stage (in this case the 1st IF) is a differential amplifier with an AGC control range of approximately 38dB. Its output is internally coupled to a mulitplicative push-pull mixer (balanced). This mixer produces few harmonics and provides suppression of the RF and oscillator frequencies. The internal oscillator frequency is fixed at 10.245MHz by a parallel resonant crystal. This gives a mixer output frequency of 455kHz for the 2nd IF.

The mixer output is filtered by a single tuned IF transformer, ceramic filter, and a second single tuned transformer and applied to the 4 stage 2nd IF amplifier in the TCA440. This 2nd IF has an AGC control range of 62dB. The two independent AGC control loops in the TCA440 provide a very wide operating dynamic range (100dB). Although a 455kHz 2nd IF frequency is used in this design, the TCA440 IF stages will operate from 0 to 2MHz.

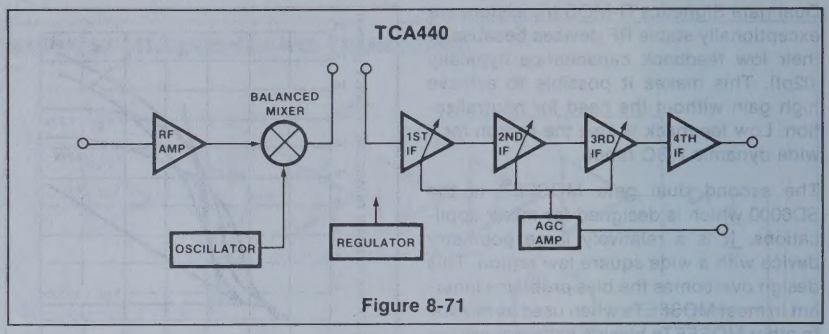


Figure 8-71

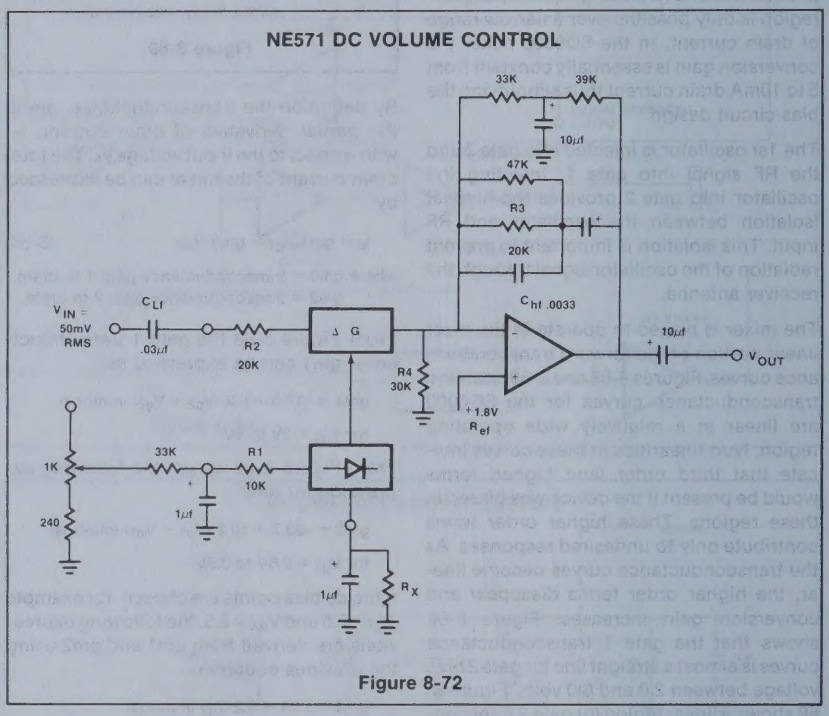


Figure 8-72

Audio Processing

The circuit shown in Figure 8-71 shows how the NE571 may be used as a dc volume control. The frequency response of the circuit is approximately 300Hz to 3kHz and the dynamic control range is greater than 60dB. Figure 8-72 shows the dc control voltage vs gain.

The output of the NE571 dc volume control drives a TBA810S audio power amplifier. The TBA 810 provides a 6 watt (@ 14.4V 4Ω) output with low harmonic and cross-over distortion. In addition, the circuit has a thermal limiting circuit which simplifies the heat sink design.

Audio Compressor

The purpose of the transmit audio compressor is to amplify the signal from the microphone to the level required to drive the modulator. It also provides an automatic level control (ALC) circuit. The ALC circuit has a transfer function which makes its output voltage constant with a wide range of input levels. It is generally desirable to have an audio compressor which provides an output level which drives the modulator to close to 100% modulation with very low input levels and does not exceed 100% with large inputs.

There are two major overmodulation problems that show up in many CB transceivers currently available. One is the audio compressor's ability to handle a wide dynamic range of microphone input levels. The current popularity of "power mics" makes it necessary for the compressor to limit the modulation index to less than 100% with very large inputs. The second overmodulation problem that may arise relates to the audio compressor's attach time. Active

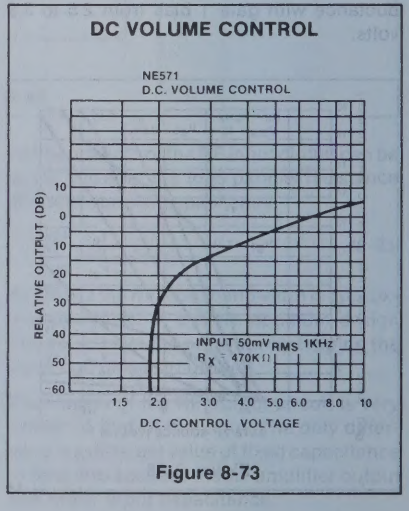


Figure 8-73

compressor circuits take a finite time to respond to a sudden change in input level.

The NE571 provides an economical solution to the above mentioned problems. Figure 8-81 shows how this ALC circuit may be implemented.

The gain of this circuit is

$$K = \frac{R1\ R2\ I_B}{2R3\ V_{IN}\ (AVG)} \text{ where } IB = 140\mu A \quad (8\text{-}36)$$

$$\text{and } \frac{V_{IN}}{V_{IN}\ (AVG)} = \frac{\pi}{2\sqrt{2}}$$

for sinc waves

R_x is included to limit the maximum gain of the compressor. This is to prevent high modulation levels at very low input levels (such as background noise). The maximum gain

$$K_{max} = \frac{\frac{R1 + R_x}{1.8} \times R2 \times I_B}{2R3} \quad (8\text{-}37)$$

The output voltage may be set to the desired level

$$V_{out} = \frac{R1\ R2\ I_B}{2R3} \cdot \frac{V_{IN}}{V_{IN}\ (AVG)} \quad (8\text{-}38)$$

The other important design equations for this circuit are:

I ALC time constant ($\tau = R1 \times C_{Rect}$) (8-39)

II Distortion $= \frac{.1\mu f}{C_{Rect}} \times \frac{1KHz}{freq} \times 2\%$

III $V_{out}\ (dc) = \left[1 + \frac{R_{dc1} + R_{dc2}}{R4}\right] 1.8V$ (8-40)

Transmit RF

Development work is currently taking place to try and solve some of the typical problems encountered in the RF section of CB transceivers. The major emphasis is towards reducing the cost of the output circuitry (elimination of the modulation transformer) and reduce spurious outputs.

The transmit oscillator signal, generated by the PLL, will drive a low level FET modulator. The modulator output then drives a linear RF power amplifier. The RF power amplifier will be implemented using a power D-MOS FET. The advantages of a MOSFET power amplifier are high transconductance, no thermal run-away, no second breakdown, and reduction in harmonic output.

Detailed information on this section of the CB transceiver will be made available as soon as the development work is completed.

NE571 ALC CIRCUIT

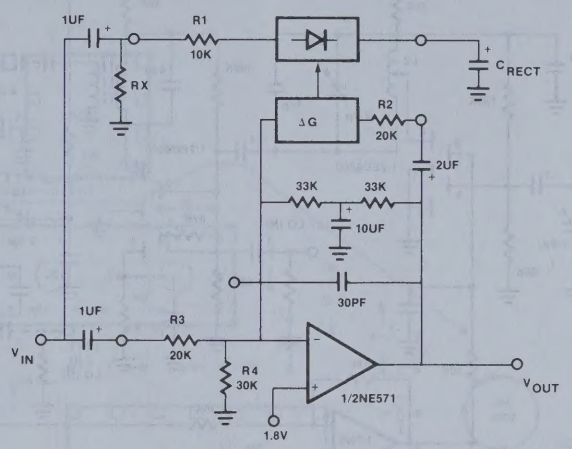


Figure 8-74

CITIZENS' BAND RECEIVER TCA440/SD6000

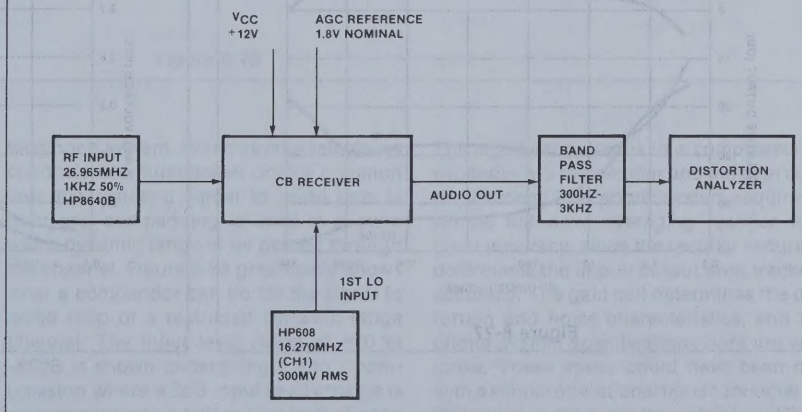


Figure 8-75

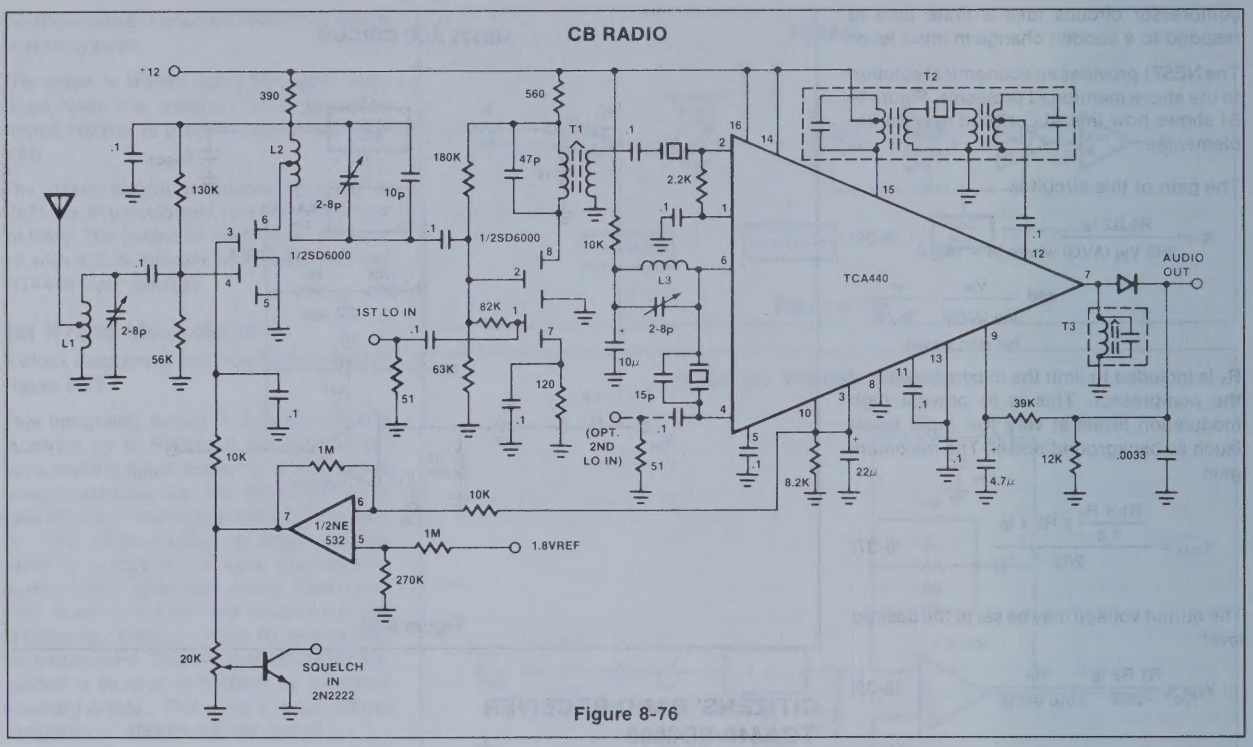


Figure 8-76

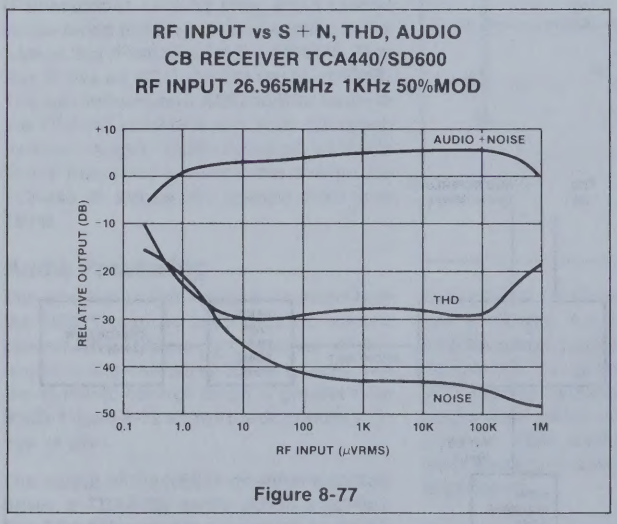


Figure 8-77

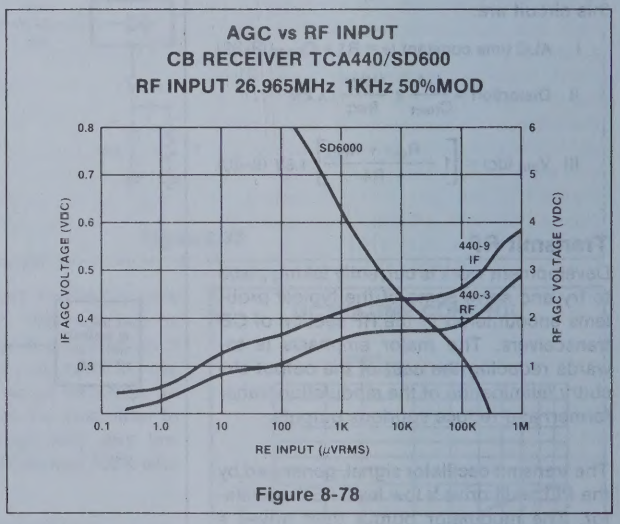
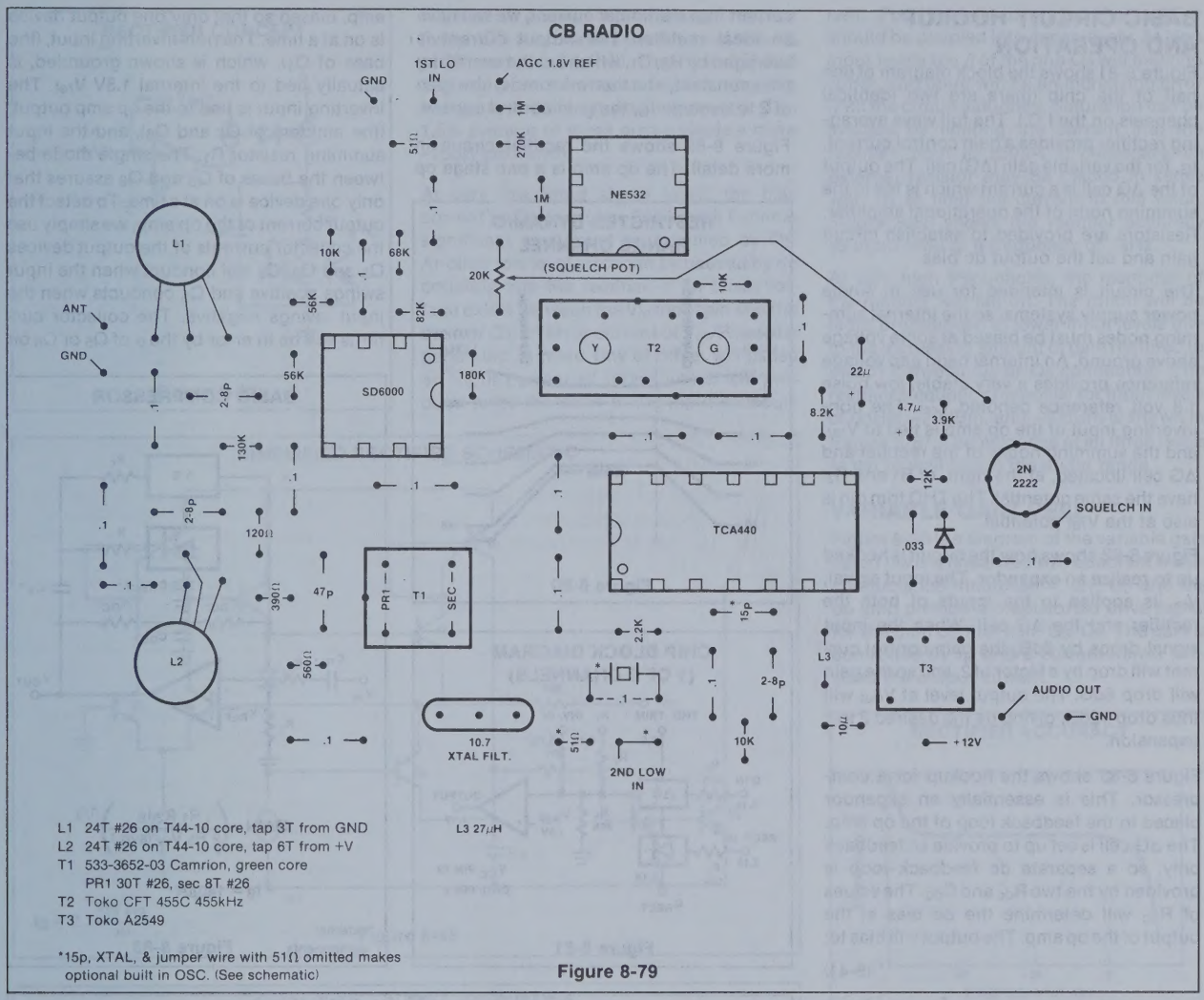


Figure 8-78



L1 24T #26 on T44-10 core, tap 3T from GND
L2 24T #26 on T44-10 core, tap 6T from +V
T1 533-3652-03 Camrion, green core
PR1 30T #26, sec 8T #26
T2 Toko CFT 455C 455kHz
T3 Toko A2549

*15p, XTAL, & jumper wire with 51Ω omitted makes optional built in OSC. (See schematic)

Figure 8-79

INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high performance is required, one has to resort to complex discrete circuitry with many expensive, well matched components. This paper describes a new integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<.1%), high signal to noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was specifically designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal to noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 8-89 graphically shows what a compandor can do for the signal to noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2 to 1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expandor are the rectifier and the gain control element. The phone system requires a simple full wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. It is hoped that these features will make the circuit as widely used in audio systems as it will be in telecommunications systems.

BASIC CIRCUIT HOOKUP AND OPERATION

Figure 8-81 shows the block diagram of one half of the chip (there are two identical channels on the I.C.). The full wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output dc bias.

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8 volt reference denoted V_{ref}. The non-inverting input of the op amp is tied to V_{ref}, and the summing nodes of the rectifier and ΔG cell (located, at the right, of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{ref} potential.

Figure 8-82 shows how the circuit is hooked up to realize an expandor. The input signal, V_{in}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{out} will thus drop 12dB, giving us the desired 2 to 1 expansion.

Figure 8-83 shows the hookup for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is set up to provide ac feedback only, so a separate dc feedback loop is provided by the two R_{dc} and C_{dc}. The values of R_{dc} will determine the dc bias at the output of the op amp. The output will bias to:

(8-41)

$$V_{out\ dc} = 1 + \frac{R_{dc1}+R_{dc2}}{R_4} V_{ref} = \left(1 + \frac{R_{dc\ tot}}{30K}\right) 1.8V$$

The output of the expandor will bias up to:

(8-42)

$$V_{out\ dc} = 1 + \frac{R_3}{R_4} V_{ref} = \left(1 + \frac{20K}{30K}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the dc bias to any desired value.

CIRCUIT DETAILS-RECTIFIER

Figure 8-83 shows the concept behind the full wave averaging rectifier. The input current to the summing node of the op amp, V_{in}/R_1, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, Cr, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.

Figure 8-85 shows the rectifier circuit in more detail. The op amp is a one stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{ref}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on

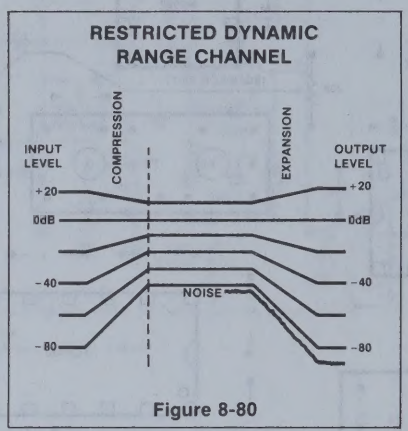


Figure 8-80

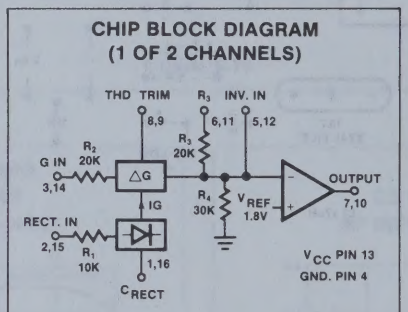


Figure 8-81

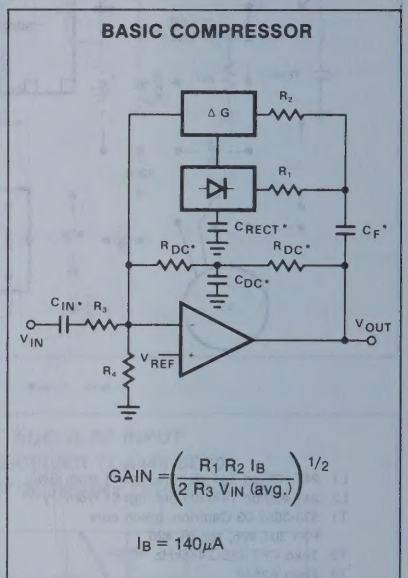


Figure 8-83

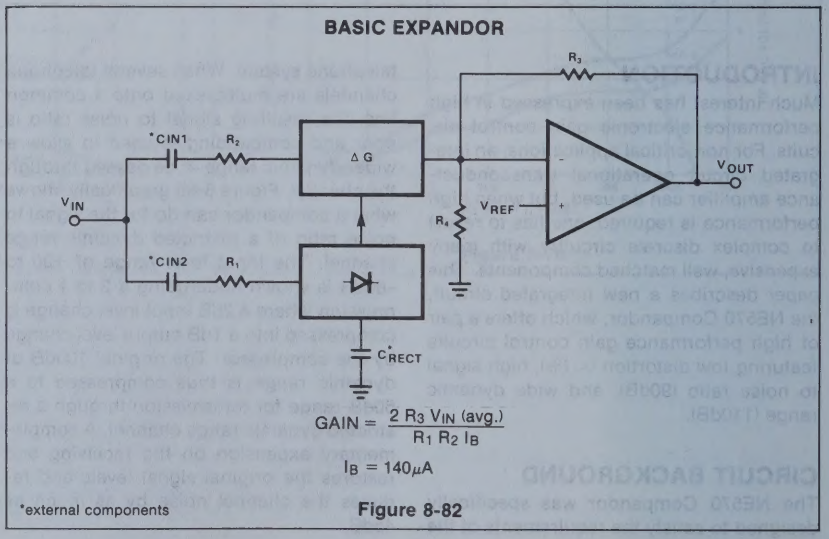


Figure 8-82

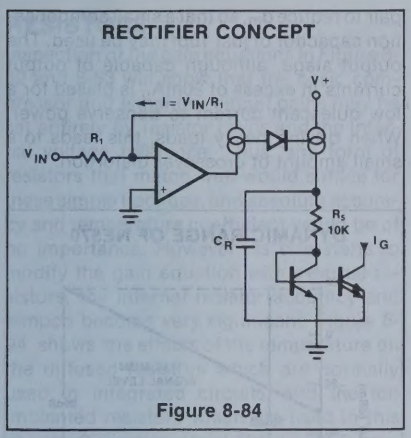


Figure 8-84

negative or positive signal swings, respectively. IC's such as this have typical npn β's of 200 and pnp β's of 40. The α's of .995 and .975 will produce errors of .5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere -13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by dc coupling into the rectifier. If an offset voltage exists between the V_{in} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mv of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the pnp Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 8-86 shows the rectifier accuracy vs input level at a frequency of 1kHz.

At very high frequencies, the response of the rectifier will fall off. The rolloff will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8-87. The response at all three levels is flat to well above the audio range.

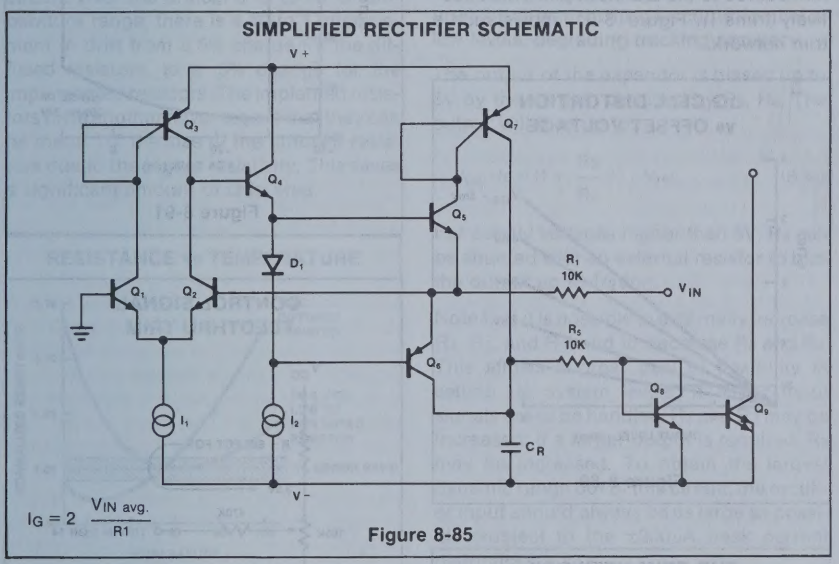


Figure 8-85

VARIABLE GAIN CELL

Figure 8-88 is a diagram of the variable gain cell. This is a linearized two quadrant transconductance multiplier[1,2]. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3, Q_4. The gain is controlled by I_G and a current mirror provides the output current.

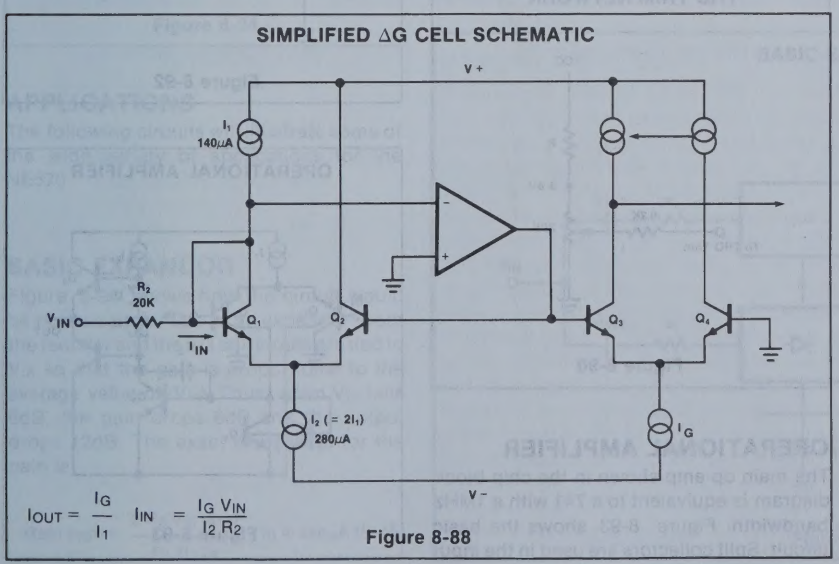


Figure 8-88

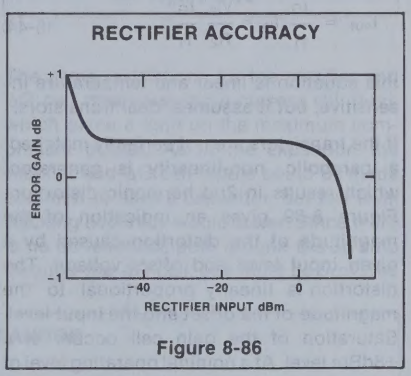


Figure 8-86

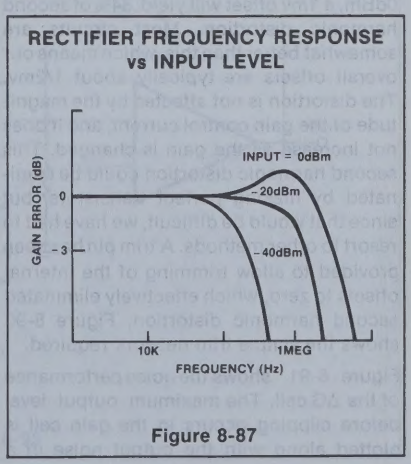


Figure 8-87

The op amp maintains the base and collector of Q_1 at ground potential (V_{ref}) by controlling the base of Q_2. The input current I_{in} ($= V_{in}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{in}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is $I_2-(I_1+I_{in}) = I_1-I_{in} = I_{C2}$. The op amp has thus forced a linear current swing between Q_1 and Q_2, by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair Q_1, Q_2 under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical, regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1+I_{in}}{I_1-I_{in}} \qquad (8\text{-}43)$$

plus the relationships $I_G = I_{C3} = I_{C4}$ and $I_{out} = I_{C4} - I_{C3}$ will yield the multiplier transfer function,

$$I_{out} = \frac{I_G}{I_1} I_{in} = \frac{V_{in}}{R_2} \frac{I_G}{I_1} \qquad (8\text{-}44)$$

this equation is linear and temperature insensitive, but it assumes ideal transistors.

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in 2nd harmonic distortion. Figure 8-89 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mv offset will yield .34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about 1/2mv. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 8-90 shows the simple trim network required.

Figure 8-91 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

Control signal feed-through is generated in the gain cell by imperfect device matching and mismatches in the current sources I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feed-through, but in general, the null for minimum feed-through will be different than the null in distortion. The control signal feed-through can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 8-91 shows such a trim network.

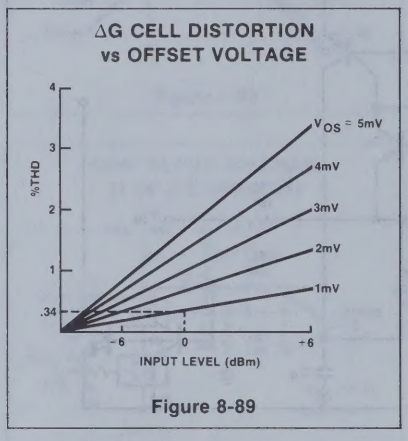


Figure 8-89

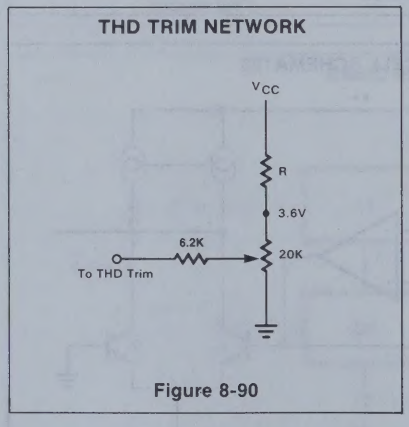


Figure 8-90

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 8-93 shows the basic circuit. Split collectors are used in the input pair to reduce g_m, so that a small compensation capacitor of just 10pf may be used. The output stage, although capable of output currents in excess of 20mA., is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

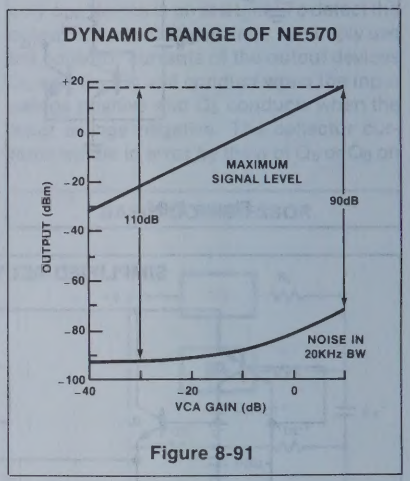


Figure 8-91

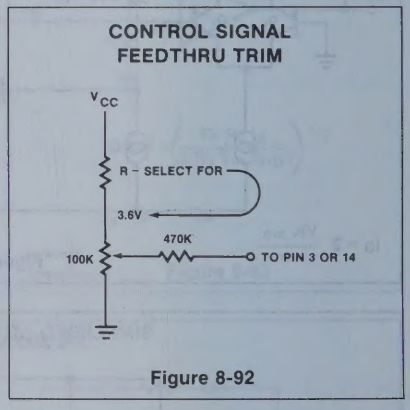


Figure 8-92

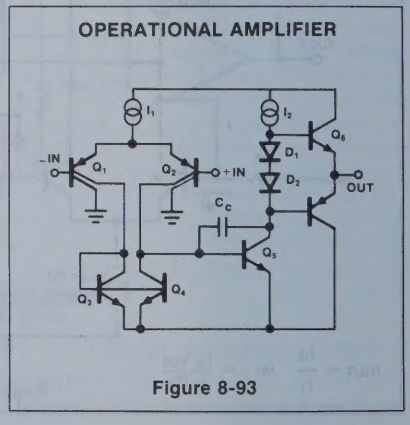


Figure 8-93

RESISTORS

Inspection of the gain equations in Figure 8-82 and 8-83 will show that the basic compressor and expandor circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hookups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 8-94 shows the effects of the temperature on the diffused resistors which are normally used in integrated circuits, and the ion implanted resistors which are used in this circuit. Over the critical 0°C to 70°C temperature range, there is a 10 to 1 improvement in drift from a 5% charge for the diffused resistors, to a .5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made 1/7 the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

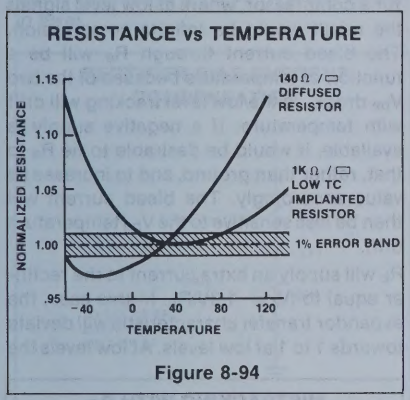


Figure 8-94

APPLICATIONS

The following circuits will illustrate some of the wide variety of applications for the NE570.

BASIC EXPANDOR

Figure 8-95 shows how the circuit would be hooked up for use as an expandor. Both the rectifier and the ΔG cell inputs are tied to V_{in} so that the gain is proportional to the average value of (V_{in}). Thus, when V_{in} falls 6dB, the gain drops 6dB and the output drops 12dB. The exact expression for the gain is

$$\text{Gain exp.} = \frac{2\,R_3\,V_{in\,(ave)}}{R_1\,R_2\,I_B} \quad ; \; I_B = 140\mu A \qquad (8\text{-}45)$$

The maximum input that can be handled by the circuit in Figure 8-104 is a peak of 3V. The rectifier input current can be as large as $I = 3V/R_1 = 3V/10K = 300\mu A$. The ΔG cell input current should be limited to $I = 2.8V/R_2 = 2.8V/20K = 140\mu A$. If it is necessary to handle larger input voltages than 0 ± 2.8V pk, external resistors should be placed in series with R_1 and R_2 to limit the input current to the above values.

Figure 8-95 shows a pair of input capacitors C_{in1} and C_{in2}. It is not necessary to use both capacitors if low level tracking accuracy is not important. If R_1 and R_2 are tied together and share a common capacitor, a small current will flow between the ΔG cell summing node and the rectifier summing node due to offset voltages. This current will produce an error in the gain control signal at low levels, degrading tracking accuracy.

The output of the expandor is biased up to 3V by the dc gain provided by R_3, R_4. The output will bias up to

$$V_{out\ dc} = \left(1 + \frac{R_3}{R_4}\right) V_{ref} \qquad (8\text{-}46)$$

For supply voltages higher than 6V, R_4 can be shunted with an external resistor to bias the output up to $^1/_2V_{CC}$.

Note that it is possible to externally increase R_1, R_2, and R_3, and to decrease R_3 and R_4. This allows a great deal of flexibility in setting up system levels. If larger input signals are to be handled, R_1 and R_2 may be increased; if a larger output is required, R_3 may be increased. To obtain the largest dynamic range out of this circuit, the rectifier input should always be as large as possible (subject to the ±300μA peak current restriction).

BASIC COMPRESSOR

Figure 8-96 shows how to use the NE570/571 as a compressor. It functions as an expandor in the feedback loop of an op amp. If the input rises 6dB, the output can rise only 3dB. The 3dB increase in output level produces a 3dB increase in the gain in the ΔG cell, yielding a 6dB increase in feedback current to the summing node. Exact expression for gain is

$$\text{Gain (comp.)} = \left[\frac{R_1\,R_2\,I_B}{2\,R_3\,V_{in\,(ave)}}\right]^{1/2} \qquad (8\text{-}47)$$

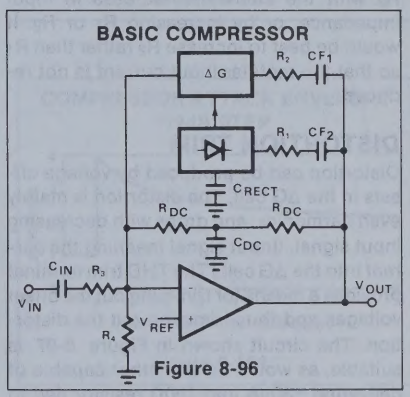


Figure 8-96

The same restrictions for the rectifier and ΔG cell maximum input current still hold, which place a limit on the maximum compressor output. As in the expandor, the rectifier and ΔG cell inputs could be made common to save a capacitor, but low level tracking accuracy would suffer. Since there is no dc feedback path around the op amp through the ΔG cell, one must be provided

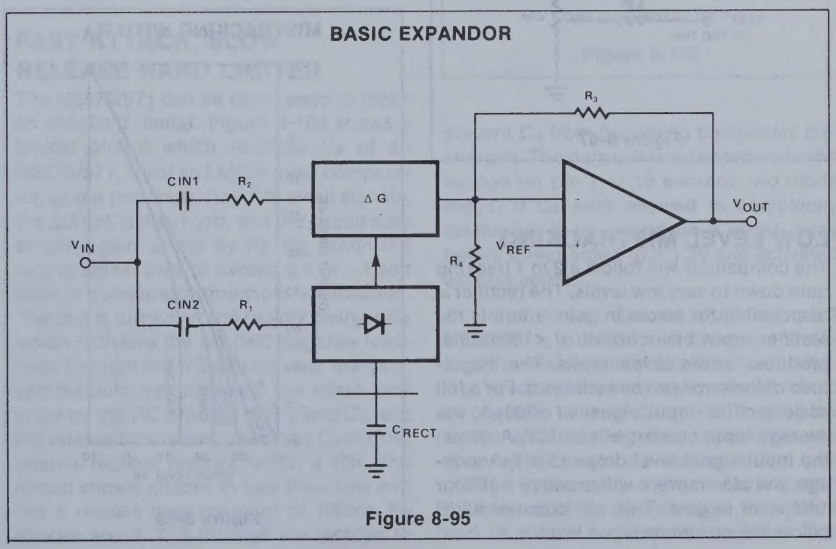


Figure 8-95

externally. The pair of resistors R_{dc} and the capacitor C_{dc} must be provided. The op amp output will bias up to

$$V_{out}\,dc = (1 + \frac{2\,R_{dc}}{R_4})\,V_{ref} \qquad (8\text{-}48)$$

For the largest dynamic range, the compressor output should be as large as possible so that the rectifier input is as large as possible (subject to the $\pm 300\mu A$ peak current restriction). If the input signal is small, a large output can be produced by reducing R_3 with the attendant decrease in input impedance, or by increasing R_1 or R_2. It would be best to increase R_2 rather than R_1 so that the rectifier input current is not reduced.

DISTORTION TRIM

Distortion can be produced by voltage offsets in the ΔG cell. The distortion is mainly even harmonics, and drops with decreasing input signal. (Input signal meaning the current into the ΔG cell.) The THD trim terminal provides a means for trimming out the offset voltages and thus trimming out the distortion. The circuit shown in Figure 8-97 is suitable, as would be any other capable of delivering $\pm 30\mu A$ into 100Ω resistor tied to 1.8V.

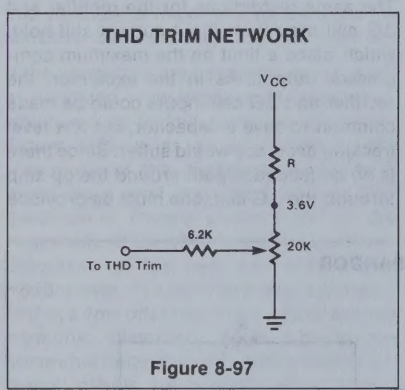


Figure 8-97

LOW LEVEL MISTRACKING

The compandor will follow a 2 to 1 tracking ratio down to very low levels. The rectifier is responsible for errors in gain, and it is the rectifier input bias current of <100na that produces errors at low levels. The magnitude of the error can be estimated. For a full scale rectifier input signal of $\pm 200\mu A$, the average input current will be $127\mu A$. When the input signal level drops to a $1\mu A$ average, the bias current will produce a 10% or 1dB error in gain. This will occur at 42dB below the maximum input level.

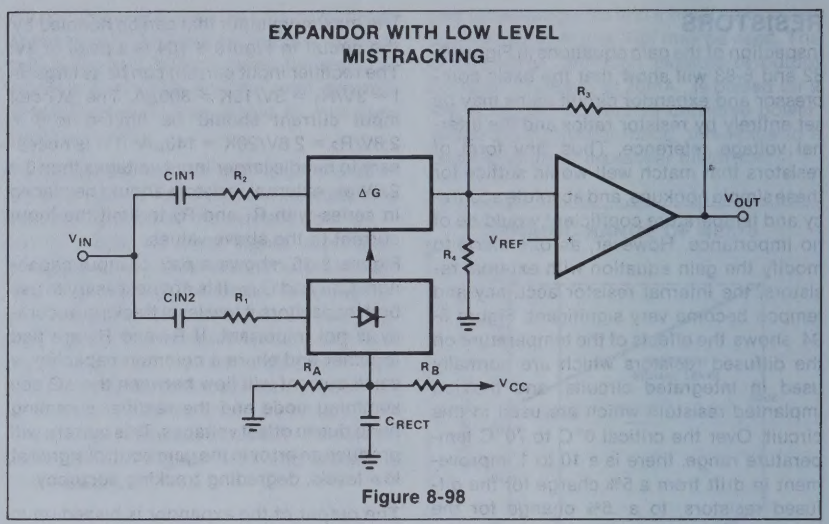


Figure 8-98

It is possible to deviate from the 2 to 1 transfer characteristic at low levels as shown in the circuit of Figure 8-98. Either R_a or R_b, (but not both), is required. The voltage on C_{rect} is $2xV_{be}$ plus V_{in} ave. For low level inputs V_{in} ave is negligible, so we can assume 1.3V as the bias on C_{rect}. If R_a is placed from C_{rect} to gnd we will bleed off a current $I = 1.3V/R_a$. If the rectifier average input current is less than this value, there will be no gain control input to the ΔG cell, so that its gain will be zero and the expandor output will be zero. As the input level is raised, the input current will exceed $1.3V/R_a$ and the expandor output will become active. For large input signals, R_a will have little effect. The result of this is that we will deviate from the 2 to 1 expansion, present at high levels, to an infinite expansion at low levels where the output shuts off completely. Figure 8-98 shows some examples of tracking curves which can be obtained. Complementary curves would be obtained for a compressor, where at low level signals the result would be infinite compression. The bleed current through R_a will be a function of temperature because of the two V_{be} drops, so the low level tracking will drift with temperature. If a negative supply is available, it would be desirable to tie R_a to that, rather than ground, and to increase its value accordingly. The bleed current will then be less sensitive to the V_{be} temperature drift.

R_b will supply an extra current to the rectifier equal to $(V_{CC} - 1.3V)R_b$. In this case, the expandor transfer characteristic will deviate towards 1 to 1 at low levels. At low levels the

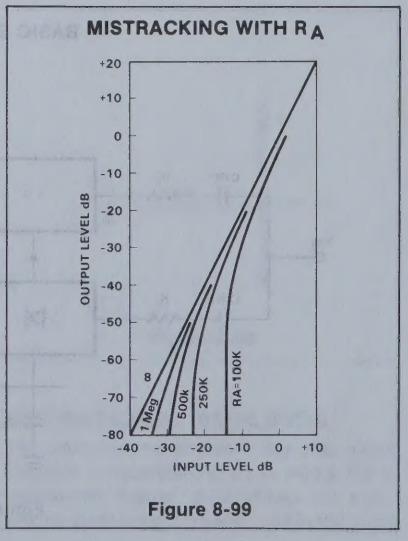


Figure 8-99

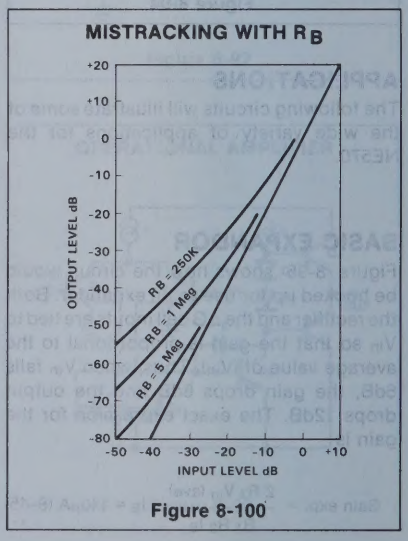


Figure 8-100

expandor gain will stop dropping and the expansion will cease. In a compressor this would lead to a lack of compression at low levels. Figure 8-100 shows some typical transfer curves. An R_b value of approximately 2.5Meg would trim the low level tracking so as to match the Bell system N2 trunk compandor characteristic.

RECTIFIER BIAS CURRENT CANCELLATION

The rectifier has an input bias current of between 50 and 100nA. This limits the dynamic range of the rectifier to about 60dB. It also limits the amount of attenuation of the ΔG cell. The rectifier dynamic range may be increased by about 20dB by the bias current trim network shown in Figure 8-101. Figure 8-111 shows the rectifier performance with and without current cancellation.

ATTACK AND DECAY TIME

The attack and decay times of the compandor are determined by the rectifier filter time constant $10K \times C_{rect}$. Figure 8-113 shows how the gain will change when the input signal undergoes a 10, 20, or 30dB change in level.

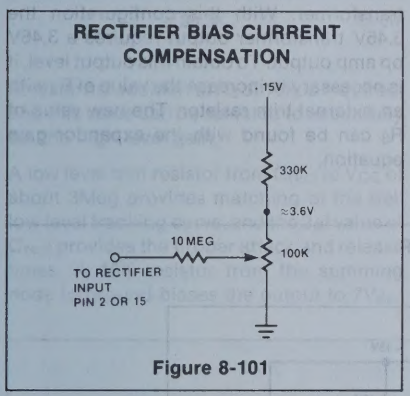


Figure 8-101

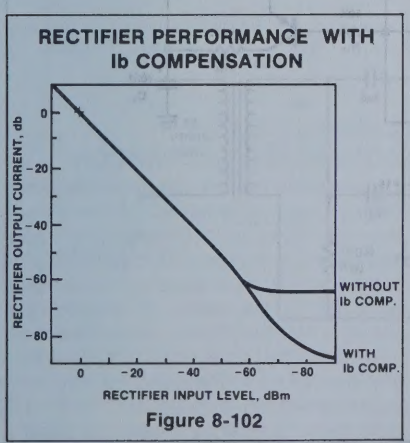


Figure 8-102

The attack time is much faster than the decay, which is desirable in most applications. Figure 8-104 shows the compressor attack envelope for a +12dB step in input level. The initial output level of 1 unit instantaneously rises to 4 units, and then starts to fall towards its final value of 2 units. The CCITT recommendation on attack and decay times for telephone system compandors, defines the attack time as when the envelope has fallen to a level of 3 units, corresponding to t = .15 in the figure. The CCITT recommends an attack time of 3± 2ms, which suggests an RC product of 20ms. Figure 8-105 shows the compressor output envelope when the input level is suddenly reduced 12dB. The output, initially at a level of 4 units, drops 12dB to 1 unit and then rises to its final value of 2 units. The CCITT defines release time as when the output has risen to 1.5 units, and suggests a value of 13.5 ± 9ms. This corresponds to t = .675 in the figure, which gain suggests a 20ms RC product. Since R_1 = 10K, the CCITT recommendations will be met if C_{rect} = 2μf.

There is a trade off between fast response and low distortion. If a small C_{rect} is used to get very fast attack and decay, some ripple will appear on the gain control line and produce distortion. As a rule, a 1μf C_{rect} will produce .2% distortion at 1kHz. The distortion is inversely proportional to both frequency and capacitance. Thus, for telephone applications where C_{rect} = 2μf, the ripple would cause .1% distortion at 1kHz and .33% at 300hz. The low frequency distortion generated by a compressor would be cancelled (or undistorted) by an expandor, providing that they have the same value of C_{rect}.

FAST ATTACK, SLOW RELEASE HARD LIMITER

The NE570/571 can be easily used to make an excellent limiter. Figure 8-109 shows a typical circuit which requires 1/2 of an NE570/571, 1/2 of an LM339 quad comparator, and a pnp transistor. For small signals, the ΔG cell is nearly off, and the circuit runs at unity gain as set by R_8, R_7. When the output signal tries to exceed a + or - 1 volt peak, a comparator threshold is exceeded. The pnp is turned on and rapidly charges C_4 which activates the ΔG cell. Negative feedback through the ΔG cell reduces the gain, and the output signal level. The attack time is set by the RC product of R_{18} and C_4, and the release time is determined by C_4 and the internal rectifier resistor, which is 10K. The circuit shown attacks in less than 1ms and has a release time constant of 100ms. R_9 trickles about .7μA through the rectifier to

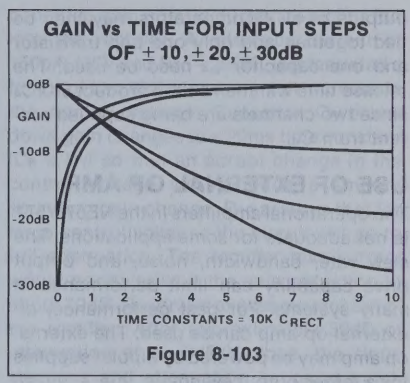


Figure 8-103

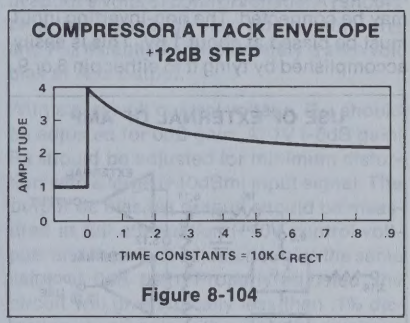


Figure 8-104

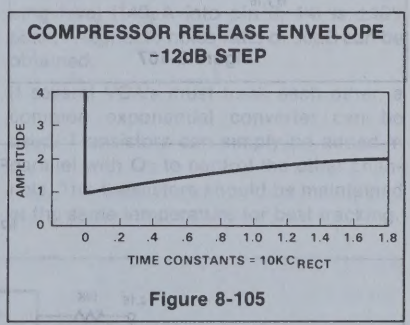


Figure 8-105

prevent C_4 from becoming completely discharged. The gain cell is activated when the voltage on pin 1 or 16 exceeds two diode drops. If C_4 were allowed to completely discharge, there would be a slight delay before it recharged to > 1.2V and activated limiting action.

A stereo limiter can be built out of 1 NE570/571, 1 LM339 and two pnp transistors. The resistor networks R_{12}, R_{13} and R_{14}, R_{15}, which set the limiting thresholds, could be common between channels. To gang the stereo channels together (limiting in one channel will produce a corresponding gain change in the second channel to maintain the balance of the stereo image), then pins 1 and 16 should be jumpered together. The

outputs of all 4 comparators may then be tied together, and only one pnp transistor and one capacitor C_4 need be used. The release time will then be the product $5K \times C_4$ since two channels are being supplied current from C_4.

USE OF EXTERNAL OP AMP

The operational amplifiers in the NE570/571 is not adequate for some applications. The slew rate, bandwidth, noise, and output drive capability can limit performance in many systems. For best performance, an external op amp can be used. The external op amp may be powered by bipolar supplies for a larger output swing.

Figure 8-107 shows how an external op amp may be connected. The non-inverting input must be biased at about 1.8V. This is easily accomplished by tying it to either pin 8 or 9,

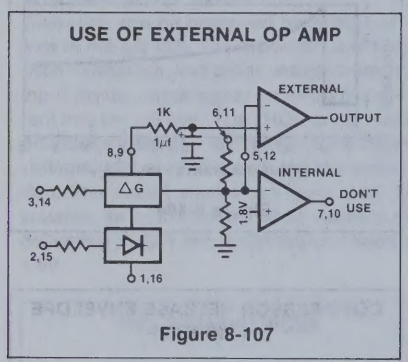


Figure 8-107

the THD trim pins, since these pins sit at 1.8V. An optional RC decoupling network is shown which will filter out the noise from the NE570/571 reference (typically about 10μV in 20kHz BW). The inverting input of the external op amp is tied to the inverting input of the internal op amp. The output of the external op amp is then used, with the internal op amp output left to float. If the external op amp is used single supply, (+V_{CC} and ground), it must have an input common mode range down to less than 1.8V.

N2 COMPANDOR

There are four primary considerations involved in the application of the NE570/571 in an N2 compandor. These are matching of input and output levels, accurate 600Ω input and output impedances, conformance to the Bell system low level tracking curve, and proper attack and release times.

Figure 8-108 shows the implementation of an N2 compressor. The input level of .245V rms is stepped up to 1.41Vrms by the 600Ω: 20KΩ matching transformer. The 20K input resistor properly terminates the transformer. An internal 20KΩ resistor (R_3) is provided, but for accurate impedance termination an external resistor should be used. The output impedance is provided by the 4K output resistor and the 4KΩ: 600Ω output transformer. The .275V RMS output level requires a 1.41V op amp output level. This can be provided by increasing the value of R_2 with an external resistor, which can be selected to fine trim the gain. A rearrangement of the compressor gain equation (6) allows us to determine the value for R_2.

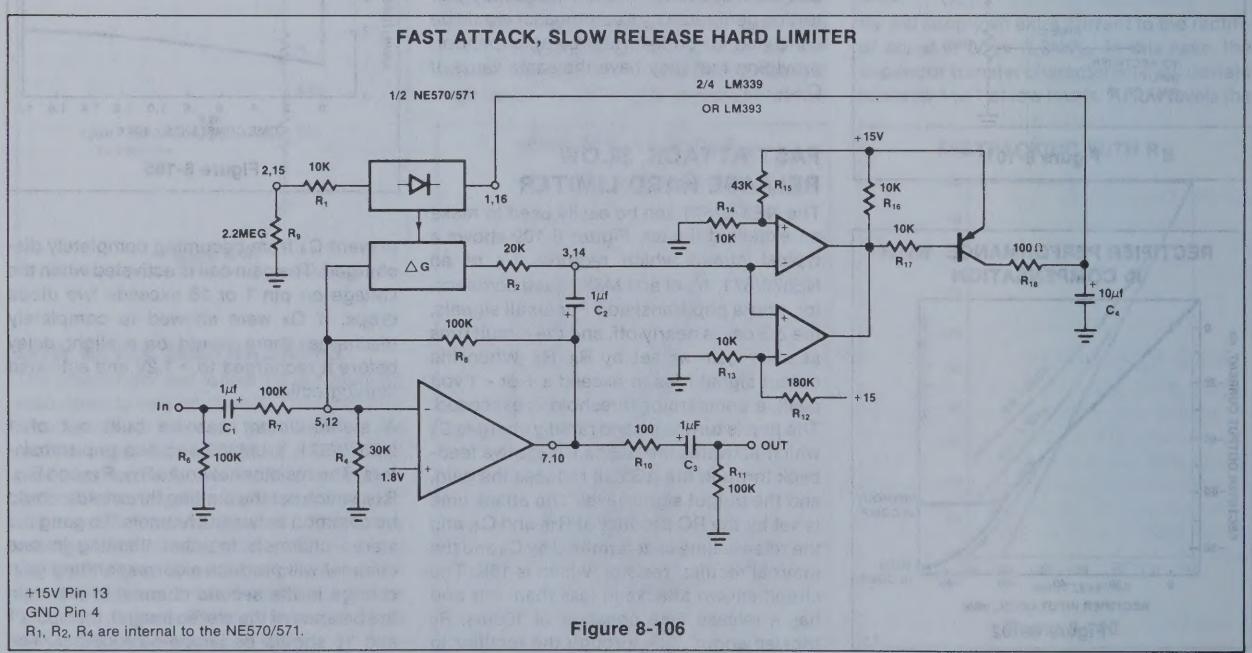
$$R_2 = \frac{\text{Gain}^2\, R_3\, V_{in\ ave}}{R_1\, I_B} = \frac{1^2 \times 2 \times 20K \times 1.27}{10K \times 140\mu A}$$

$$= 36.3K \qquad (8\text{-}49)$$

The external resistance required will thus be 36.3K - 20K = 16.3K.

The Bell compatible low level tracking characteristic is provided by the low level trim resistor from C_{rect} to V_{CC}. As shown in Figure 9-98 this will skew the system to a 1:1 transfer characteristic at low levels. The 2μf rectifier capacitor provides attack and release times of 3ms and 13.5ms respectively, as shown in Figures 8-88 and 8-89. The R-C-R network around the op amp provides dc feedback to bias the output at dc.

An N2 expandor is shown in Figure 8-109. The input level of 3.27Vrms is stepped down to 1.33V by the 600Ω: 100Ω transformer, which is terminated with a 100Ω resistor for accurate impedance matching. The output impedance is accurately set by the 150Ω output resistor and the 150Ω: 600Ω output transformer. With this configuration the 3.46V transformer output requires a 3.46V op amp output. To obtain this output level, it is necessary to increase the value of R_3 with an external trim resistor. The new value of R_3 can be found with the expandor gain equation.



+15V Pin 13
GND Pin 4
R_1, R_2, R_4 are internal to the NE570/571.

Figure 8-106

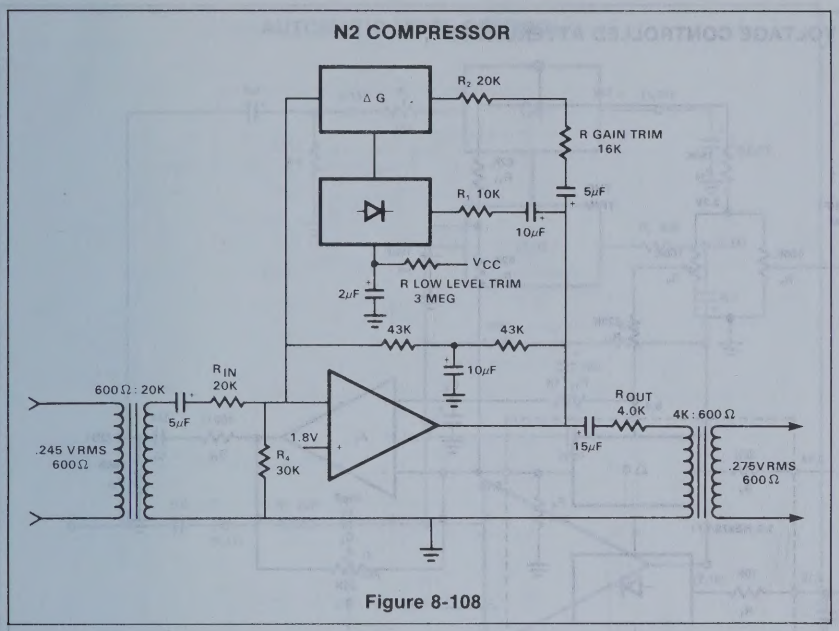


Figure 8-108

$$R_3 = \frac{R_1 R_2 I_B \text{ Gain}}{2 V_{in \text{ ave}}} = \frac{10K \times 20K \times 140\mu A \times 2.6}{2 \times 1.20}$$

$$= 30.3K \qquad (8\text{-}50)$$

An external addition to R_3 of 10K is required, and this value can be selected to accurately set the high level gain.

A low level trim resistor from C_{rect} to V_{CC} of about 3Meg provides matching of the Bell low level tracking curve, and the 2μf value of C_{rect} provides the proper attack and release times. A 16K resistor from the summing node to ground biases the output to $7V_{dc}$.

VOLTAGE CONTROLLED ATTENUATOR

The variable gain cell in the NE570/571 may be used as the heart of a high quality voltage controlled amplifier (VCA). Figure 8-110 shows a typical circuit which uses an external op amp for better performance, and an exponential converter to get a control characteristic of -6dB/V. Trim networks are shown to null out distortion and dc shift, and to fine trim gain to 0dB with zero volts of control voltage.

Op amp A_2 and transistors Q_1 and Q_2 form the exponential converter generating an exponential gain control current, which is fed into the rectifier. A reference current of 150μA, (15V and R_{20} = 100K), is attenuated a factor of two (6dB) for every volt increase in the control voltage. Capacitor C_6 slows down gain changes to a 20ms time constant (C_6 x R_1) so that an abrupt change in the control voltage will produce a smooth sounding gain change. R_{18} assures that for large control voltages the circuit will go to full attenuation. The rectifier bias current would normally limit the gain reduction to about 70dB. R_{18} draws excess current out of the rectifier. After approximately 50dB of attenuation at a -6dB/V slope, the slope steepens and attenuation becomes much more rapid until the circuit totally shuts off at about 9 volts of control voltage. A_1 should be a low noise high slew rate op amp. R_{13} and R_{14} establish approximately a zero volt bias at A_1's output.

With a zero volt control voltage, R_{19} should be adjusted for 0dB gain. At 1V (-6dB gain) R_9 should be adjusted for minimum distortion with a large (+10dBm) input signal. The output dc bias (A_1 output) should be measured at full attenuation (+10V control voltage) and then R_8 is adjusted to give the same value at 0dB gain. Properly adjusted, the circuit will give typically less than .1% distortion at any gain with a dc output voltage variation of only a few millivolts. The clipping level (140μA into pin 3, 14) is ±10V peak. A signal to noise ratio of 90dB can be obtained.

If several VCA's must track each other, a common exponential converter can be used. Transistors can simply be added in parallel with Q_2 to control the other channels. The transistors should be maintained at the same temperature for best tracking.

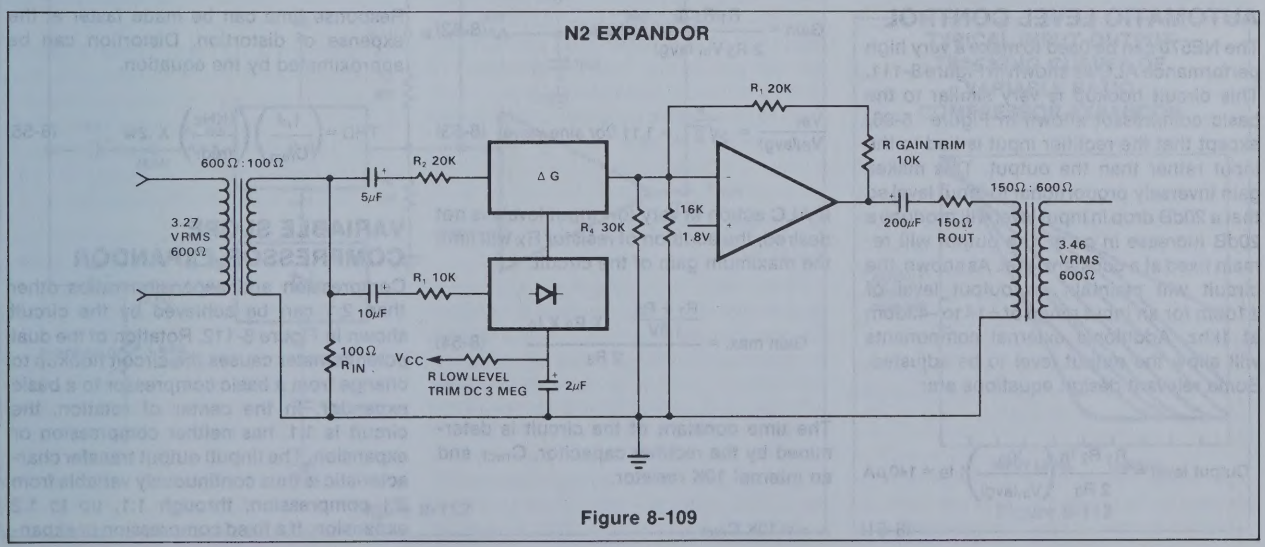


Figure 8-109

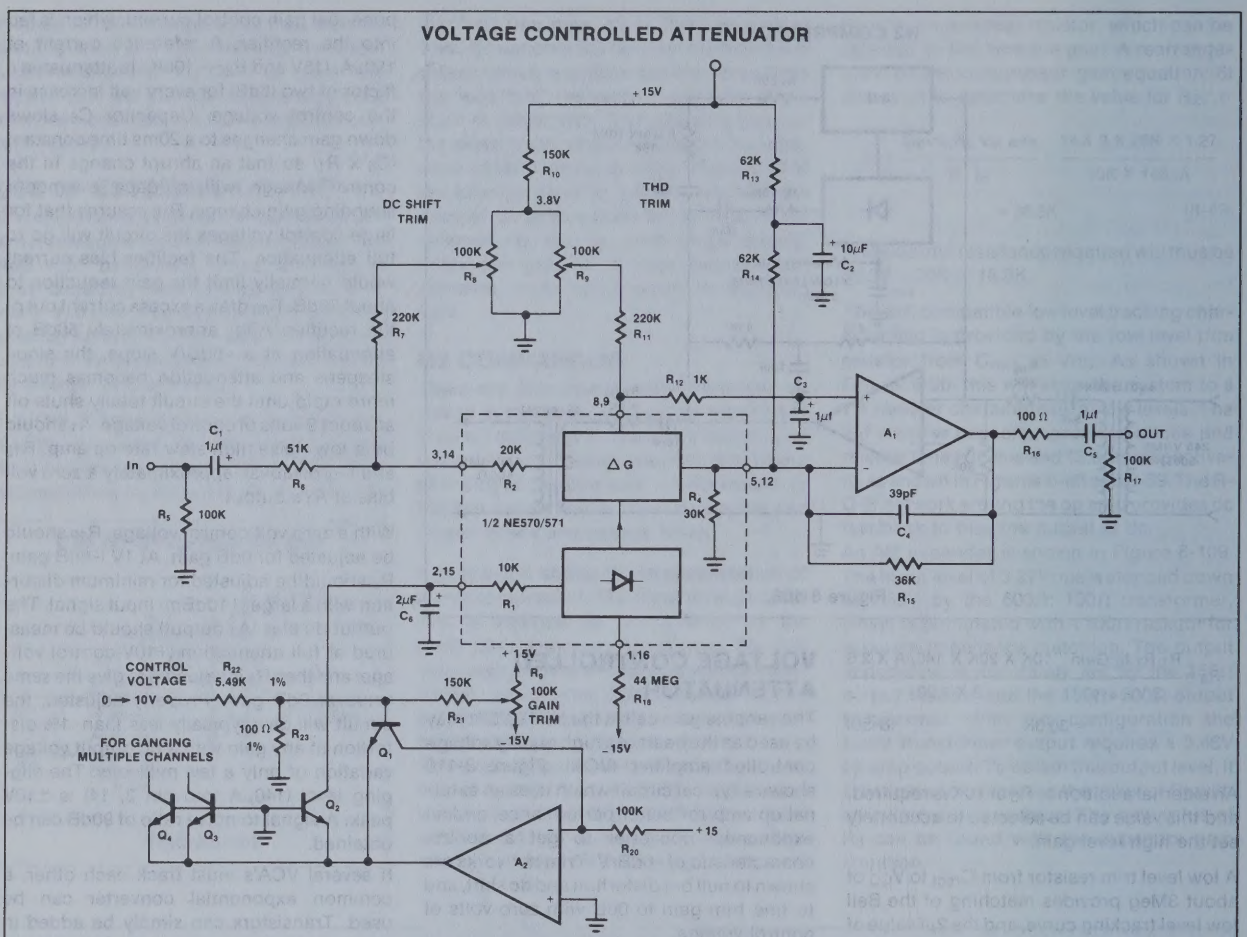


Figure 8-110

AUTOMATIC LEVEL CONTROL

The NE570 can be used to make a very high performance ALC as shown in Figure 8-111. This circuit hookup is very similar to the basic compressor shown in Figure 8-96, except that the rectifier input is tied to the input rather than the output. This makes gain inversely proportional to input level so that a 20dB drop in input level will produce a 20dB increase in gain. The output will remain fixed at a constant level. As shown, the circuit will maintain an output level of ±1dbm for an input range of +14 to -43dbm at 1khz. Additional external components will allow the output level to be adjusted. Some relevant design equations are:

$$\text{Output level} = \frac{R_1 R_2 I_B}{2 R_3}\left(\frac{V_{in}}{V_{in(avg)}}\right);\ I_B = 140\,\mu A \qquad (8\text{-}51)$$

$$\text{Gain} = \frac{R_1 R_2 I_B}{2 R_3 V_{in}\,(avg)} \quad \text{where} \qquad (8\text{-}52)$$

$$\frac{V_{IN}}{V_{IN(avg)}} = \frac{\pi}{2\sqrt{2}} = 1.11 \text{ (for sine wave)} \qquad (8\text{-}53)$$

If ALC action at very low input levels is not desired, the addition of resistor R_X will limit the maximum gain of the circuit.

$$\text{Gain max.} = \frac{\frac{R_1 + R_X}{1.8V} \times R_2 \times I_B}{2 R_3} \qquad (8\text{-}54)$$

The time constant of the circuit is determined by the rectifier capacitor, C_{rect}, and an internal 10K resistor.

$$\tau = 10K\ C_{rect}$$

Response time can be made faster at the expense of distortion. Distortion can be approximated by the equation.

$$THD = \left(\frac{1\mu f}{C_{rect}}\right)\left(\frac{1KHz}{freq.}\right) \times .2\% \qquad (8\text{-}55)$$

VARIABLE SLOPE COMPRESSOR-EXPANDOR

Compression and expansion ratios other than 2:1 can be achieved by the circuit shown in Figure 8-112. Rotation of the dual potentiometer causes the circuit hookup to change from a basic compressor to a basic expandor. In the center of rotation, the circuit is 1:1, has neither compression or expansion. The (input) output transfer characteristic is thus continuously variable from 2:1 compression, through 1:1, up to 1:2 expansion. If a fixed compression or expan-

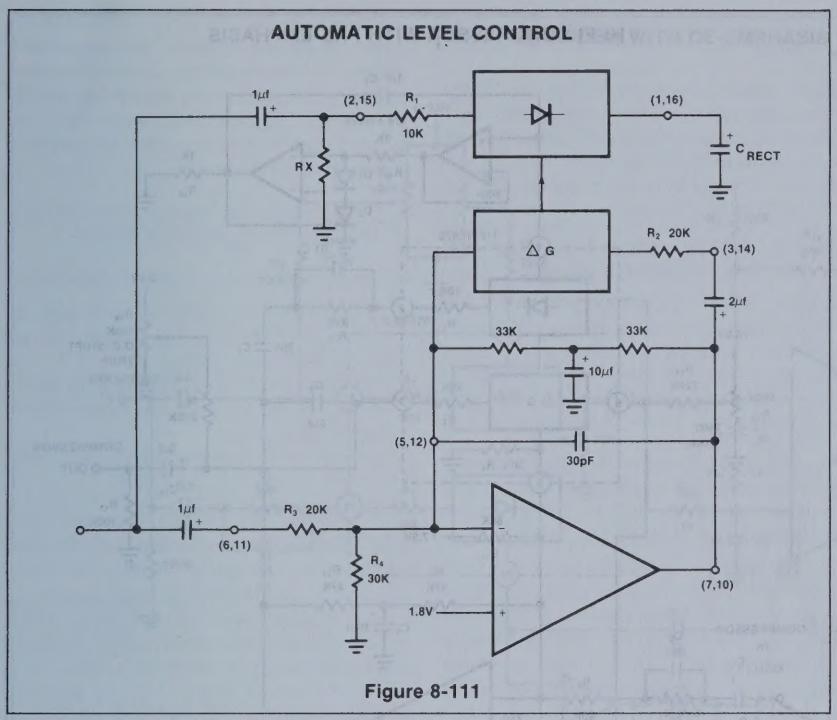


Figure 8-111

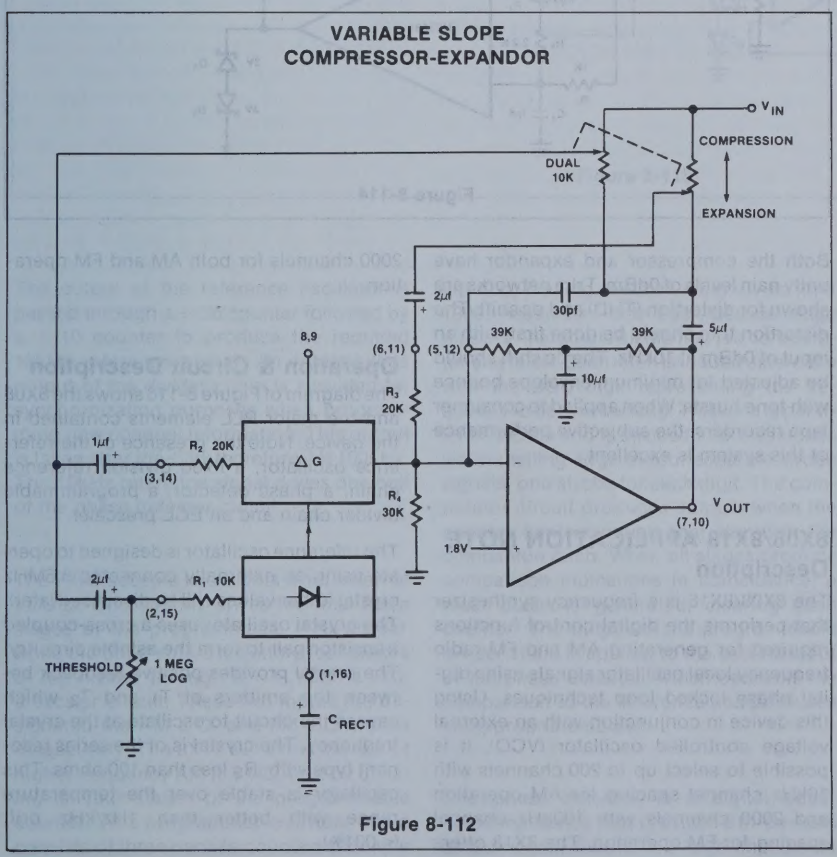


Figure 8-112

sion ratio is desired, proper selection of fixed resistors can be used instead of the potentiometer. The optional threshold resistor will make the compression or expansion ratio deviate towards 1:1 at low levels. A wide variety of (input) output characteristics can be created with this circuit, some of which are shown in Figure 8-113.

HI FI COMPANDOR

The NE570 can be used to construct a high performance compandor suitable for use with music. This type of system can be used for noise reduction in tape recorders, transmission systems, bucket brigade delay lines, and digital audio systems. The circuits to be described contain features which improve performance, but are not required for all applications.

A major problem with the simple NE570 compressor (Figure 8-96) is the limited op amp gain at high frequencies. For weak input signals, the compressor circuit operates at high gain and the 570 op amp simply runs out of loop gain. Another problem with the 570 op amp is its limited slew rate of about .6v/μs. This is a limitation of the expandor, since the expandor is more likely to produce large output signals than a compressor.

Figure 8-114 is a circuit for a high fidelity compressor which uses an external op amp and has a high gain and wide bandwidth. An input compensation network is required for stability.

Another feature of the circuit in Figure 8-114 is that the rectifier capacitor (C_9) is not grounded, but is tied to the output of an op amp circuit. This circuit, built around an LM324, speeds up the compressor attack time at low signal levels. The response times

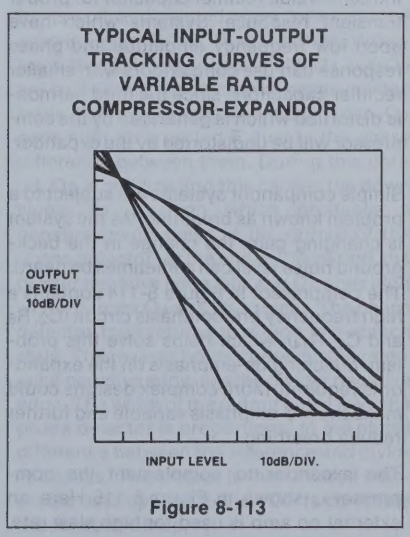


Figure 8-113

of the simple expandor and compressor (Figures 8-95 and 8-96),) become longer at low signal levels. The time constant is not simply $10K \times C_{rect}$, but is really

$$\left(10K + 2\left(\frac{.026V}{I_{rect}}\right)\right) \times C_{rect} \quad (8\text{-}56)$$

When the rectifier input level drops from 0dBm to -30dBm, the time constant increases from $10.7K \times C_{rect}$ to $32.6K \times C_{rect}$. In systems where there is unity gain between the compressor and expandor, this will cause no overall error. Gain or loss between the compressor and expandor will be a mistracking of low signal dynamics. The circuit with the LM324 will greatly reduce this problem for systems which cannot guarantee the unity gain.

When a compressor is operating at high gain, (small input signal), and is suddenly hit with a signal, it will overload until it can reduce its gain. Overloaded the output will attempt to swing rail to rail. This compressor is limited to approximately a 7V peak to peak output swing by the brute force clamp diodes D_3 and D_4. The diodes cannot be placed in the feedback loop because their capacitance would limit high frequency gain. The purpose of limiting the output swing is to avoid overloading any succeeding circuit such as a tape recorder input.

The time it takes for the compressor to recover from overload is determined by the rectifier capacitor C_9. A smaller capacitor will allow faster response to transients, but will produce more low frequency third harmonic distortion due to gain modulation. A value of 1 μf seems to be a good compromise value and yields good subjective results. Of course, the expandor should have exactly the same value rectifier capacitor for proper transient response. Systems which have good low frequency amplitude and phase response can use compandors with smaller rectifier capacitors, since the third harmonic distortion which is generated by the compressor will be undistorted by the expandor.

Simple compandor systems are subject to a problem known as breathing. As the system is changing gain, the change in the background noise level can sometimes be heard. The compressor in Figure 8-114 contains a high frequency pre-emphasis circuit (C_2, R_5 and C_8, R_{14}), which helps solve this problem. Matching de-emphasis on the expandor is required. More complex designs could make the pre-emphasis variable and further reduce breathing.

The expandor to complement the compressor is shown in Figure 8-115. Here an external op amp is used for high slew rate.

HI-FI COMPRESSOR WITH PRE-EMPHASIS

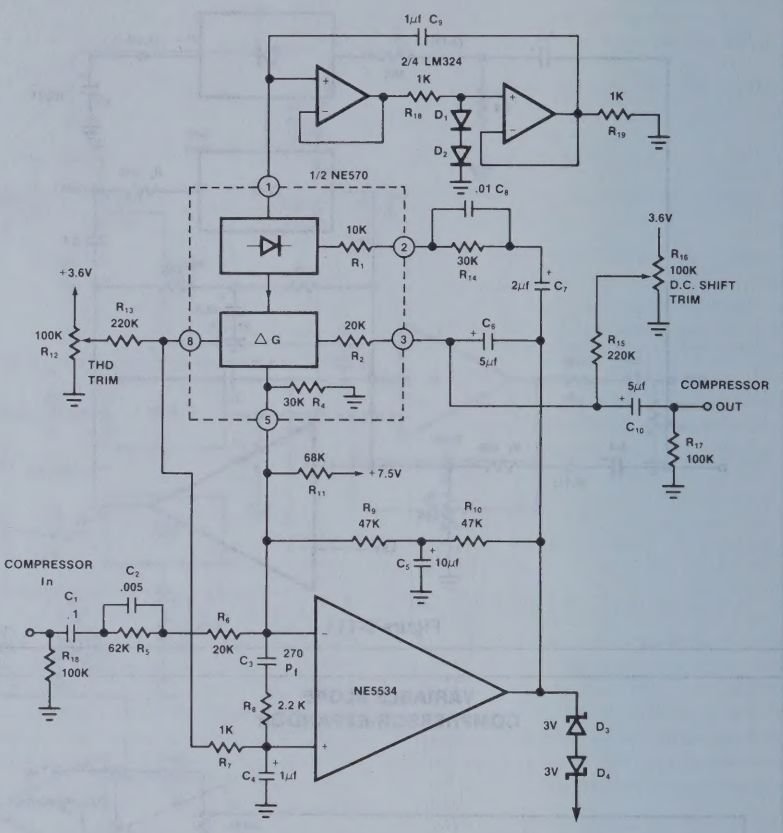


Figure 8-114

Both the compressor and expandor have unity gain levels of 0dBm. Trim networks are shown for distortion (THD) and dc shift. The distortion trim should be done first, with an input of 0dBm at 10kHz. The dc shift should be adjusted for minimum envelope bounce with tone bursts. When applied to consumer tape recorders, the subjective performance of this system is excellent.

8X08/8X18 APPLICATION NOTE

Description

The 8X08/8X18 is a frequency synthesizer that performs the digital control functions required for generating AM and FM radio frequency local oscillator signals using digital phase locked loop techniques. Using this device in conjunction with an external voltage controlled oscillator (VCO), it is possible to select up to 200 channels with 10kHz channel spacing for AM operation and 2000 channels with 100kHz channel spacing for FM operation. The 8X18 offers 2000 channels for both AM and FM operation.

Operation & Circuit Description

The diagram of Figure 8-116 shows the 8X08 and the major PLL elements contained in the device. Note the presence of the reference oscillator, a fixed division reference chain, a phase detector, a programmable divider chain and an ECL prescaler.

The reference oscillator is designed to operate using an externally connected 3.6MHz crystal (other values will be discussed later). The crystal oscillator uses a cross-coupled transistor pair to form the astable circuitry. The crystal provides positive feedback between the emitters of T_1 and T_2 which causes the circuit to oscillate at the crystal frequency. The crystal is of the series resonant type with R_S less than 100 ohms. This oscillator is stable over the temperature range with better than 1Hz/kHz drift (<.001%).

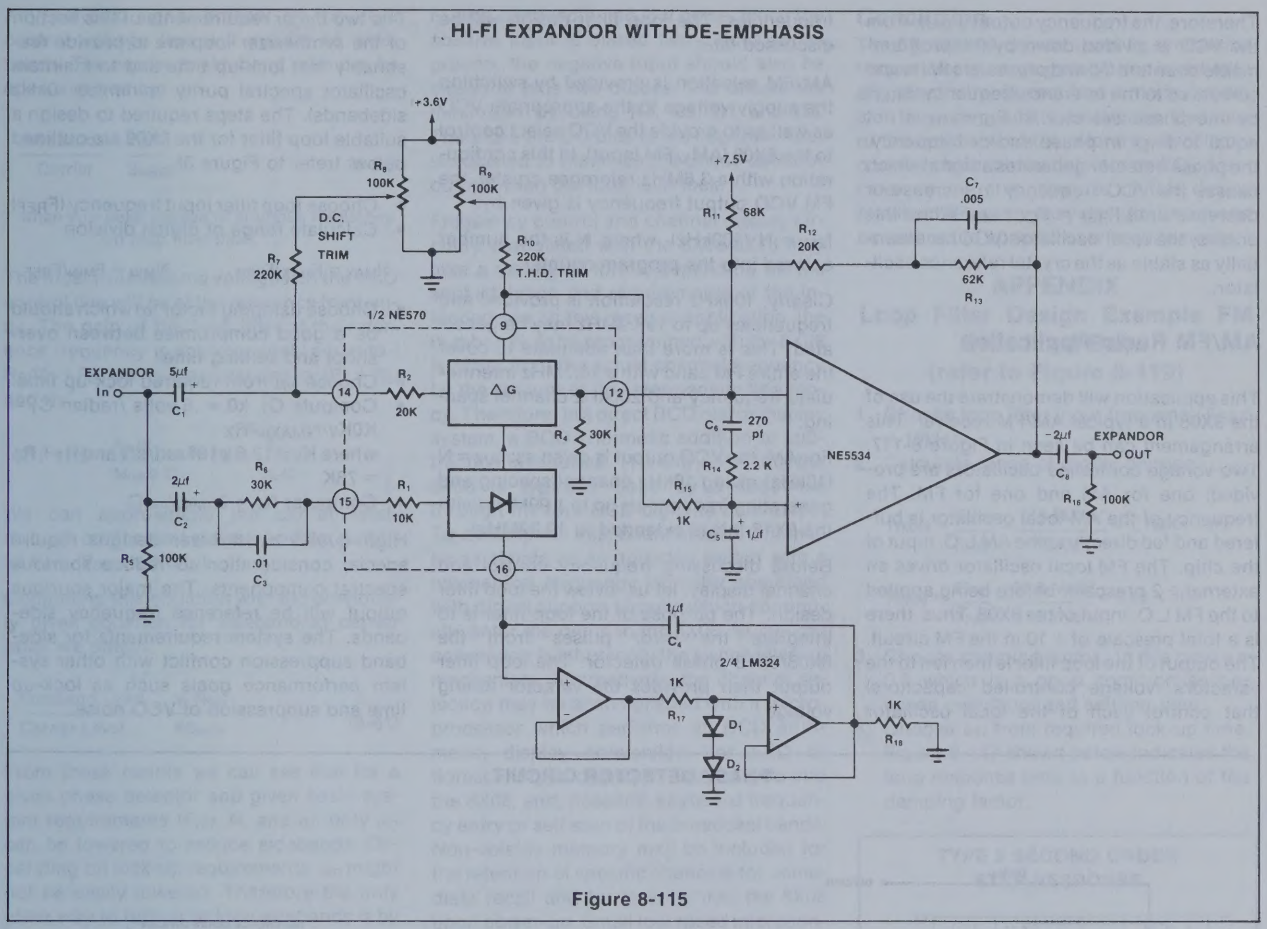


Figure 8-115

The output of the reference oscillator is passed through a ÷ 36 counter followed by a ÷ 10 counter to produce the required 10kHz reference signal. An intermediate output of the divider chain is provided for synchronization purposes when programming new channel information. This output is taken after the ÷ 36; therefore it is 100kHz. The 10kHz reference signal drives one half of the phase detector circuit.

The 8X08 accepts two inputs from external VCO(s). One directly drives the final three stages of the programmable (÷N) divider while the other enters the entire four stages of the divider through a ÷ 5, 80MHz ECL prescaler circuit. These two inputs are designated the AM L.O. and FM L.O. inputs respectively. The 8X18 will allow the use of higher frequency AM IF's (460kHz) by utilizing all four stages of the programmable counter. This programmable divider chain consists of three decade counters plus one flip flop, making the maximum divide limit 1999. Associated with each decade stage plus the final single bit flip flop is a comparator and latch. Each latch is loaded externally with the BCD digit representing the frequency to be synthesized. This data is parallel true BCD and is strobed into the latches via the falling edge of four separate strobe signals, one strobe for each digit. The comparator circuit produces outputs when the counter content equals that stored in the companion latch. When all stages produce comparison indications in coincidence, a reset pulse is generated, clearing each counter. The output of the programmable divider chain is applied to the second input of the phase detector, which performs the comparison to the reference and produces an appropriate output.

The phase detector is a digital edge-detecting device that provides a three-state output signal that is in a high impedance state when the two input signals are equal in phase and/or frequency. The phase detector circuit and related wave forms can be seen in Figure 8-116. With the phase detector in the high impedance state, Q_A and Q_B are both low. If the reference negative edge leads the divider negative edge, then Q_A goes high for a period E dual to the phase difference between them. During this period, Q_B is still low and this causes the down signal to go high which produces a negative-going pulse at the output of the phase detector. At the end of this period, the divider negative edge falls and Q_B goes high which causes Q_A and Q_B to clear. The phase detector thus returns to a high impedance state. The reverse holds true when the reference negative edge lags the divider negative edge. The width of the output pulse from the phase detector is proportional to the phase difference between the reference and divider signals. This output is then filtered (integrated) and applied to the VCO to complete the feedback loop.

Therefore, the frequency output (F_{OUT}) from the VCO is divided down by the programmable counters (N) and prescalers (M) is and compared to the reference frequency (F_{REF}) by the phase detector. If $F_{OUT/MN}$ is not equal to F_{REF} in phase and/or frequency, the phase detector generates a signal which causes the VCO frequency to increase or decrease until $F_{REF} = F_{OUT/MN}$. When this occurs, the local oscillator (VCO) is essentially as stable as the crystal reference oscillator.

AM/FM Radio Application

This application will demonstrate the use of the 8X08 in a typical AM/FM receiver. This arrangement can be seen in Figure 8-117. Two voltage controlled oscillators are provided: one for AM and one for FM. The frequency of the AM local oscillator is buffered and fed directly to the AM L.O. input of the chip. The FM local oscillator drives an external ÷ 2 prescaler before being applied to the FM L.O. input of the 8X08. Thus, there is a total prescale of ÷ 10 in the FM circuit. The output of the loop filter is then fed to the varactors (voltage controlled capacitors) that control each of the local oscillator frequencies. The loop filter design will be discussed later.

AM/FM selection is provided by switching the supply voltage to the appropriate VCO as well as to provide the VCO select control to the 8X08 (AM$\sqrt{}$FM input). In this configuration with a 3.6MHz reference crystal, the FM VCO output frequency is given by:

f_{FM} = N (100kHz), where N is the number entered into the program counter.

Clearly, 100kHz resolution is provided and frequencies up to 199.9MHz may be generated. This is more than adequate to cover the entire FM band with a 10.7MHz intermediate frequency and 200kHz channel spacing.

For AM, the VCO output is given as: f_{AM} = N (10kHz) giving 10kHz channel spacing and generating frequencies up to 1.99MHz (with the 8X18 this is extended to 19.99MHz).

Before discussing frequency control and channel display, let us review the loop filter design. The purpose of the loop filter is to integrate the error pulses from the 8X08/8X18 phase detector. The loop filter output then provides the varactor tuning voltage.

The two major requirements of this section of the synthesizer loop are to provide reasonably fast lock-up time and to maintain oscillator spectral purity (minimize 10kHz sidebands). The steps required to design a suitable loop filter for the 8X08 are outlined below: (refer to Figure 3)

- Choose loop filter input frequency (F_{REF})
- Calculate range of digital division

$N_{MAX} = F_{MAX}/F_{REF}$ $N_{MIN} = F_{MIN}/F_{REF}$

- Choose damping factor (α) which should be a good compromise between overshoot and settling time.
- Choose ω_N from required lock-up time.
- Compute C_1, k0 = .6 volts /radian $C_1 = K0Kv/N_{MAX}\omega^2R_X$ where Kv = 12.6 x 10^6 rad/s/v and $R_1 + R_3$ = 78K.
- Computer $R_2 = 2\alpha_{MIN}/\omega_N C$

High quality synthesizer designs require special consideration to reduce spurious spectral components. The major spurious output will be reference frequency sidebands. The system requirements for sideband suppression conflict with other system performance goals such as lock-up time and suppression of VCO noise.

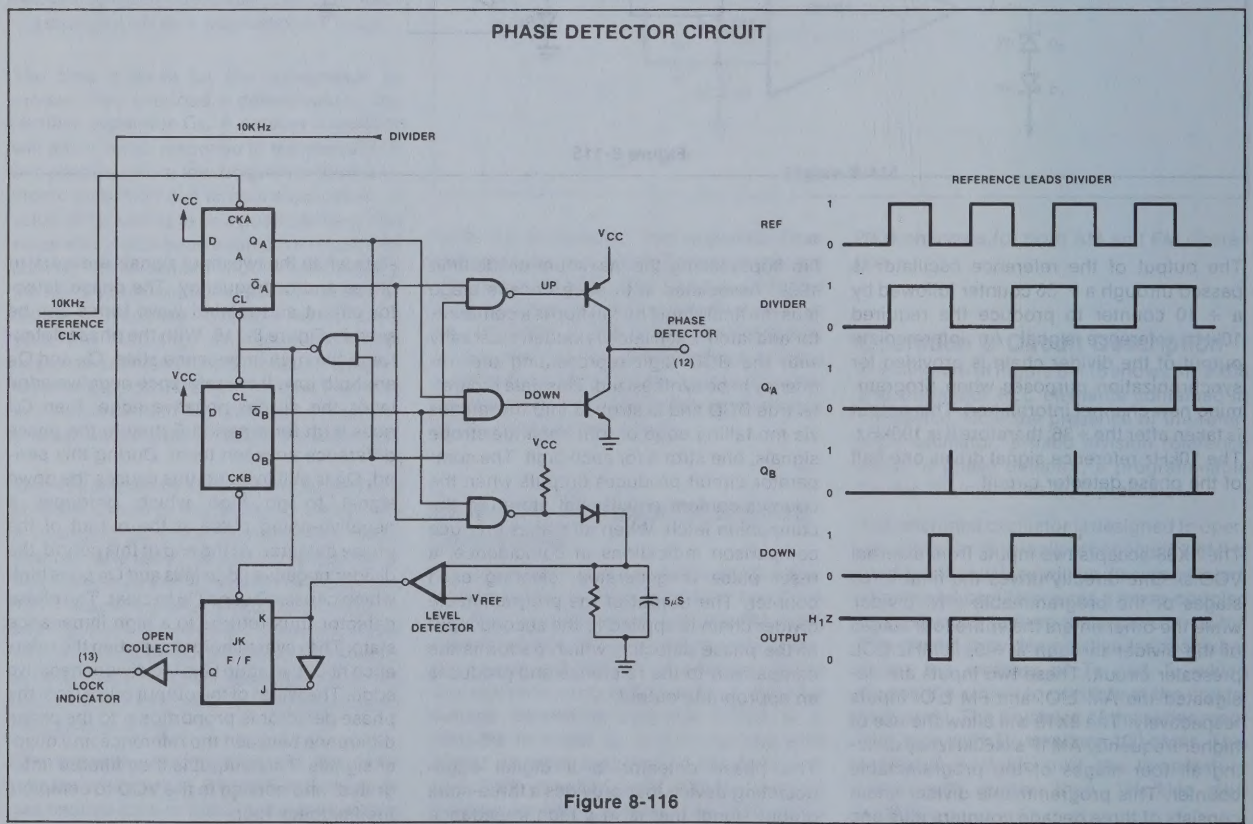


Figure 8-116

Any periodic signal present on the VCO control voltage line will appear as sidebands. The carrier to sideband ratio can be approximated by:

$$\frac{\text{Sidebands}}{\text{Carrier}} \approx \frac{V_C K_V}{2\omega_{REF}} \quad (8\text{-}60)$$

when V_C = peak voltage of spurious frequency on loop filter input

The most troublesome voltages on the VCO control line will be at the reference frequency. The gain of the loop filter at the reference frequency is approximately equal to $-R_2/R_1 + R_3$. Using the equations for $(R_1 + R_3)$ and R_2,

$$(R_1 + R_3) = \frac{K_O/K_V}{N\omega_N^2 C} \text{ and } R_2 = \frac{2\alpha}{\omega_n C}$$

We can approximate the carrier feedthrough component at the loop filter output as $V_c \approx (2\alpha\omega_N N/K0K_Y)$.

Combining this equation with the previously given equation for sideband to carrier ratio, we obtain:

$$\frac{\text{Sideband Level}}{\text{Carrier Level}} \approx \frac{V_c N\omega_n}{K0\omega_{ref}} \quad (8\text{-}61)$$

From these results we can see that for a given phase detector and given basic system requirements (F_{ref}, N, and α), only ω_n can be lowered to reduce sidebands. Depending on lock-up requirements, ω_n might not be easily lowered. Therefore the only other way to further reduce sidebands is by additional filtering. This additional filtering will give additional suppression given by Sup dB = $\text{Log}_{10}(\omega c/\omega_{ref})$ where ω is the added filter cut-off frequency. This filter should not affect the loop dynamic performance if ωc is chosen to be approximately five times ωn ($\omega c = 5\omega n$). This additional pole is the combination of R_1, R_3, C_2 as shown in Figure 3. One addiitonal pole can be added at the filter output to further improve spectral purity. (R_6, C_3). An example of this loop filter design for the FM broadcast band is given in the appendix of this application note.

It can be seen from the sideband to carrier suppression given, that it is important to minimize the phase detector output signal when the loop is in lock. Since the 8X08 has a three-state output and in a high impedance state when the loop is locked, care should be taken to minimize input offsets in the loop filter. Obviously, any offsets in the input to the loop filter will cause a change in tuning voltage and a phase detector error.

The NE542 was used for the loop filter operational amplifier because of its relatively wide bandwidth and low noise. Since the positive input is biased two diodes above ground, the negative input should also be biased at plus two diodes. The offsets are minimized by using R4, R5, D1 and D2. Therefore the DC bias at the negative input is adjusted to minimize the phase detector output when the loop is in lock.

Frequency control and channel display circuitry associated with the 8X08/8X18 may take a variety of forms, depending on the sophistication and requirements of the intended use. In this receiver application, the number, N, to be programmed with the 8X08 is offset from the actual channel frequency by the amount of the intermediate frequency. Therefore, in a direct BCD dial or display system, a BCD arithmetic addition or subtraction is required. The entry of N into the 8X08 is typically done by a sequence through the four BCD digits to be entered. To accomplish this, channel selection may be as simple as an encoded switch with a mechanical frequency indicator combined with digital support circuits which continually enter the digits to the 8X08. Numerical conversion is inherent in the switch/display mechanism. Alternatively, the channel selection may be accomplished with a microprocessor which performs all BCD arithmetic, display conversion (for LED or florescent type displays), entry of data into the 8X08, and, possibly, keyboard frequency entry or self scan of the broadcast bands. Non-volatile memory may be included for the retention of specific channels for immediate recall and for re-entry into the 8X08 upon power-up. Small low speed microcontrollers can be used to perform all the required 8X08 display and channel selection interfaces, including self-scan of the band and seek, whenever a signal is encountered meeting certain decision criteria like signal strength, etc.

General Application

The 8X08 was initially designed for direct use in AM/FM radio receivers, but, because of its flexibility, it can be used in a variety of other applications. The crystal for the reference oscillator may be set at any convenient value to provide a reference frequency, which produces the proper channel spacing. Various crystal values can provide resolution from 4kHz to 25kHz with maximum frequencies from near 800kHz up to 100MHz, the maximum clock rate of the ECL pre-scaler. Therefore, the 8X08 may be used in a variety of PLL frequency synthesis applications, including various multi-band receivers and transmitters plus test equipment and signal generators.

Conclusion

The 8X08/8X18 can be used to synthesize frequencies of varying resolution in virtually any spectral range required in modern radio and telecommunications circuits. Because of the inclusion of the reference oscillator, counter chain, phase detector an ECL prescaler on the chip, the use of this device results in relatively easy designs which can be tailored to specific user requirements.

APPENDIX
Loop Filter Design Example FM Broadcast Band (refer to Figure 8-119)

1. Choose loop filter input frequency F_{REF} = 10kHz.
2. Calculate range of digital division.

$$N_{MAX} = \frac{F_{MAX}}{F_{REF}} = \frac{118.6\text{MHz}^*}{10\text{ kHz}} = 1.186 \times 10^4$$

$$N_{MIN} = \frac{F_{min}}{F_{REF}} = \frac{98.8\text{ MHz}^*}{10\text{ kHz}} = 9.88 \times 10^3$$

3. Choose damping factor. In this case α = 0.8 which is a good compromise between overshoot and settling time.
4. Choose ω_N from required lock-up time. Figure 8-117 shown below indicates the loop response time as a function of the damping factor.

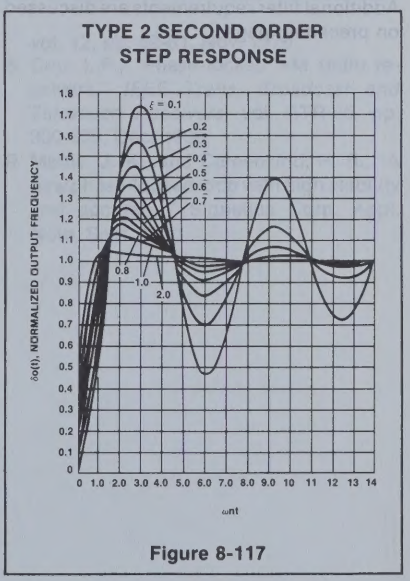


Figure 8-117

NOTE: (* Radio frequency plus 10.7MHz IF)

Figure 8-117 shows that the loop will settle to within 5% of its final value at $\omega_N T = 4.5$ if we use a damping factor of α = 0.8. The required lock-up time was arbitrarily chosen to be 50 ms.

$$\omega_N = \frac{\omega_N R}{T} = \frac{4.5}{50 \times 10^{-3}} = 90 \text{ Rad/Sec.}$$

5. To compute C, the phase detector gain and R_X must be known. Since the phase detector gain for the 8X08/8X18 is not specified, it was calculated by assuming a 180° phase error would produce it 50% duty cycle output. The phase detector gain, K0 is therefore:

$$K0 = \frac{4.2 - .3V}{2} = .62 \text{ volts/radian}$$

where
4.2 = maximum amplitude of 0 detector
0.3V = minimum amplitude of 0 detector
R_X was chosed to be 78K ohms.

Therefore:

$$C_1 = \frac{K0Kv}{N_{MAX}\omega_N 2R_X} \quad Kv\ 12.6 \times 10^6 \text{ Rad/S/V}$$

$$C = \frac{.62 \times 12.6 \times 10^6}{1.186 \times 10^4 \times 90 \times 90 \times 78 \times 10^3} = 1\ \mu f$$

6. R_2 may now be calculated:

$$R_2 = \frac{2 \text{ MIN}}{\omega_N C} = \frac{2 \times .8}{90 \times 1 \times 10^{-6}} = 18K$$

Additional filter requirements are discussed on preceding page.

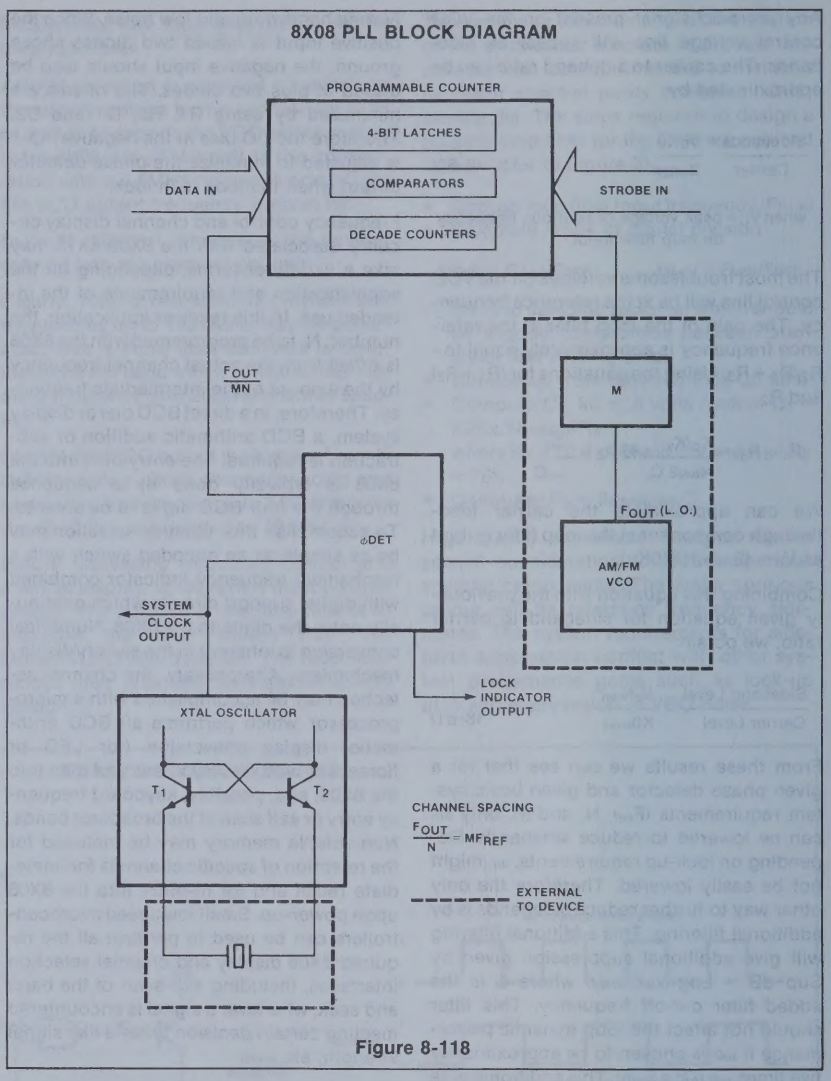


Figure 8-118

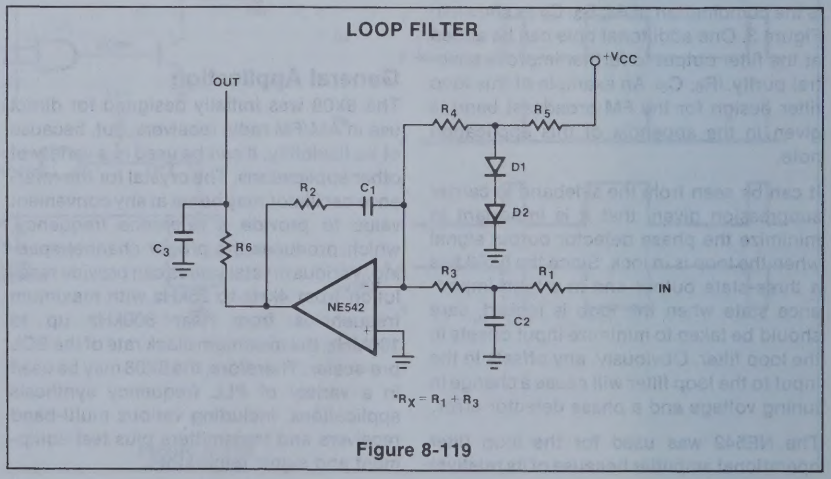


Figure 8-119

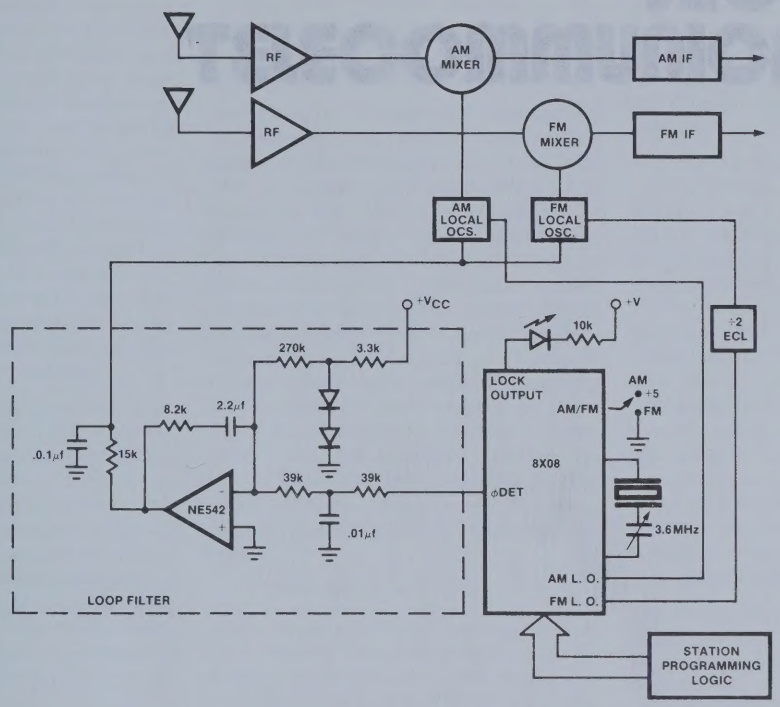


Figure 8-120

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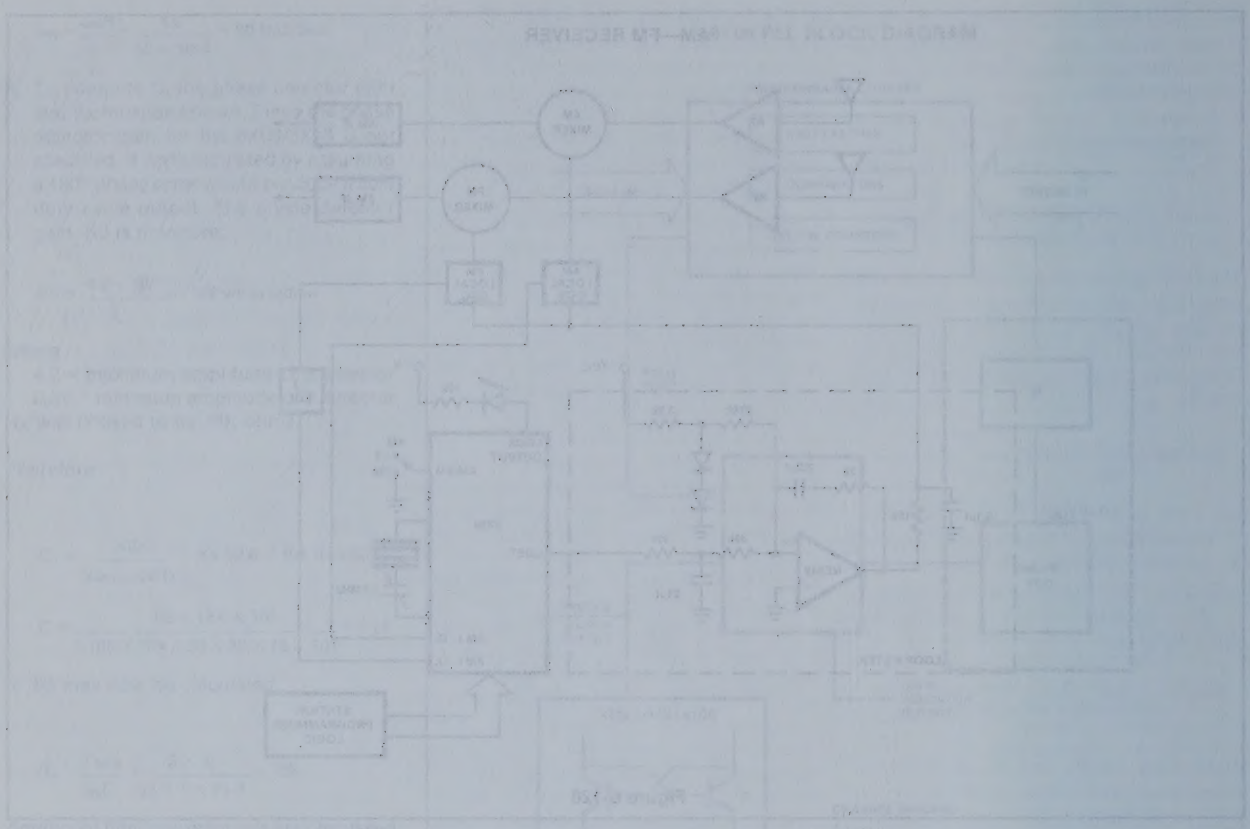
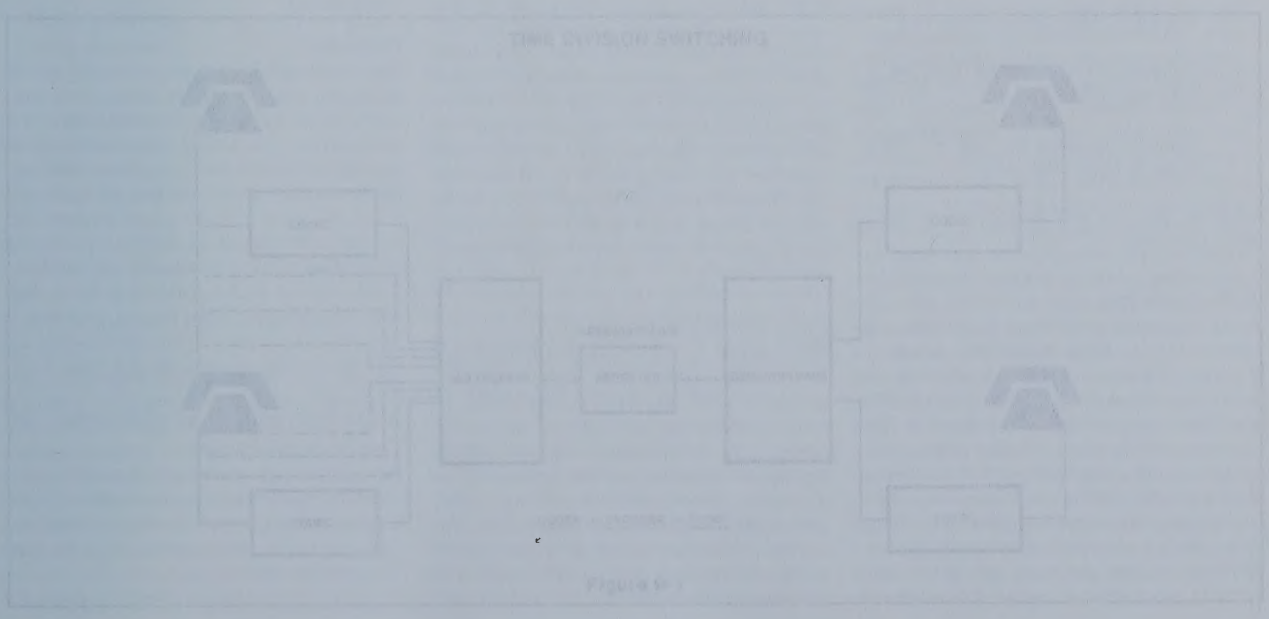


SECTION 9
TELECOMMUNICATIONS



INTRODUCTION

When telephone communication was first introduced and for a considerable number of years thereafter, the speech signals were conveyed across fairly long distances by a pair of copper wires. This type of transmission was adequate (provided the distances were not too long), since degradation of the signal due to noise, distortion, etc., were very disturbing. The use of line amplifiers improved the situation and the introduction of co-axial transmission helped considerably. However, the rise in traffic necessitated the number of lines to be increased considerably, and resulted in higher costs due to the shortage of copper cable. This led to the requirement of packing more channels into the same transmission medium.

One of the early ways this was done (it is still used at present) was by use of carrier frequencies. The so-called FDM (Frequency Division Multiplexing) system uses many channels spaced every 4kHz. However, the signals conveyed over the transmission medium are still analog, leading to the attendant problems of maintaining good signal-to-noise ratio, low distortion, etc. The desire to be more or less independent of the transmission medium but still convey the necessary information over long distances has led to more esoteric schemes.

The Present System

In the early sixties, the Bell system introduced their D1 system which used PCM (Pulse Code Modulation) techniques. The signals conveyed over the transmission medium was in digital form so that the effects of noise, distortion, etc., introduced by the medium were minimized. To gain a better understanding of this process, consider the system shown in figure 1. Even though a number of channels are shown, let us consider a single channel for the sake of convenience.

According to information theory and Shannon's theorem, to convey (between two points) all the information contained in a band of frequencies of bandwidth W, it is necessary and sufficient for 2W samples to be conveyed. In other words, if the samples contained in the band limited signal of bandwidth W are transmitted between two points at a sampling frequency of 2W, all the information content of the signal is essentially conveyed between the two points. In speech, most of the information and clarity is contained in the lower frequencies. Since one is not interested in high fidelity transmission over the telephone network, the speech signal is bandlimited over a range of 300Hz - 3400Hz by a transmit filter. Thus, once the incoming signal is bandlimited, we have

$$\text{Bandwidth } W \simeq 3400\text{Hz}$$

necessitating a minimum sampling rate of 2W or 6800Hz. Even though the transmit filter does roll off fast, the signal level is not really down to acceptable levels until a frequency of 4kHz has been reached. For this reason, the sampling rate is a 8kHz rate.

Encoding

The incoming speech may in reality be a very complex signal, but assume that it is represented as a single sine wave within the 300Hz - 3400Hz band. This single frequency sinusoidal passes through the transmit filter and is sampled by the S/H (Sample and Hold) at an 8kHz rate resulting in PAM (Pulse Amplitude Modulation) signal. This PAM signal passes through the analog multiplexer at the appropriate time, and is applied to the codec.

The codec which is used at the present time is an expensive and elaborate system. To reduce costs, it is actually shared between the 24 channels. Since it treats each channel the same, let us continue tracing the signal of a single channel as it is operated upon by the codec. The input to the codec as mentioned before is the PAM signal. The codec converts *each sample* of the input PAM into an 8 bit coded digital signal. This conversion, however, is not a linear process, but a companding one. The reason for this is that for a faithful reproduction at the receiving end of the transmitted information, it has been found that an accuracy of 12 bits plus sign is required. This is because of the variation in the talker levels, and intelligibility at low levels is a problem.

The companding which is employed follows a specific law. In North America, this is known as the μ-law and is described by the equation

$$y = \frac{\ln(1 + \mu x)}{\ln(1 + \mu)} \qquad (9.1)$$

where $\mu = 255$, x = input and y = output (in the D1 channel bank, $\mu = 100$ was used, but in the D3 channel bank, $\mu = 255$). The curve is shown in figure 2.

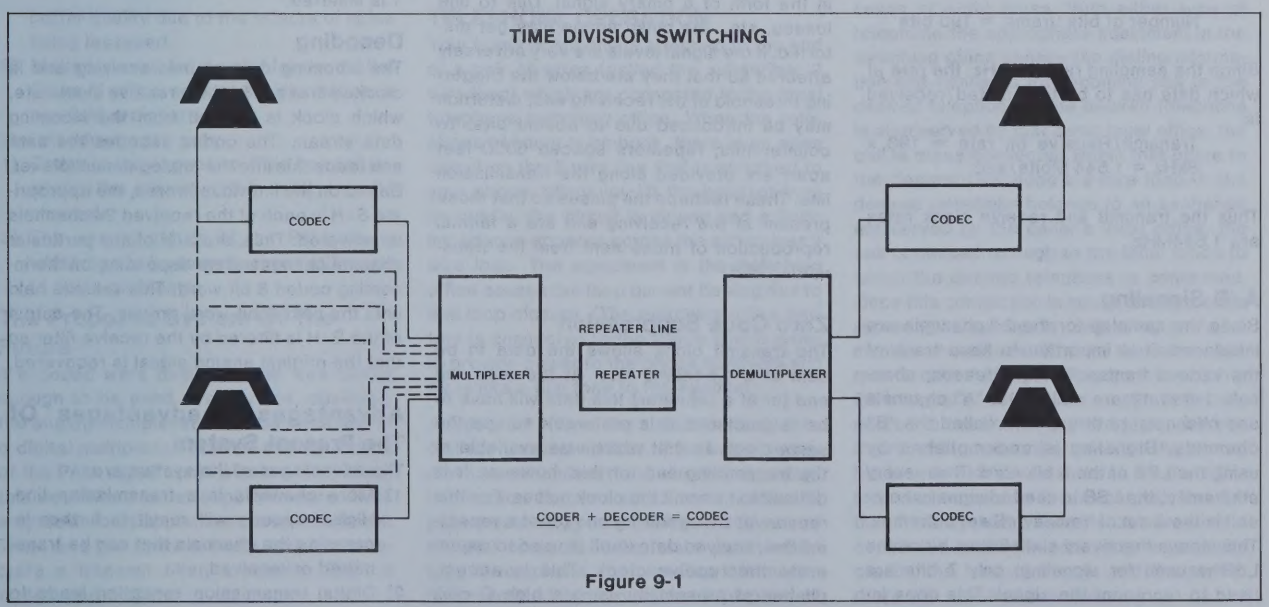


Figure 9-1

Since a smooth curve is difficult to synthesize, a piecewise linear approximation to the curve is what is generally used. The upper half and lower halves of the curve are each split up into 8 segments each and since the middle two are collinear and pass through the origin, the piecewise linear model is generally referred to as consisting of 15 segments. Each segment in turn is split up into 16 steps each, so that the total number of steps is 256 and due to collinearity, one can say $\mu = 255$. It should be evident from figure 2 that the resolution at low level signals is much better, but does not suffer at high level signals (this means that whether you are shouting at your spouse or whispering to your lover, both will get the message). The output of the codec is thus an 8 bit signal (1 sign bit + 3 chord bits and 4 level bits).

Since the codec is time shared among 24 channels in channel banks, the signals from the 24 channels are interlaced. In other words, after sample 1 from channel 1 has been encoded, sample 1 from channel 2 is encoded rather than sample 2 from channel 1. Next, sample 1 from channel 3 and so on until all first samples from the 24 channels have been encoded. After this has been completed, all the second samples of each of the 24 channels are encoded and so on (see figure 3).

Each completion of the individual samples from each of the channels is called a frame. Thus, since there are 8 bits/samples and 24 channels, the number of bits/frame is 8 x 24 = 192 bits. One bit called the "framing bit" is added to this so that:

Number of bits/frame = 193 bits

Since the sampling rate is 8kHz, the rate at which data has to be transmitted/received is:

Transmit/Receive bit rate = 193 x 8kHz = 1.544 Mbits/sec

Thus the transmit and receive clock rates are 1.544MHz.

A/B Signaling

Since the samples for the 24 channels are interlaced, it is important to keep track of the various frames. For this reason, channels 1 thru 12 are called the "A" channels and channels 13 thru 24 are called the "B" channels. Signaling is accomplished by using the LSB of the 8 bit word. Thus, every six frames, the LSB is used to signal whether it is the A set of frames or B set of frames. This means that every sixth frame, since the LSB is used for signaling, only 7 bits are used to represent the signal. This does introduce some distortion, but it is insignificant. This method of signaling is known as A/B signaling and is standard practice in D3 channel banks.

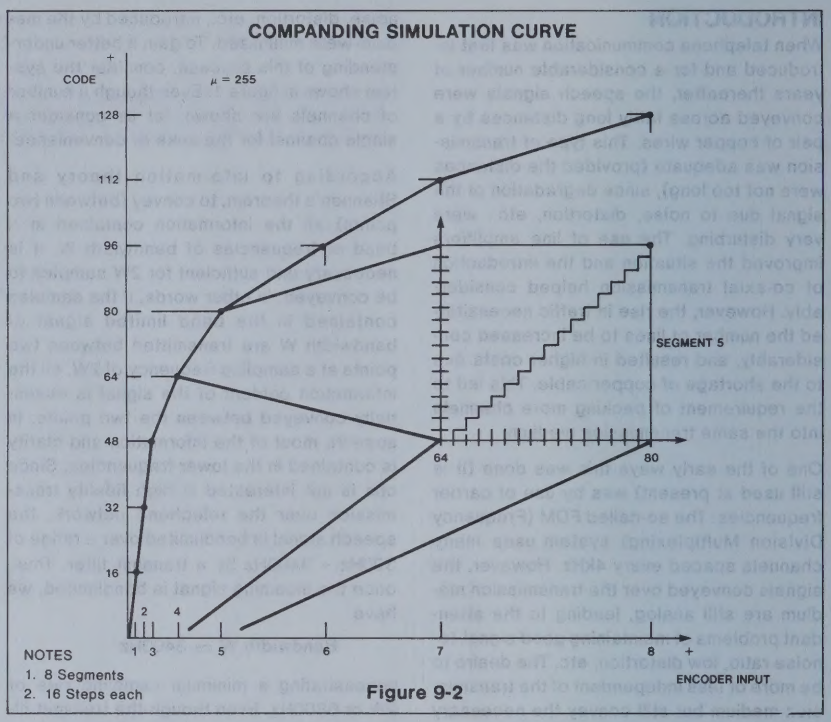


Figure 9-2

Repeaters

The output of the codec, which is a digital stream, is what is transmitted over the transmission line. The actual transmission is in the form of a binary signal. Due to line losses, etc., the pulse shape may get distorted. If the signal levels are very adversely affected so that they are below the triggering threshold at the receiving end, distortion may be introduced due to absent bits. To counter this, repeaters spaced 6000 feet apart are provided along the transmission line. These reshape the pulses so that those present at the receiving end are a faithful reproduction of those sent from the transmitting end.

Zero Code Suppression

The transmit clock allows the data to be sent at a 1.544MHz rate. At the receiving end (or at a repeater) this data will have to be restructured. It is preferable to use the same clock as that which was available at the transmitting end for this; however, it is difficult to transmit the clock pulses. For this reason, at the receiving end (or at a repeater) the received data itself is used to regenerate the receive clock. This is accomplished at present by using a high Q coil, though a phase locked loop can be used for the same purpose (see App. Note). Whatever method is used, a long succession of zeros will make it extremely difficult to recover the clock. For this reason, no more than seven successive zeros in any single word are allowed to be transmitted. If there are seven successive zeros, then the seventh bit in the 8 bit word is suppressed and a 1 is inserted.

Decoding

The incoming data at the receiving end is clocked in at a 1.544MHz receive clock rate, which clock is derived from the incoming data stream. The codec decodes the data and feeds this into the analog demultiplexer. Based on the individual words, the appropriate S/H in each of the received 24 channels is activated. Thus, the S/H of any particular channel changes state depending on the incoming coded 8 bit word. This value is held until the next 8 bit word arrives. The output of the S/H is filtered by the receive filter so that the original analog signal is recovered.

Advantages/Disadvantages Of The Present System

The advantages of the system are:

1) More channels in a transmission line. Higher speeds will result in further increasing the channels that can be transmitted or received.
2) Digital transmission/reception leads to

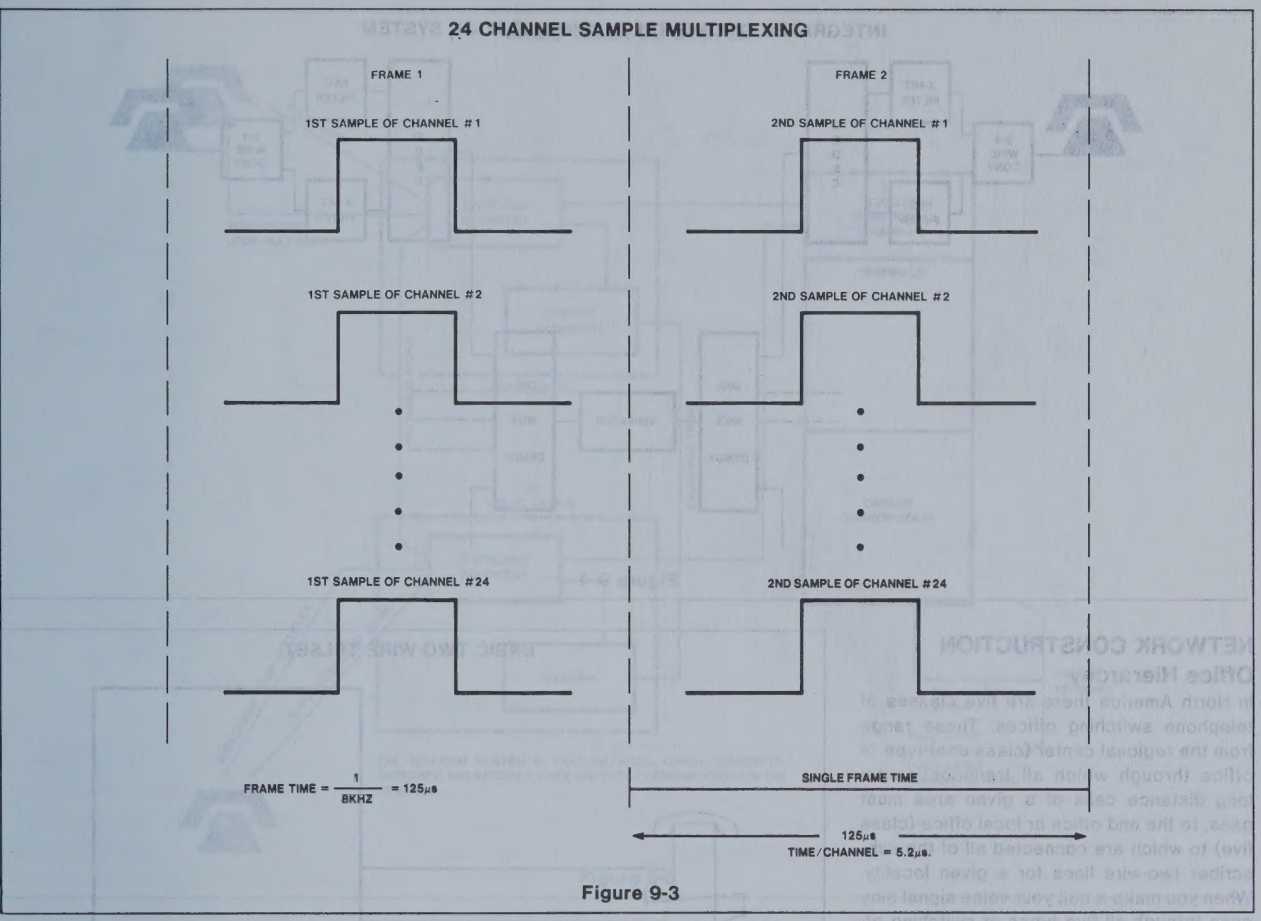


Figure 9-3

better quality due to the effects of noise being lessened.

3) Makes possible a completely digital Class V office so that all information is handled in digital form.

The disadvantages are:

1) Codec is too expensive. This has necessitated the sharing of the codec over 24 channels.
2) The analog nature of the PAM signal which has to be routed around still leads to noise problems.

The Proposed System Of The Future

If a codec were available that was cheap enough to be used in every line, obviously the analog multiplexer could be replaced by a digital multiplexer. Further routing around of the PAM signal could also be eliminated; this would lead to better performance. Such a system would appear as shown in figure 4. Thus, on a per channel basis, one would require a transmit filter, a receive filter, a codec, and a hybrid.

TELEPHONE OPERATION

Your home telephone is attached to the end of a pair of wires (called the subscriber 2 wire loop) which are connected to the local telephone switching office. When the telephone handset is on-hook, there is an open circuit on the 2 wire line that is attached to your phone. When you lift the handset from its cradle, the circuit is closed and a finite impedance appears across the subscriber 2 wire loop. The equipment in the switching office senses the loop current flowing due to this loop closure, (The switching office battery is connected to the 2 wire line in order to provide power to the phone handset) and transmits a dial tone to the handset.

At this point in time, the subscriber begins to dial the desired number. If he has a rotary dial type of handset the dialing (or signaling) information is transmitted by a series of pulses caused by the opening and closure of the dial contacts. If he has a push button type of telephone, the signaling information is transmitted by combinations of pairs of seven or eight tones. With either type of telephone the appropriate equipment in the switching office senses the dialing information and connects the incoming call to the desired telephone. If the desired telephone is also served by that same local office, the call is cross-connected within that office to the desired telephone's 2-wire loop. If the desired telephone belongs to an exchange not served by the caller's local office, the call is passed through to the local office to which the desired telephone is connected. Once this connection is made, the bell in the receiving telephone is rung using one of a number of methods. (One of the more common is called 20-cycle ringdown in which a 20Hz signal of about 100V amplitude is connected to the line to ring the phone.) When the receiving subscriber answers the phone, his loop is closed which turns off the 20Hz tone and completes the voice path through the phone system. When the conversation is completed and the handset is returned to its cradle, the loop opens up and the switch drops the cross-connection.

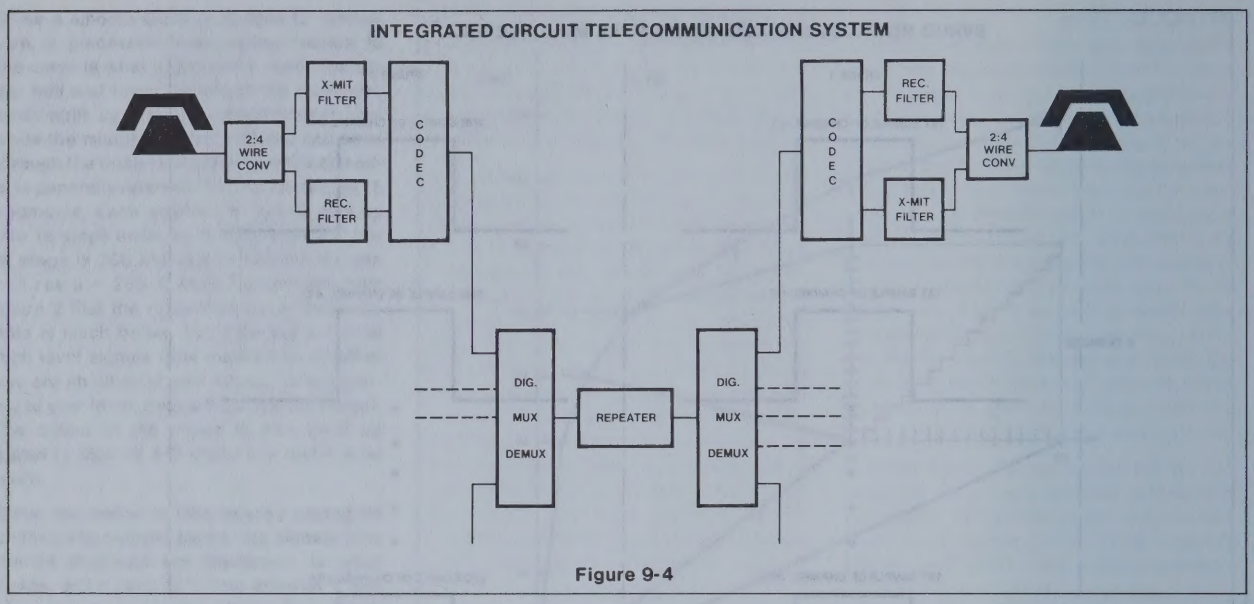


Figure 9-4

NETWORK CONSTRUCTION

Office Hierarchy

In North America there are five classes of telephone switching offices. These range from the regional center (class one) type of office through which all transcontinental long distance calls of a given area must pass, to the end office or local office (class five) to which are connected all of the subscriber two-wire lines for a given locality. When you make a call your voice signal may pass through all five types of switching office.

Between any two offices there are a given number of connecting circuits or trunks. Obviously, the number of trunk lines is less than the total number of handsets connected to each office since all of those telephones are not in use at once. Thus, these trunk lines are shared by many subscribers. When the demand for telephone service between two offices outstrips the capacity of the installed plant, two basic alternatives are available. One alternative is to install more cable pairs between the offices. The other alternative is to utilize more efficiently the capacity of the already installed plant through some form of multiplexing. There are a number of trade-offs involved in making this decision, including the relative costs of the two approaches, the future anticipated growth in demand for service, and the time frame in which this new service is desired (consider the difference in the level of telephone service required in Plains, Ga., today as opposed to two years ago this time). Since a nominal voice channel is 4KHz wide, it is possible to stack a number of channels up in frequency using modulation techniques before the frequency limiting characteristics of the cable become apparent. This is called frequency division multiplexing (FDM). Until very recently (with the advent of MSI & LSI digital IC's), FDM was the predominant type of signal concentration technique. Recently, however, another form of signal concentration is growing. This is called time division multiplexing, TDM. In a TDM system the voice signal is sampled at an appropriate rate and this sample is converted into an 8-bit digital word. This 8-bit word is assigned a time slot and a number of channels are combined into a continuous bit stream. This sampling and converting are the functions performed by our ST100 codec. It also performs the corresponding digital to analog conversion in the receive direction of transmission. These same multiplexing techniques can be (and are) applied at every level of the US telephone network

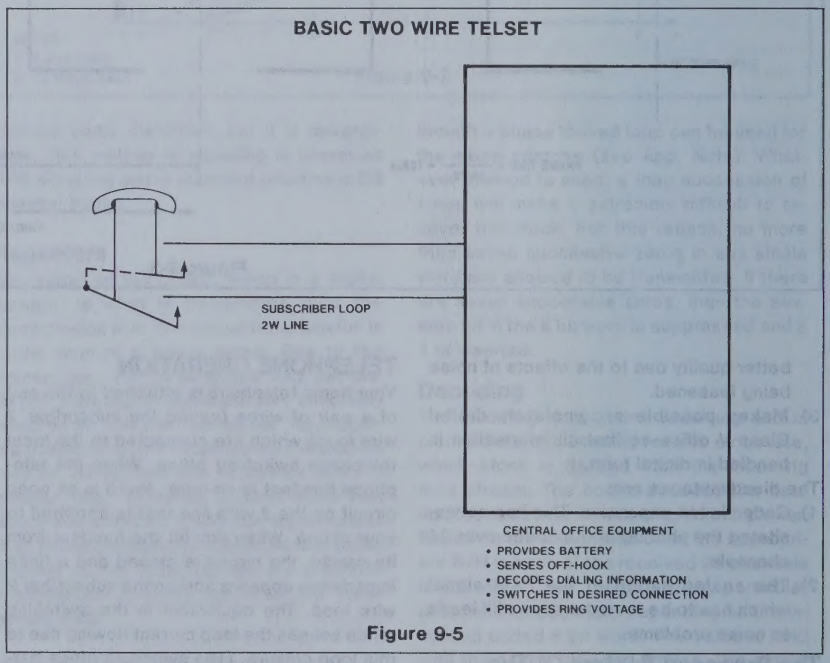


Figure 9-5

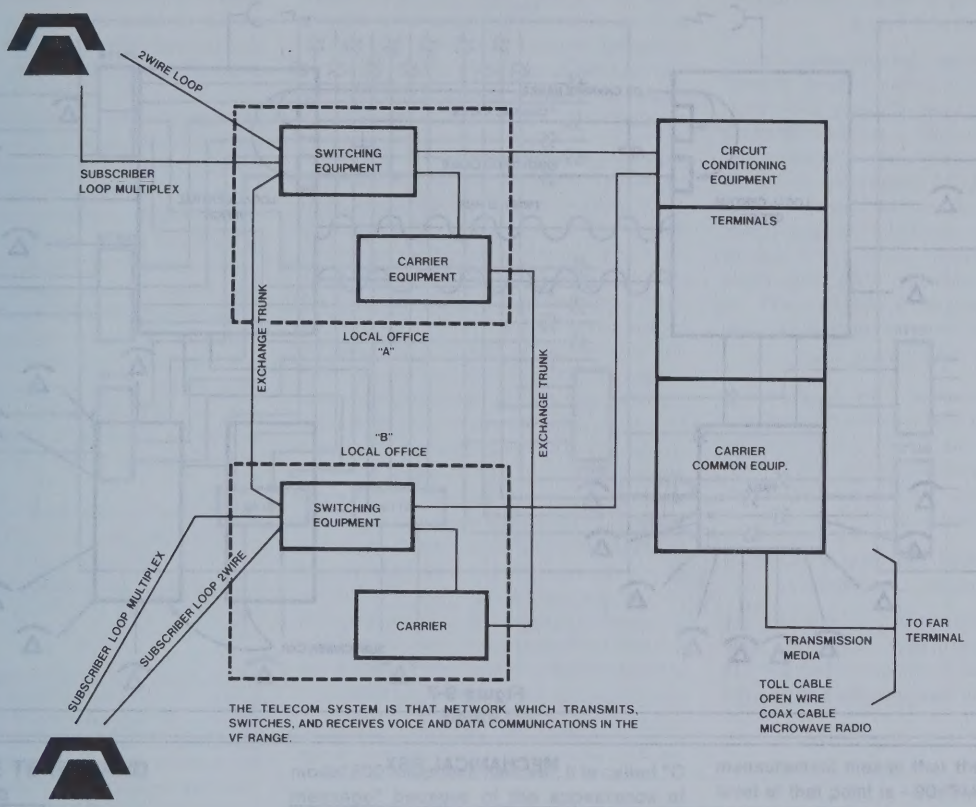


Figure 9-6

from the smallest local office in rural, wherever, to the long distance transcontinental heavy density transmission trunks.

A number of different types of transmission mediums are used. In local applications, twisted pair cable finds heavy use. For between-office trunks, coax cable can be found. The first installation of optical fiber cables are in this inter-office type of application. For long distance transmission, microwave radio and coax cable are employed. In all of these cases there are many instances where the installation of more circuits through the duplication of existing facilities can be avoided by more efficient use of the existing plant through multiplexing techniques. Increasingly, the form of multiplexing employed is TDM. It is for these applications that we have designed the ST100.

The reason TDM is taking over is that it is much more compatible with the new electronic switches and the TDM channel units are much cheaper than FDM ones. The new electronic switches are computer-controlled systems which can very easily process a digital voice signal such as the kind derived from a TDM multiplex. Since almost all new switches that are installed will be electronic ones, TDM equipment is replacing FDM as the type of multiplex to use.

Another area of application for the ST100 is the PBX market. PBX stands for private branch exchange. Basically, a PBX is a switching device that is used by a subscriber who requires more than one or two phones on his premises. It is his own private switching machine for calls within his plant. The newest PBX's on the market are electronic, computer-controlled machines. They offer many features not available on the older mechanical machines due to their stored memory capabilities. Again, as in the case with the central office (C.O.) switches, a digital voice format is easier to handle and thus there is a need for our ST100 in this market as well.

A few words about PBX machines and C.O. switches are necessary here. The older mechanical versions of both of these types of machines switched on a 2-wire basis since stepper relays (the primary switching element) were capable of bi-directional transmission. However, the new electronic versions of these machines switch on a four wire basis since electronic devices can operate only in a uni-directional mode and must have two separate transmission paths. The implications of this system architecture change for our ST120 2W/4W hybrid are shocking.

With mechanical switches, the only time a 2W to 4W conversion had to occur was when it was necessary for the signal to be amplified between local offices. Thus, the 2W/4W hybrid was only needed on trunk circuits, not on the subscriber loop. The same situation existed on PBX's where all internal-to-the-plant circuits were 2W and the 2W/4W conversion occurred only on the few trunks from the plant-to-the-outside-world local office. Since the new electronic machines are 4W machines, every subscriber loop (that is every telephone handset) must have a 2W/4W hybrid to operate. This situation holds for PBX's and electronic switching machines. Our ST120 performs this 2W/4W conversion and is intended for use in both of these applications.

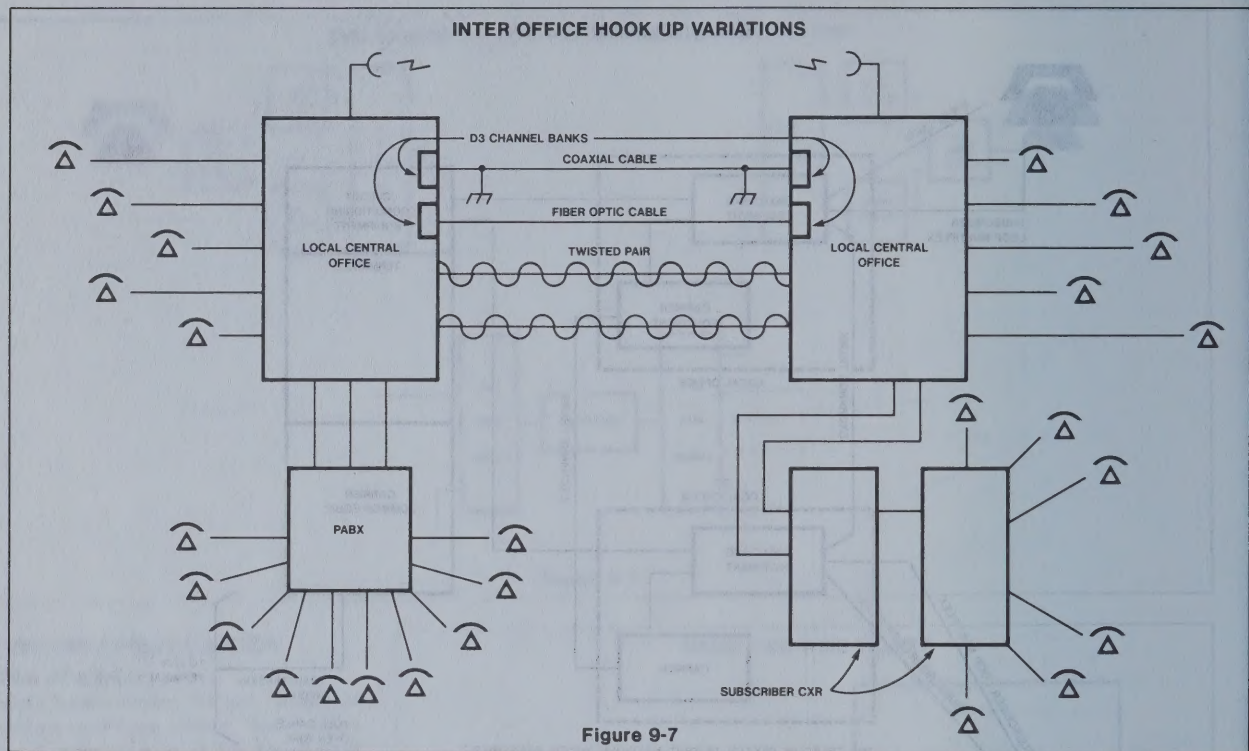


Figure 9-7

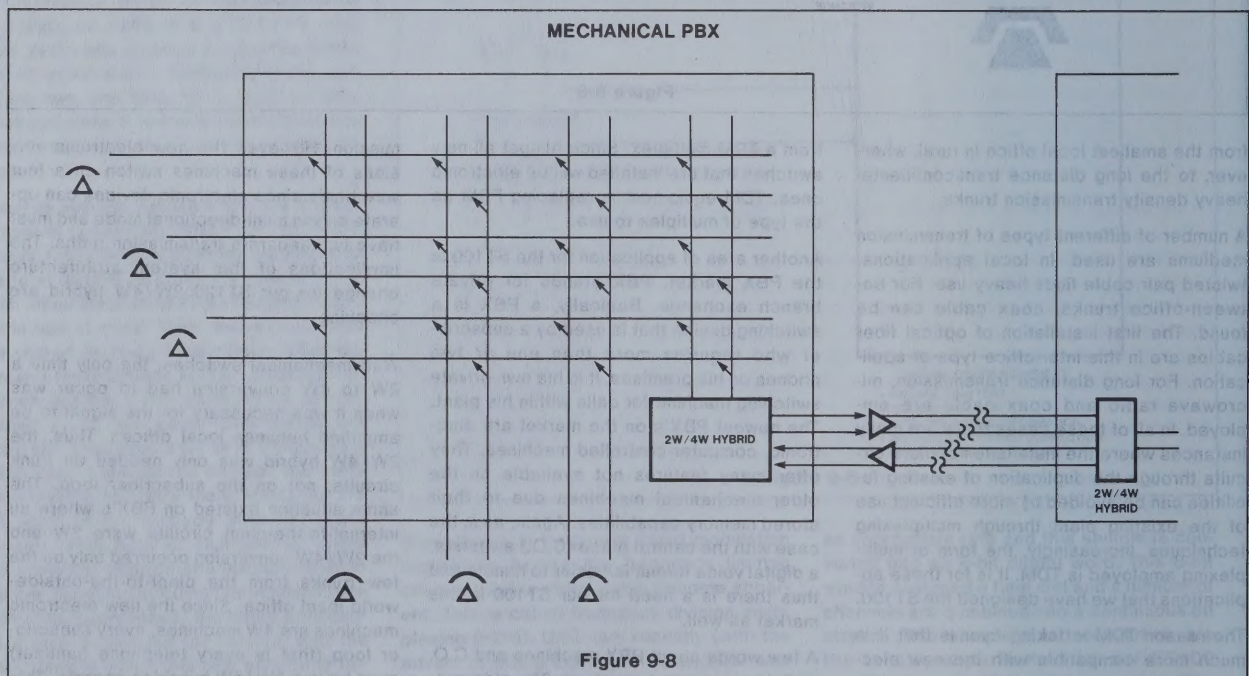


Figure 9-8

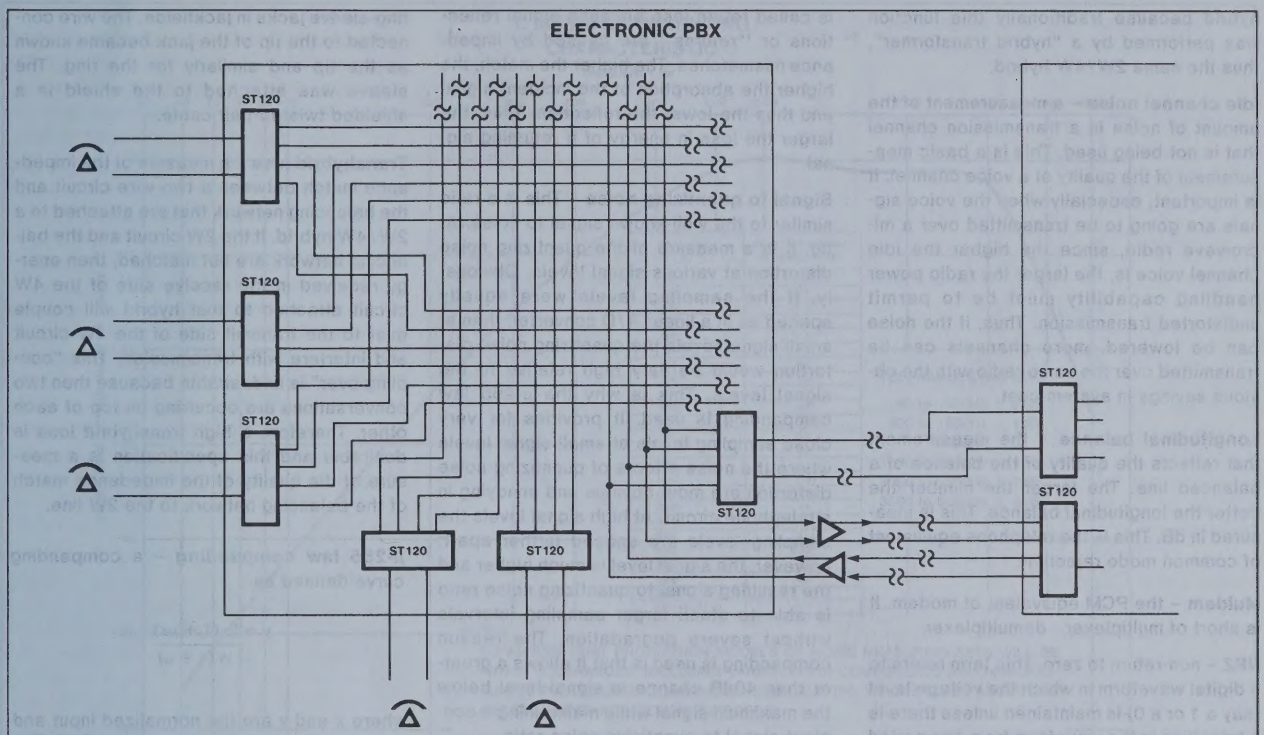


Figure 9-9

TELEPHONE TERMS AND DEFINITIONS

A-law companding - this is companding algorithm that is used in Europe instead of the μ-255 law that is the standard here. It is defined as

$$y = \frac{Ax}{(1 + \log A)}$$

where x and y are the normalized input and output of the compander and A = 87.6. A 13 segment approximation of the A-law curve is used in European equipment.

Balanced line or circuit - a circuit that consists of two wires over which the signal is transmitted in a differential mode. The word "balanced" comes from the fact that the capacitance from either side of the line to ground is theoretically equal on each of the two wires. The better the capacitive match (or balance) the less susceptible the circuit is to induced common mode signals. Thus, the line balance is analogous to the CMRR of op amps. Since there tends to be a lot of inductively induced noise and voltage spikes in central office environments due to mechanical switching equipment, a high level of circuit balance is required to minimize transient pickup.

C message filter - a test filter which approximates the frequency response of a model 500 telephone handset. It is called "C message" because of the appearance of the frequency response plot.

Codec - shortened form of coder - decoder.

Crosstalk - there are two principle types of crosstalk: interchannel and intrachannel. Interchannel crosstalk is a much less severe problem in PCM systems than it is in FDM systems and is one of the reasons PCM is cheaper and is, therefore, replacing FDM. Intrachannel crosstalk (transmit to receive and vice-versa) can be a problem if sufficent attention is not paid to proper grounding and separation of the analog transmit and receive sections of the circuit.

dBm - a power measurement. Zero dBm is defined as 1mW across a 600Ω load.

dBrn - a power measurement referenced to an arbitrary noise floor (rn meets reference noise). Zero dBrn is defined as - 90dBm and equals 1pW across 600Ω. Therefore 90dBrn equals 0dBm.

dBrnC - dBrn measurement taken through a C message filter.

dBrnCo - a relative dBrnC measurement referenced to the nominal level at the point where the measurement is taken. Thus, at a-10dBm nominal signal point, a 10 dBrnCO measurement means that the signal power level at that point is - 90dBM.

Echo - echo is the return of a talker's voice. If it is delayed a few milliseconds, it becomes very annoying to the speaker. It is usually caused by impedance mismatches in the circuit. The 2W/4W hybrid is one of the circuit elements most likely to cause this mismatch.

Frame - a full sequence of samples from each channel in the channel bank is called a frame. In North American applications there are 193 bits in a frame.

24 channels x 8 bits/channel
+ 1 frame bit = 193

The purpose of the frame bit is to tell the receiving terminal when each full sampling sequence starts.

Gain Tracking - this is a performance specification that is made on an end-to-end basis that measures the accuracy with which the coding and decoding are performed. This is a measure of how closely the signal amplitude that comes out on the receive end resembles that which was put in on the transmit side.

2W/4W Hybrid - a device used to convert a 2-wire circuit into a 4W circuit. It is called a

hybrid because traditionally this function was performed by a "hybrid transformer", thus the name 2W/4W hybrid.

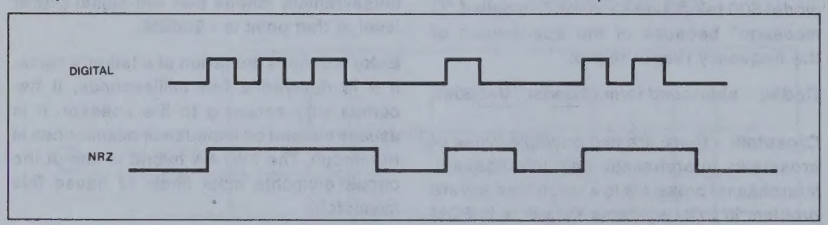
Idle channel noise - a measurement of the amount of noise in a transmission channel that is not being used. This is a basic measurement of the quality of a voice channel. It is important, especially when the voice signals are going to be transmitted over a microwave radio, since the higher the idle channel voice is, the larger the radio power handling capability must be to permit undistorted transmission. Thus, if the noise can be lowered, more channels can be transmitted over the same radio with the obvious savings in system cost.

Longitudinal balance - the measurement that reflects the quality of the balance of a balanced line. The larger the number the better the longitudinal balance. This is measured in dB. This is the telephone equivalent of common mode rejection.

Muldem - the PCM equivalent of modem. It is short of multiplexer - demultiplexer.

NRZ - non-return to zero. This term refers to a digital waveform in which the voltage level (say a 1 or a 0) is maintained unless there is a transition in the waveform from one period to the next.

Examples



Quantizing noise (Quantizing Noise Distortion) - quantizing noise occurs in the A to D conversion process due to the fact that discrete sampling levels are used in the conversion process. If the input signal amplitude falls in between the sampling levels, then the amount of the signal which is above the next lowest sampling level is truncated and gets "lost" in the conversion process. Upon decoding this "lost" signal level cannot be replaced and the resulting effect is a "hissing" type of "noise".

Return loss - A measure of the impedance match of a load to a line. It can be calculated as follows:

$$R_L = 20\ln\left(\frac{n+x}{n-x}\right)$$

where n is the characteristic impedance of the line and x is the impedance of the load. It is called return loss because signal reflections or '"returns"' are caused by impedance mismatches. The higher the match, the higher the absorption of the incident signal and thus the lower the reflection. Thus, the larger the loss in energy of a returning signal.

Signal to quantizing noise - This is a ratio similar to the well-known signal to noise ratio. It is a measure of the quantizing noise distortion at various signal levels. Obviously, if the sampling levels were equally spaced as in a linear A/D converter, then at small signal levels the quantizing noise distortion would be very high relative to the signal levels. This is why the μ-255 law companding is used. It provides for very close sampling levels at small signal levels where the noise effects of quantizing noise distortion are most obvious and annoying in a telephone circuit. At high signal levels the sampling levels are spaced further apart; however, the signal level is much higher and the resulting signal to quantizing noise ratio is able to stand larger sampling intervals without severe degradation. The reason companding is used is that it allows a greater than 40dB change in signal level below the maximum signal while maintaining a constant signal to quantizing noise ratio.

Singing - Singing is the result of sustained oscillations due to positive feedback in telephone amplifier or amplifying circuits. Circuits that sing are unusable. Singing may be thought of as echo that is completely out of control. This can occur at the frequency at which the circuit is resonant. Under such conditions the circuit losses at the singing frequency are so low that oscillation will continue even after the impulse that started it ceases to exist. The primary cause of echo and singing generally can be attributed to the mismatch between the balancing network and its two-wire connection associated with the subscriber loop.

Subscriber Loop - The circuit from the central office to the customer's telephone handset. Usually this is a 2-wire circuit with the subscriber (customer) telephone at the end of the loop.

Tip and ring - Two names for either side of a balanced line that arise from the use of tip-ring-sleeve jacks in jackfields. The wire connected to the tip of the jack became known as the tip and similarly for the ring. The sleeve was attached to the shield in a shielded twisted-pair cable.

Transhybrid loss - a measure of the impedance match between a two-wire circuit and the balancing network that are attached to a 2W/4W hybrid. If the 2W circuit and the balancing network are not matched, then energy received in the receive side of the 4W circuit attached to that hybrid will couple over to the transmit side of the 4W circuit and interfere with transmission. This "coupling over" is undesirable because then two conversations are occurring on top of each other. Therefore a high transhybrid loss is desirable and this specification is a measure of the quality of the impedance match of the balancing network to the 2W line.

μ-255 law companding - a companding curve defined as

$$y = \frac{\ln(1+\mu x)}{\ln(1+\mu)}$$

where x and y are the normalized input and output of the compander and $\mu = 255$. The purpose of this companding is to provide more resolution at low signal levels and thus improve the signal to quantizing noise ratio. The improvement in resolution allows an 8 bit companded A/D and D/A converter to offer performance equivalent to a 13 bit linear A/D and D/A converter. A 15 segment approximation to the μ-law curve is used in the ST100.

Zero Code Suppression - this is a phrase used to describe a circuit capability which senses the presence of an all zero output code on the transmit digital output and upon detection of such a condition inserts a "one" bit in the digital word before it is transmitted. Thus, there is at least one "one" bit in each transmitted digital word. This is necessary to be able to regenerate the clock frequency at the receiving terminal.

2W line - a balanced circuit consisting of 2 wires over which transmission occurs bi-directionally. These circuits are most frequently associated with the subscriber loop.

4W line - a circuit consisting of two balanced lines with one pair of wires dedicated to sending information and the other pair dedicated to receiving information. These uni-directional transmission paths are necessary because of the uni-directional gain characteristics of electronic amplification circuits and devices.

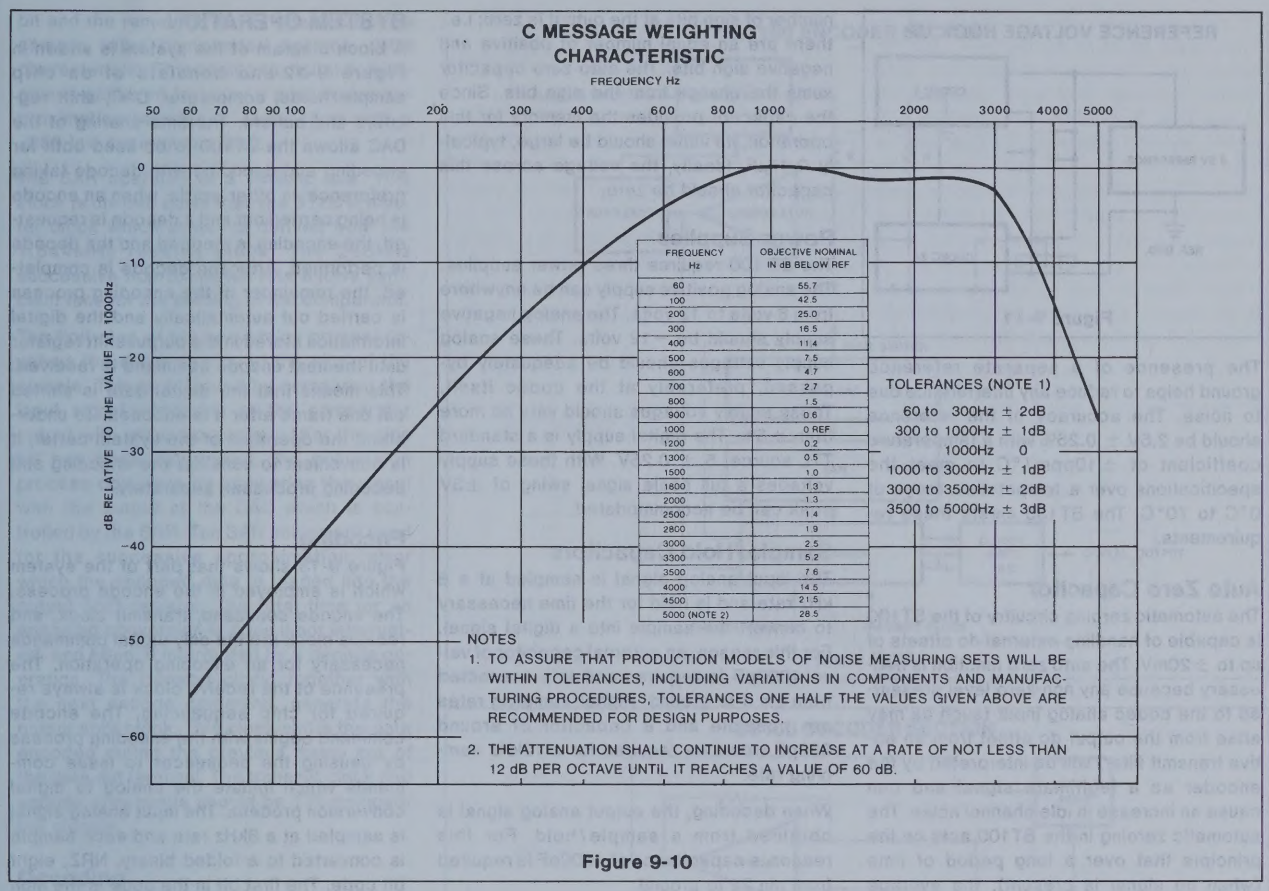

C MESSAGE WEIGHTING CHARACTERISTIC
FREQUENCY Hz
50 60 70 80 90 100 200 300 400 600 800 1000 2000 3000 4000 5000
0
-10
-20
-30
-40
-50
-60
dB RELATIVE TO THE VALUE AT 1000Hz
FREQUENCY Hz | OBJECTIVE NOMINAL IN dB BELOW REF
60 55.7
100 42.5
200 25.0
300 16.5
400 11.4
500 7.5
600 4.7
700 2.7
800 1.5
900 0.6
1000 0 REF
1200 0.2
1300 0.5
1500 1.0
1800 1.3
2000 1.3
2500 1.4
2800 1.9
3000 2.5
3300 5.2
3500 7.6
4000 14.5
4500 21.5
5000 (NOTE 2) 28.5
TOLERANCES (NOTE 1)
60 to 300Hz ± 2dB
300 to 1000Hz ± 1dB
1000Hz 0
1000 to 3000Hz ± 1dB
3000 to 3500Hz ± 2dB
3500 to 5000Hz ± 3dB
NOTES
1. TO ASSURE THAT PRODUCTION MODELS OF NOISE MEASURING SETS WILL BE WITHIN TOLERANCES, INCLUDING VARIATIONS IN COMPONENTS AND MANUFACTURING PROCEDURES, TOLERANCES ONE HALF THE VALUES GIVEN ABOVE ARE RECOMMENDED FOR DESIGN PURPOSES.
2. THE ATTENUATION SHALL CONTINUE TO INCREASE AT A RATE OF NOT LESS THAN 12 dB PER OCTAVE UNTIL IT REACHES A VALUE OF 60 dB.

Figure 9-10

THE ST100 CODEC: OPERATION & APPLICATION

DESCRIPTION

The ST100 is a single chip per channel codec in a 24 pin package which is built using I^2L technology. It is capable of both synchronous and asynchronous operation. Dual channel (A/B) signalling and zero code suppression are included for full D3 compatibility. The codec is time shared for encode and decode operations with the decode having precedence.

SYSTEM REQUIREMENTS

External Components

For its operation, the ST100 needs the following external components.

1) Transmit filter
2) Receive filter
3) +2.5V reference
4) Encode Sample/Hold capacitor
5) Decode Sample/Hold capacitor
6) Auto zero capacitor
7) Three power supplies (+8V to +12V, −12V and +5V)

In addition, the power supplies should be adequately bypassed, preferably at the codec package itself.

Transmit Filter

The transmit filter provides the necessary bandlimiting for the encode operation and should follow the standard D3 requirements. The input impedence of the codec is fixed at 15kΩ for convenience in designing the transmit filter. The analog input will accept a maximum signal swing of ±3V peak when a 2.5V reference is used with ±12V supplies.

Receive Filter

The output of the decoder is in the form of sampled and held pulses and has the familiar staircase pattern. For this reason, it is required that the receive filter have a response which is the inverse of the Sin x/x characteristic. The peaking required at 3000Hz is 2.1dB. *It is very essential that the receive filter have the response as shown in figure 9-17 since the performance, particularly frequency response and gain tracking, is very dependent upon the filter characteristic.* The analog output has an output impedence of about 10Ω and is capable of driving a full scale (±3V peak) signal across a 10KΩ load.

+2.5V Reference and Full Scale Signal Level

An external 2.5V source is the reference voltage required for proper operation of the codec. There is a direct relationship between the value of the reference and the permissible full scale input signal level. This relationship can be written as

$$FS \simeq 1.2V_{REF} = 3.0V \text{ pk when } V_{REF} = 2.5V \quad (1)$$

The current drawn from the 2.5V source is very small (about 1μA) since the reference voltage input of the ST100 is buffered. It is possible to run 24 channels from a single reference (such as the ST135) if such a configuration is desired.

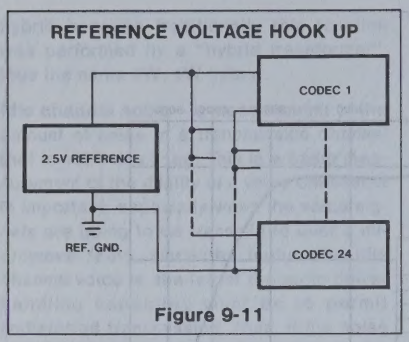


Figure 9-11

The presence of a separate reference ground helps to reduce any interference due to noise. The accuracy of the reference should be 2.5V ± 0.25% with a temperature coefficient of ±10ppm/°C to meet the specifications over a temperature range of 0°C to 70°C. The ST135 meets these requirements.

Auto Zero Capacitor

The automatic zeroing circuitry of the ST100 is capable of handling external dc offsets of up to ±20mV. The auto zero function is necessary because any non-zero level presented to the codec analog input (such as may arise from the output dc offset from an active transmit filter) will be interpreted by the encoder as a legitimate signal and can cause an increase in idle channel noise. The automatic zeroing in the ST100 acts on the principle that over a long period of time (when no signal is present), the average number of sign bits at the output is zero; i.e., there are an equal number of positive and negative sign bits. The auto zero capacitor sums the charge from the sign bits. Since the capacitor provides the memory for this operation, its value should be large, typically 0.47μF. Ideally, the voltage across this capacitor should be zero.

Power Supplies

The ST 100 requires three power supplies. The analog positive supply can be anywhere from 8 volts to 12 volts. The analog negative supply should be −12 volts. These analog supply voltages should be adequately bypassed, preferably at the codec itself. These supply voltages should vary no more than ±5%. The digital supply is a standard TTL source, 5 ± 0.25V. With these supply voltages a full scale signal swing of ±3V peak can be accommodated.

Sample/Hold Capacitors

The input analog signal is sampled at a 8 kHz rate and is held for the time necessary to convert the sample into a digital signal. For this reason, an external capacitor of value 1000pF is required and this connected from pin 4 to ground. Higher sampling rates are possible and a capacitor of around 600pF would be required for a 12kHz sampling rate.

When decoding, the output analog signal is obtained from a sample/hold. For this reason, a capacitance of 1000pF is required from pin 22 to ground.

SYSTEM OPERATION

A block diagram of the system is shown in Figure 9-12 and consists of on chip sample/holds, comparator, DAC, shift registers and buffers. The time sharing of the DAC allows the ST100 to be used both for encoding and decoding with decode taking preference. In other words, when an encode is being carried out and a decode is requested, the encoding is stopped and the decode is performed. After the decode is completed, the remainder of the encoding process is carried out automatically and the digital information stored in the output shift register until the next encode command is received. This means that the digital data is shifted out one frame after it is encoded. To understand the operation of the system better, it is convenient to consider the encoding and decoding processes separately.

Encoding

Figure 9-13 shows that part of the system which is employed in the encode process. The encode command, transmit clock, and receive clock are the only digital commands necessary for an encoding operation. The presence of the receive clock is always required for chip sequencing. The encode command begins with the encoding process by causing the sequencer to issue commands which initiate the analog to digital conversion process. The input analog signal is sampled at a 8kHz rate and each sample is converted to a folded binary, NRZ, eight bit code. The first bit in the code is the sign

BLOCK DIAGRAM

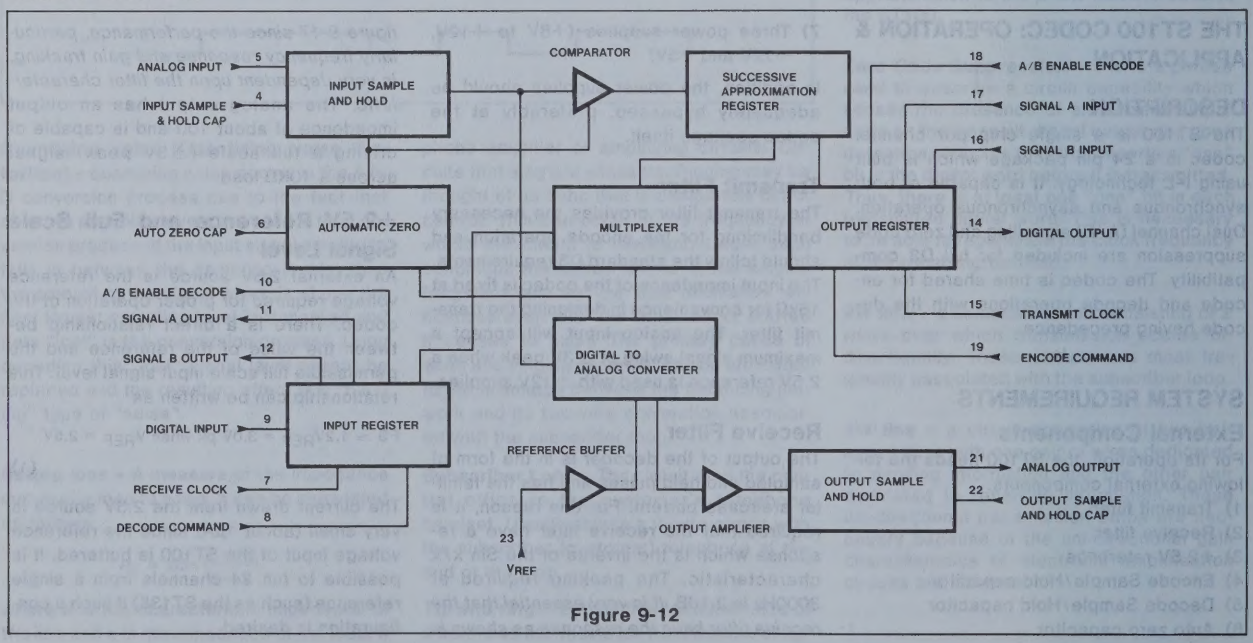


Figure 9-12

bit and the remaining seven bits decide the sample value companded per the μ255 characteristic. This analog to digital conversion is achieved by using a successive approximation register in conjunction with a μ255 law companding DAC.

The SAR operates at a 256kHz rate. This clock is divided down from the 512kHz master clock which in turn is derived from the 1.544MHz receive clock. The 256kHz successive approximation rate allows sufficient time for the settling of the comparator.

The first step of the conversion process involves the determination of the sign of the sample. This is achieved by comparing the input signal appearing at the comparator output with ground potential. After the sign bit has been determined, the conversion process continues by comparing the signal with the output of the DAC which is controlled by the SAR. Ten SAR pulses are used for the successive approximation, after which the encoded data is loaded into the output shift register. The total time for an encoding conversion is 40μs if not interrupted, and 56μs, if interrupted by a decode operation. The transmit clock, together with the next encode command, generate the output shift clock. This clock shifts the data encoded during the previous frame out of the data out terminal. The transmit clock and encode commands should be TTL compatible signals.

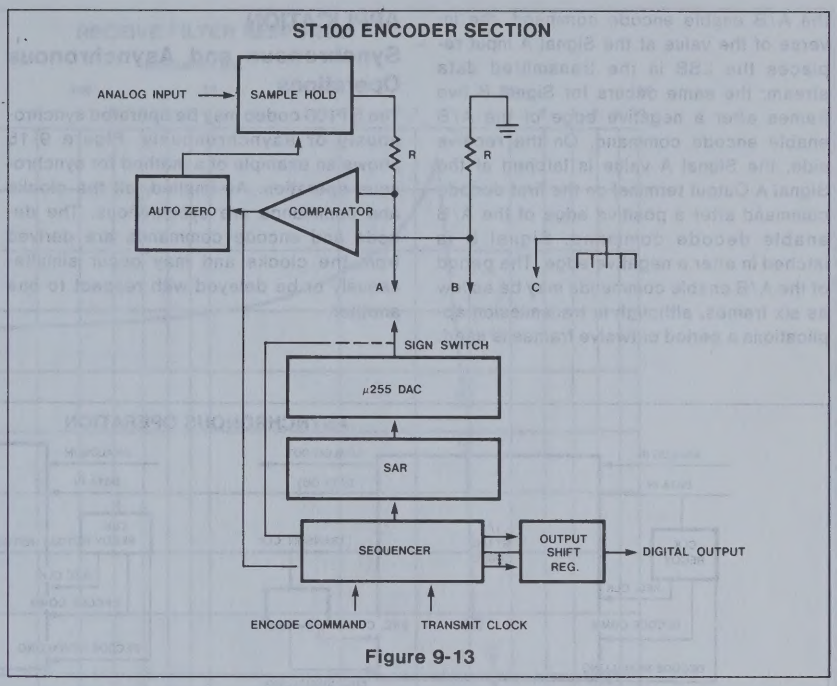


Figure 9-13

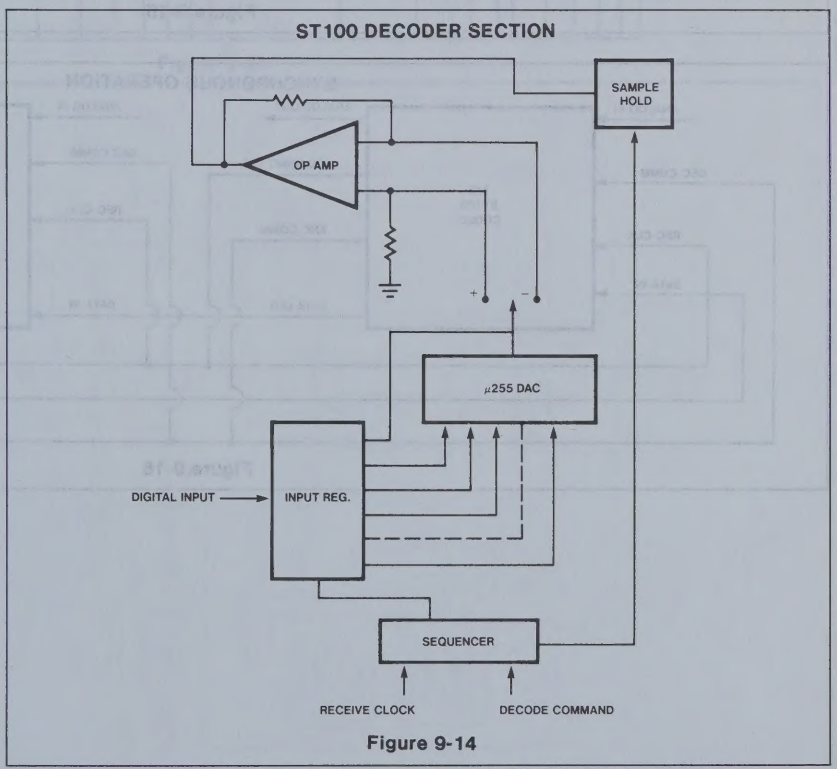


Figure 9-14

Decoding

Figure 9-14 shows the block diagram of the decode portion of the system. For a decode operation to begin, the only digital commands required are a decode command and the receive clock. The receive clock, in the presence of a decode command, generates an eight pulse shift clock which accepts the input data. (The shift clock is 90° out of phase with the receive clock allowing the data to be shifted in at the center of the bit). The decode command also results in a DAC request being generated, which begins the digital to analog conversion process. An internal timer allows 8μs after the DAC request for the data to be shifted in and for the DAC to settle. Then another 8μs is allowed for the digital to analog conversion. The digital data from the input shift register is applied in parallel form to the DAC. The conversion of the DAC output currents to voltage is done only by an op amp whose output drives a sample and hold which changes state depending upon the voltage applied. The receive clock and decode commands should be TTL compatible signals.

A/B Signalling

Circuitry is included on the chip which allows A/B signalling to be inserted into the data stream. To transmit the A/B signalling, the Signal A Input, Signal B Input and A/B Enable Encode inputs must be accessed. The Signal A Output, Signal B Output, and A/B Enable Decode terminals are used to recover the A/B signals at the receiving terminal. Two frames after the positive edge of

the A/B enable encode command, the inverse of the value at the Signal A Input replaces the LSB in the transmitted data stream; the same occurs for Signal B two frames after a negative edge of the A/B enable encode command. On the receive side, the Signal A value is latched at the Signal A Output terminal on the first decode command after a positive edge of the A/B enable decode command. Signal B is latched in after a negative edge. The period of the A/B enable commands may be as low as six frames, although in transmission applications a period of twelve frames is used.

APPLICATION

Synchronous and Asynchronous Operations

The ST100 codec may be operated synchronously or asynchronously. Figure 9-15 shows an example of a method for synchronous operation. As implied, all the clocks and commands are synchronous. The decode and encode commands are derived from the clocks and may occur simultaneously or be delayed with respect to one another.

Figure 9-16 shows a method for asynchronous operation. For a codec, the receive clock may be generated from the incoming data. The decode command and decode signalling enable command are in turn derived from the receive clock. Asynchronous with respect to the data in and receive clock, the transmit clock, together with the encode command, shift the encoded digital data out of the codec. This data, when received by another codec, generates a receive clock.

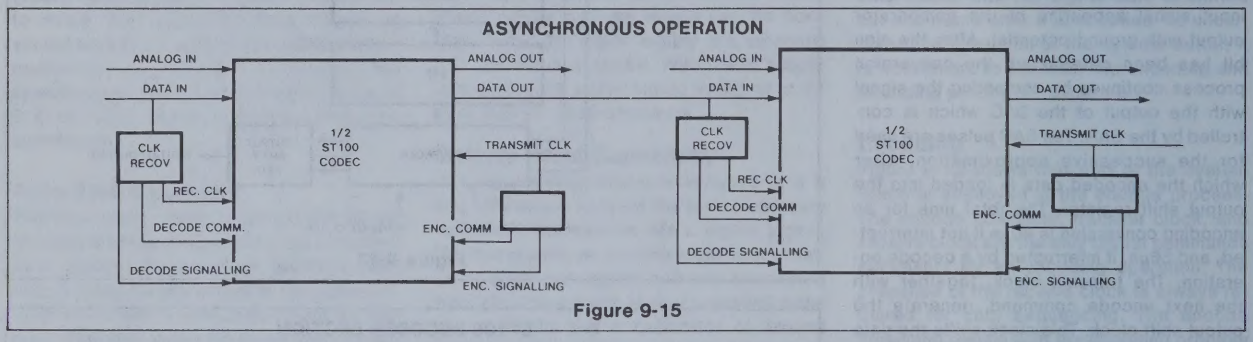


Figure 9-15

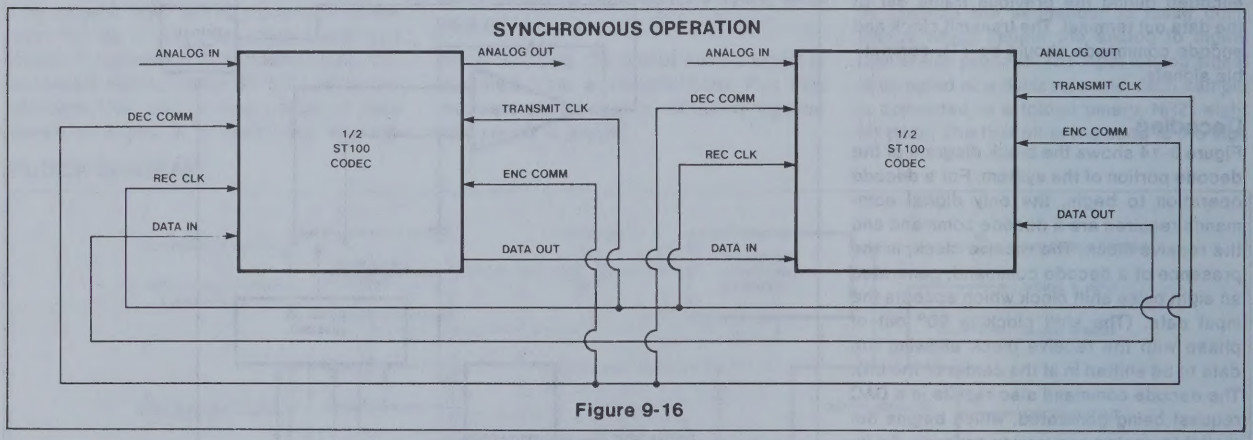


Figure 9-16

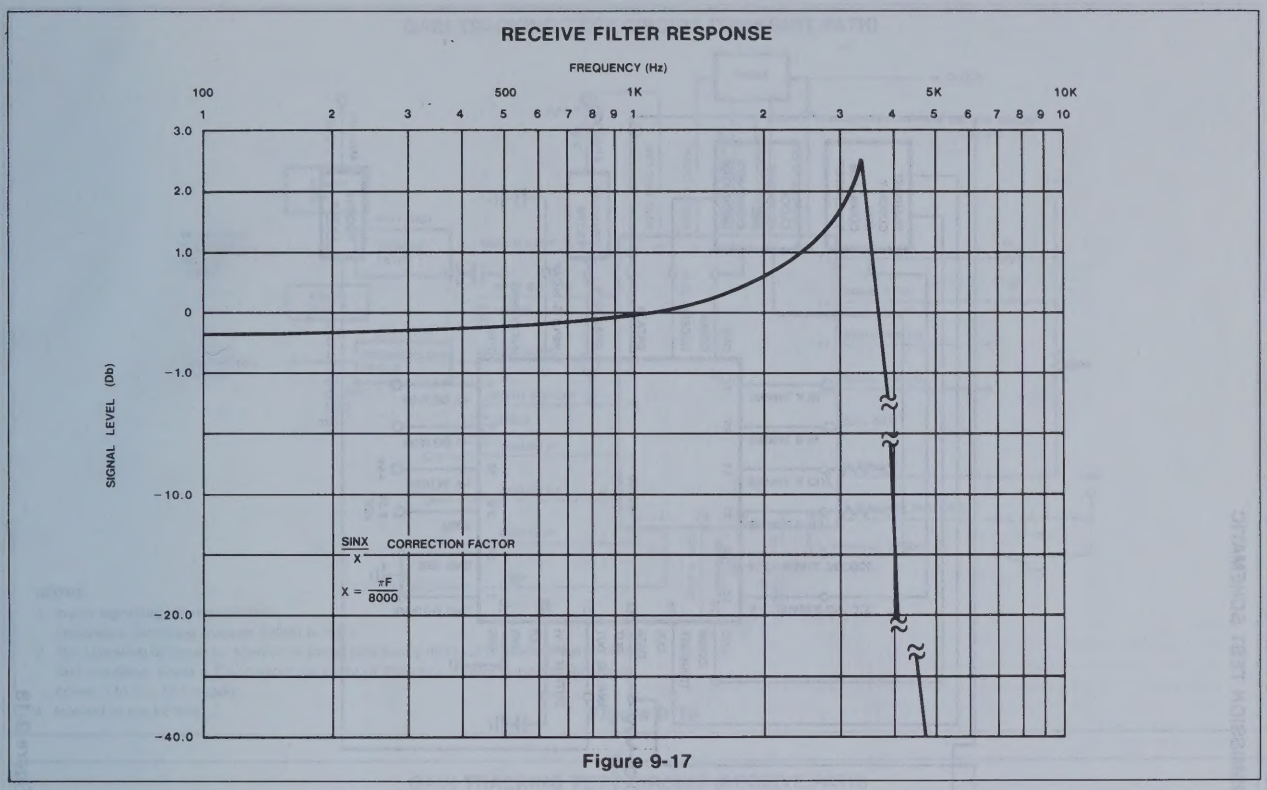

RECEIVE FILTER RESPONSE
FREQUENCY (Hz)
100
500
1K
5K
10K
1
2
3
4
5
6
7
8
9
1
2
3
4
5
6
7
8
9
10
3.0
2.0
1.0
0
-1.0
-10.0
-20.0
-40.0
SIGNAL LEVEL (Db)
SINX/X CORRECTION FACTOR
X = πF/8000

Figure 9-17

END-TO-END TRANSMISSION TEST SCHEMATIC

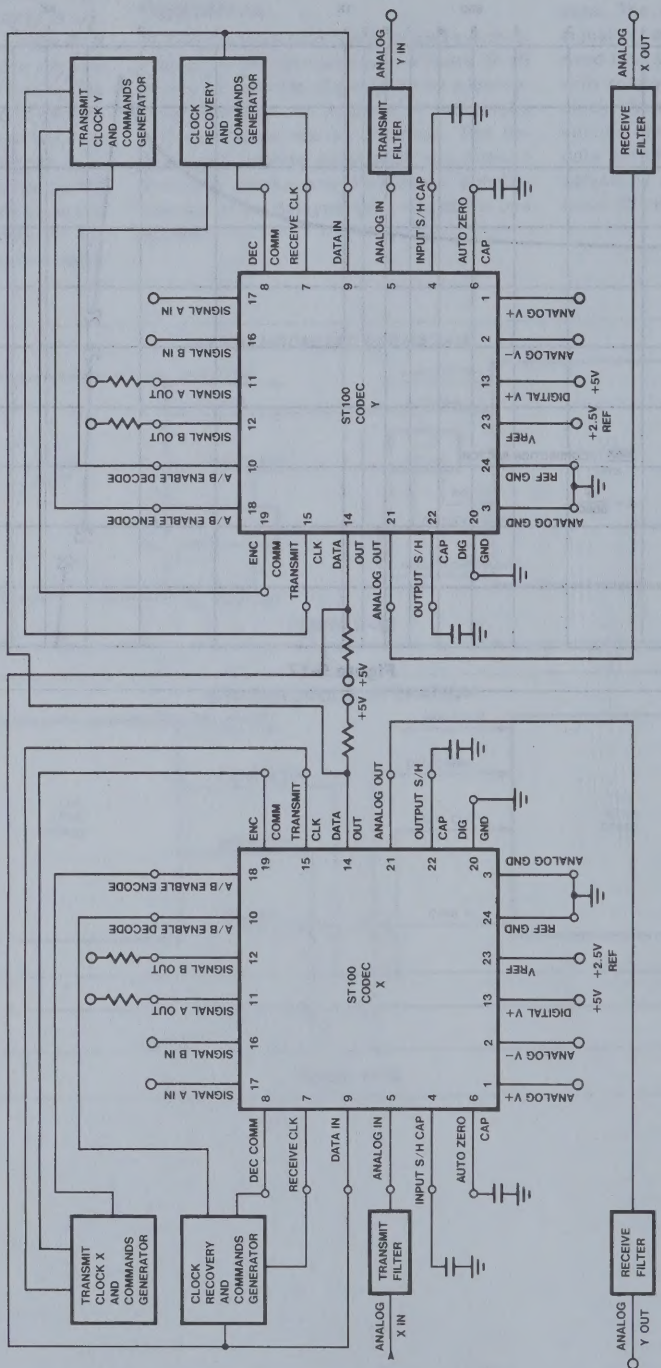
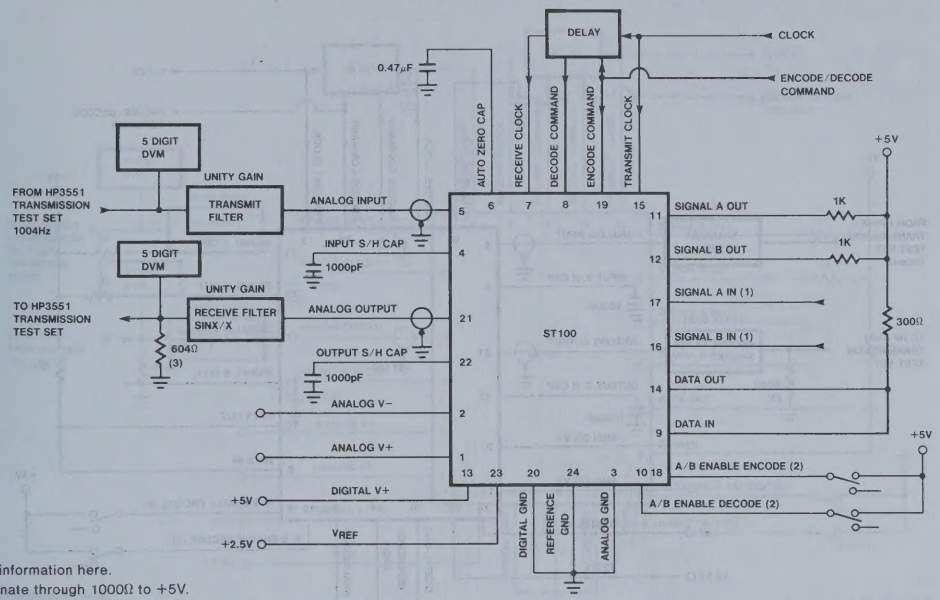


Figure 9-18

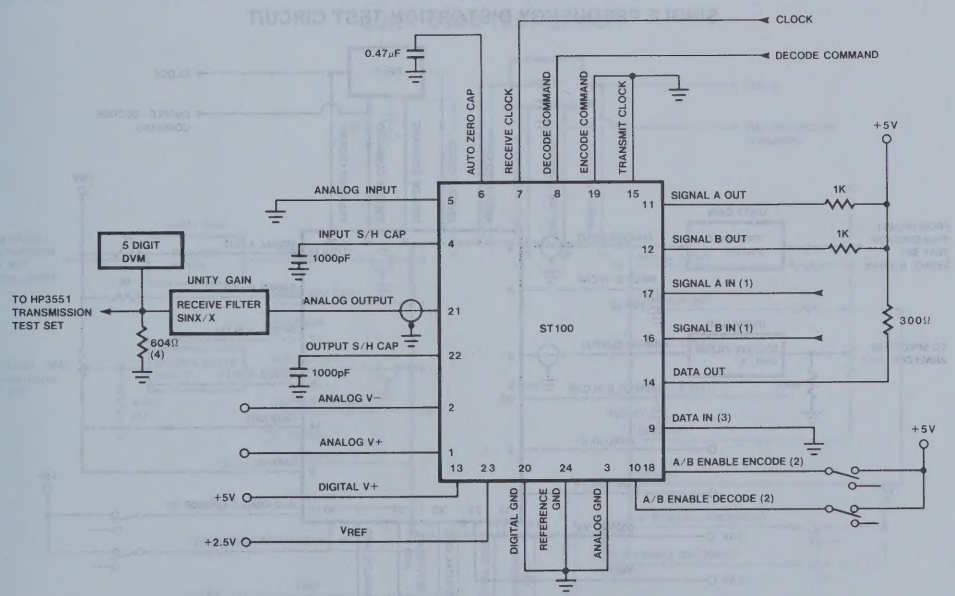
GAIN TRACKING TEST CIRCUIT (TRANSMIT PATH)



NOTES
1. Insert signalling information here.
   Otherwise, terminate through 1000Ω to +5V.
2. The signalling bits may be enabled at these pins during this test to obtain a worst case test condition. Apply a TTL compatible pulse of 250μs or greater duration. Otherwise connect to the +5V supply.
3. Internal to the HP3551.

Figure 9-19

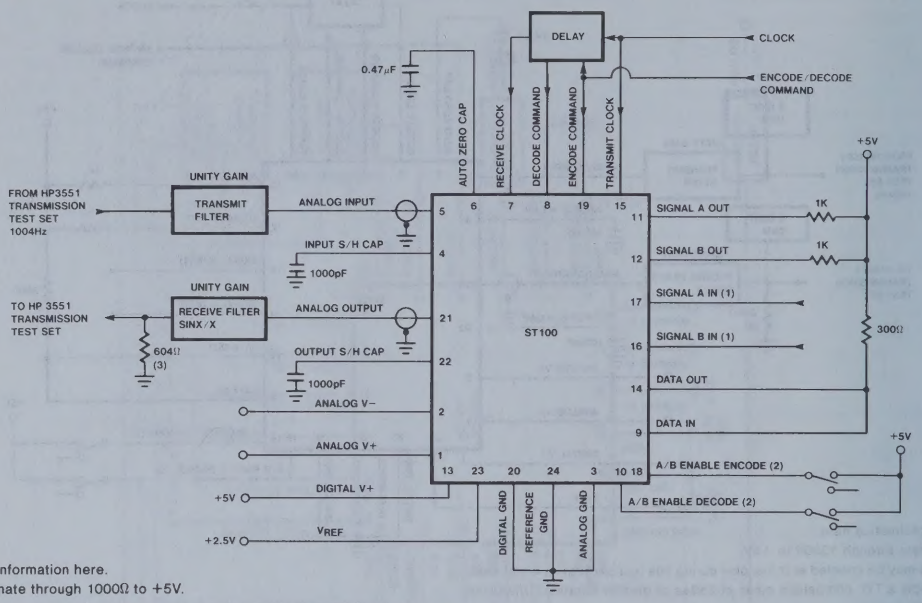
GAIN TRACKING TEST CIRCUIT (RECEIVE PATH)



NOTES
1. Insert signalling information here.
   Otherwise, terminate through 1000Ω to +5V.
2. The signalling bits may be enabled at these pins during this test to obtain a worst case test condition. Apply a TTL compatible pulse of 250μs or greater duration. Otherwise connect to the +5V supply.
3. Apply standard PCM word for a digital milliwatt.
4. Internal to the HP3551.

Figure 9-20

QUANTIZING DISTORTION TEST CIRCUIT

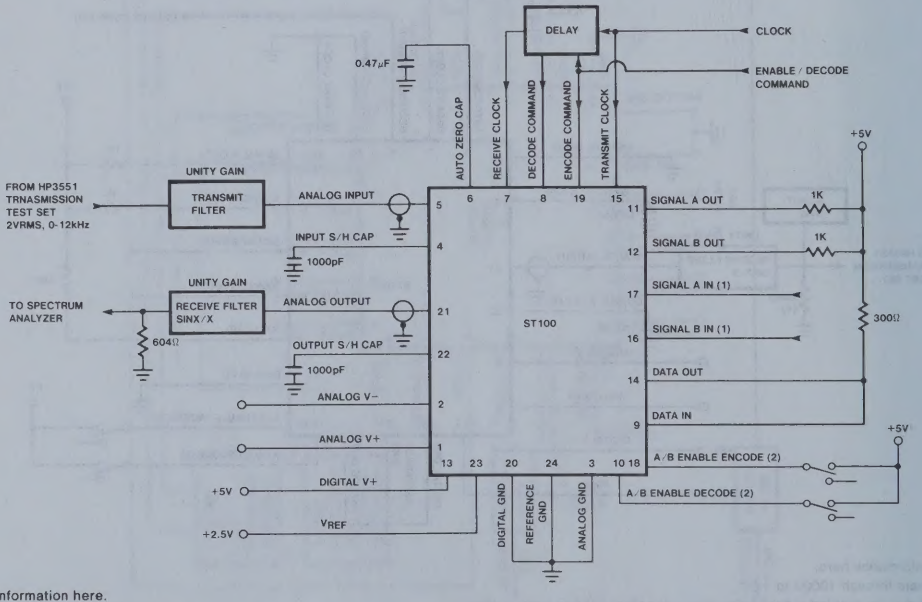


NOTES

1. Insert signalling information here.
   Otherwise, terminate through 1000Ω to +5V.
2. The signalling bits may be enabled at these pins during this test to obtain a worst case test condition. Apply a TTL compatible pulse of 250μs or greater duration. Otherwise connect to the +5V supply.
3. Internal to the HP3551.

Figure 9-21

SINGLE FREQUENCY DISTORTION TEST CIRCUIT

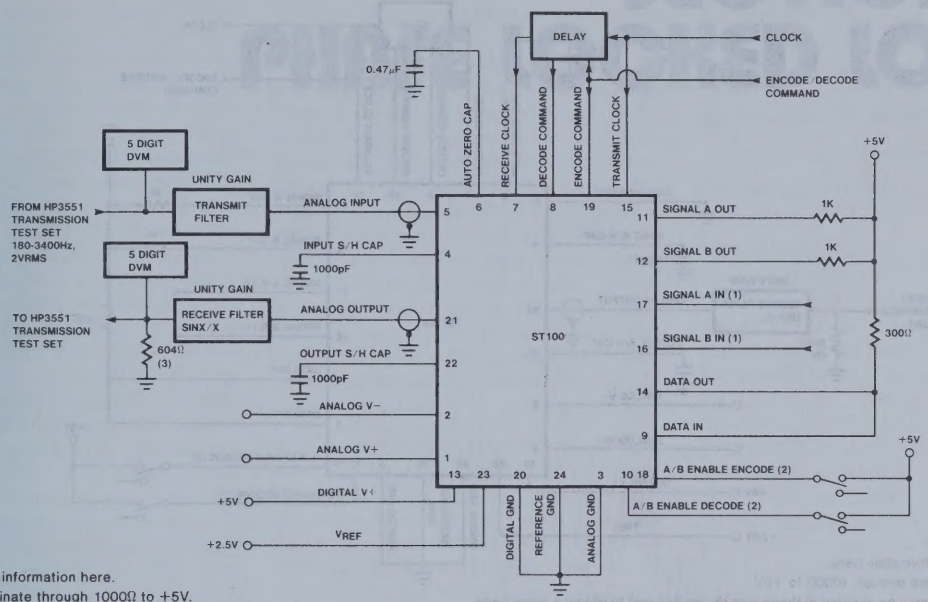


NOTES

1. Insert signalling information here.
   Otherwise, terminate through 1000Ω to +5V.
2. The signalling bits may be enabled at these pins during this test to obtain a worst case test condition. Apply a TTL compatible pulse of 250μs or greater duration. Otherwise connect to the +5V supply.

Figure 9-22

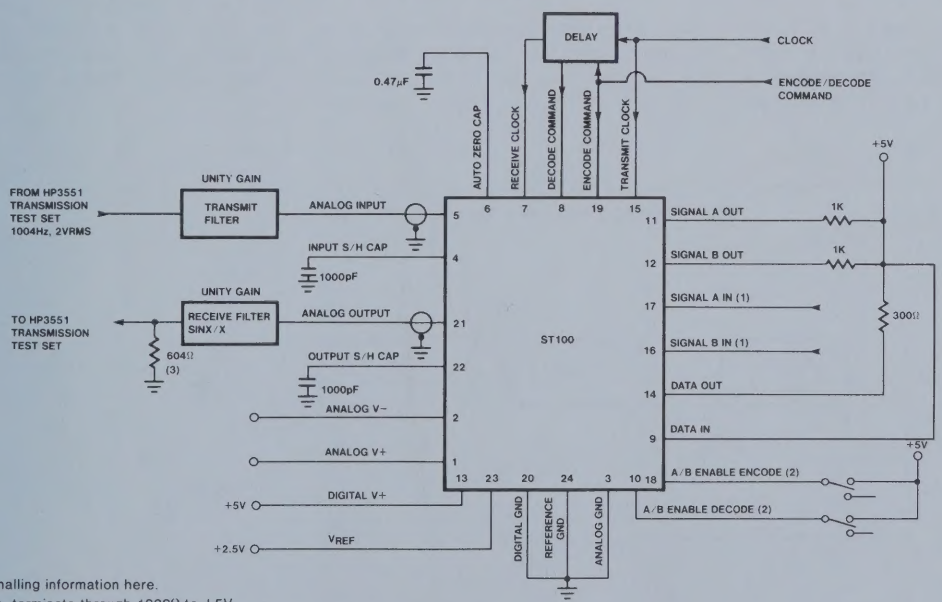
FREQUENCY RESPONSE TEST CIRCUIT



NOTES
1. Insert signalling information here.
   Otherwise, terminate through 1000Ω to +5V.
2. The signalling bits may be enabled at these pins during this test to obtain a worst case test condition. Apply a TTL compatible pulse of 250μs or greater duration. Otherwise connect to the +5V supply.
3. Internal to the HP3551.

Figure 9-23

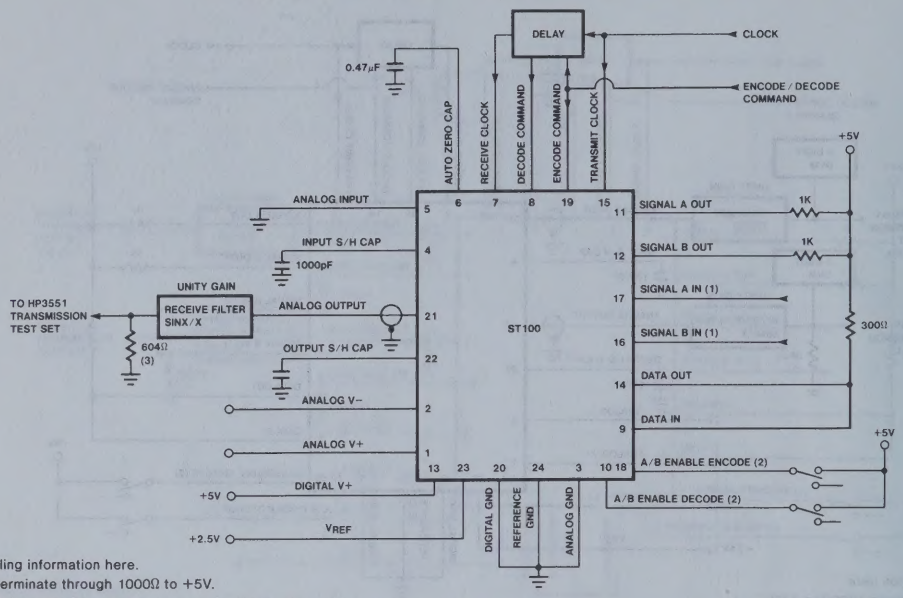
QUIET CODE TEST CIRCUIT



NOTES
1. Insert signalling information here.
   Otherwise, terminate through 1000Ω to +5V.
2. The signalling bits may be enabled at these pins during this test to obtain a worst case test condition. Apply a TTL compatible pulse of 250μs or greater duration. Otherwise connect to the +5V supply.
3. Internal to the HP3551.

Figure 9-24

IDLE CHANNEL NOISE TEST CIRCUIT

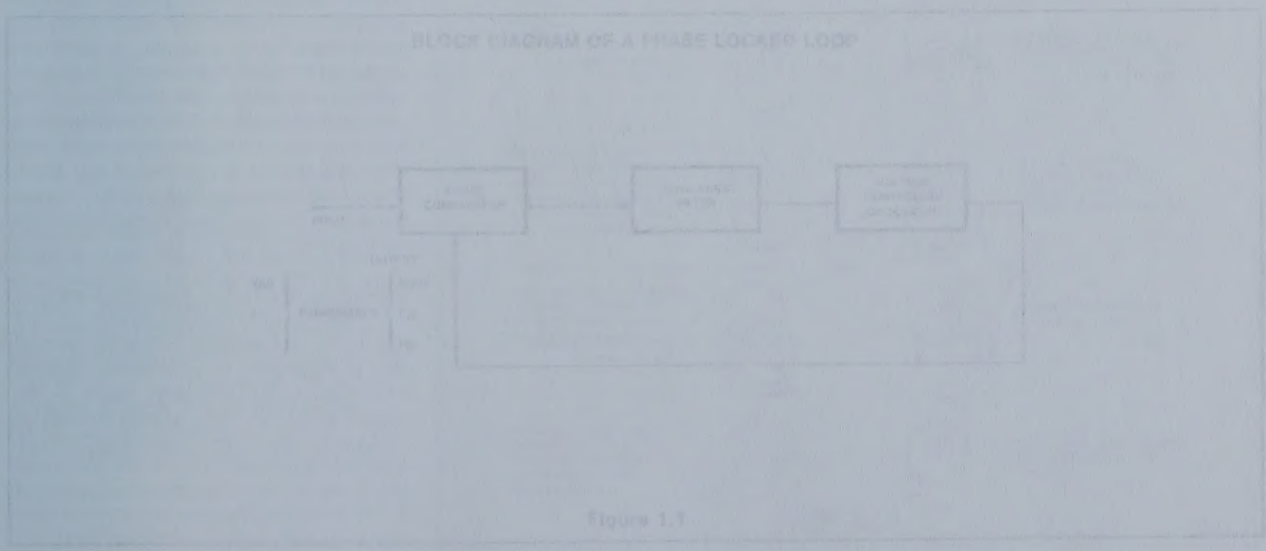


NOTES

1. Insert signalling information here. Otherwise, terminate through 1000Ω to +5V.
2. The signalling bits may be enabled at these pins during this test to obtain a worst case test condition. Apply a TTL compatible pulse of 250μs or greater duration. Otherwise connect to the +5V supply.
3. Internal to the HP3551.

Figure 9-25

SECTION 10
PHASE LOCKED LOOPS



10 MOTOR SPEED CONTROL CIRCUIT

INTRODUCTION

The basic phase locked loop (PLL) concept has been known and widely utilized since first being proposed in 1922 (1). Since that time PLLs have been used in instrumentation, space telemetry, and many other applications requiring a high degree of noise immunity and narrow bandwidth. Techniques and systems involved in these applications frequently are quite complex, requiring a high degree of sophistication. Many of the PLL applications have been at microwave frequencies and employ complex phase shifters, signal splitters, modulation, and demodulation schemes such as biphase and quadraphase. Because of the high frequencies involved in microwave applications, most all components of these PLL systems are made from discrete as opposed to integrated circuits. However in other communication system applications such as FSK and FM and AM demodulation where frequencies are below approximately 100MHz, monolithic PLLs have found wide application because of their low cost versus high performance.

A block diagram representation of a PLL is shown in Figure 1.1. Phase locked loops operate by producing an oscillator frequency to match the frequency of an input signal, f_i. In this locked condition, any slight change in f_i first appears as a change in phase between f_i and the oscillator frequency. This phase shift then acts as an error signal to change the frequency of the local PLL oscillator to match f_i. The locking onto a phase relationship between f_i and the local oscillator accounts for the name phase locked loop.

A MECHANICAL ANALOG TO THE PLL

To better visualize the frequency and phase relationships in a PLL, consider the mechanical system shown in Figure 1.2 which is a dual to the electronic PLL. This mechanical system has two identical, heavy disks with two separate center shafts attached to each disk. Each shaft is presumed to be mounted on a bearing that allows each massive disk to be rotated in either direction when some external force is applied. The shafts are coupled together by a spring whose end points are fixed to each shaft. This spring can be twisted in either direction depending upon the relative positions of the shafts. The spring cannot "kink up" due to the shafts passing through the center of the spring.

Now suppose the sequence of events shown in Figure 1.3 occurs to the mechanical system. The disks are simply represented like clock faces with positional reference markers. Initially both disks are stationary in a neutral position. Then the left disk, or input, is advanced slowly clockwise through an angle Θ_1 from the neutral position. The right disk, or output, initially doesn't move as the spring begins to tighten. As the input continues to move and when it reaches Θ_2, the output disk just begins to turn and tracks the input with a positional phase shift error of

$$\Theta_e = \Theta_2. \qquad (1.1)$$

At any point in time with both disks slowly turning at the same speed, there will be some inherent phase error between the disks, or

$$\Theta_e = \Theta_3 - \Theta_4. \qquad (1.2)$$

This positional phase error in the mechanical system is analogous to the phase error in the electronic PLL. When the input disk coasts to a stop, the output also gradually comes to a stop with a fixed phase error equal to that in Equation 1.2, or

$$\Theta_e = \Theta_5 - \Theta_6 = \Theta_3 - \Theta_4. \qquad (1.3)$$

The spring has a residual stored twist in one direction due to Θ_e.

Now consider that the disks are first returned to their neutral positions. Then the input disk is instantaneously rotated through an angle of Θ_1 as shown in Figure 1.4. The output disk can't respond instantaneously because of its large mass. It doesn't move instantaneously and the spring develops considerable torque. Then as shown in the sequence of events in Figure 1.4, the output disk begins accelerating after some delay due to the large phase error. It swings past the stopped position of the input disk due to its momentum, reaches a peak overshoot, and gradually oscillates about Θ_1 with a damped response, finally coming to rest with some small residual phase error. The input twist of Θ_1 represents the application of a step of position or phase to the system, and the response of the output disk is typical for a second-order, under-damped system. This same type of second-order behavior occurs in the PLL system for an instantaneous change of input phase.

As a final example, consider the events in Figure 1.5 where both disks are rotating at a constant rate. Applying a strobing light (strobotac) simultaneously to both disks

BLOCK DIAGRAM OF A PHASE LOCKED LOOP

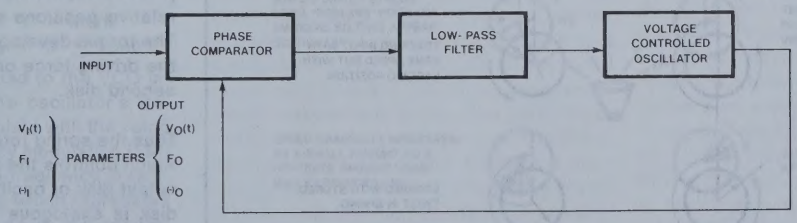


Figure 1.1

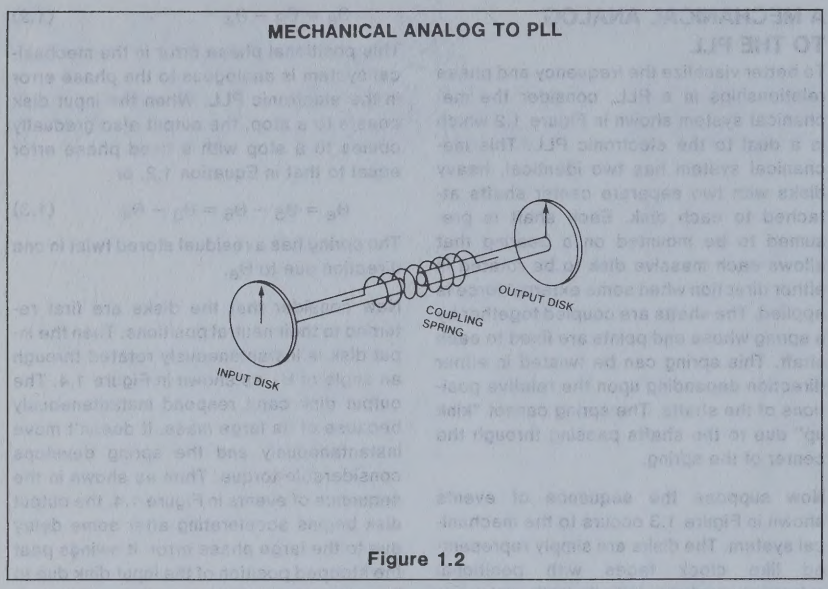


Figure 1.2

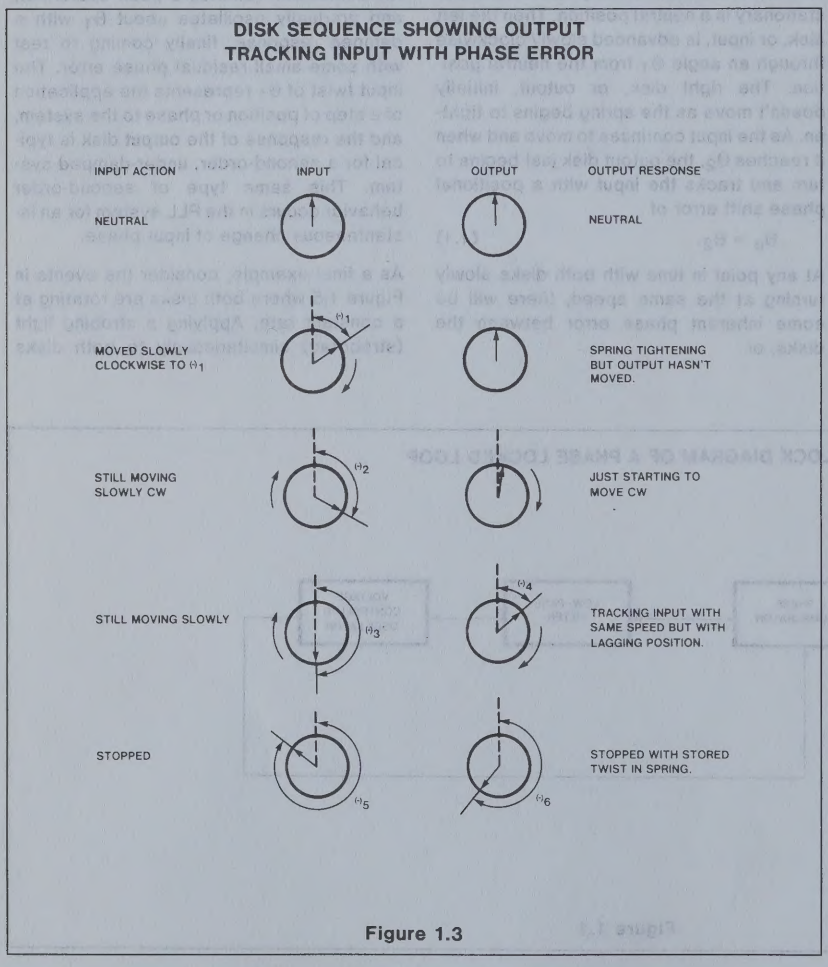


Figure 1.3

and adjusting its flashing rate to one flash per disk rotation will cause the positional markers to appear stationary. There will be a constant phase error in this case just as there was in Figure 1.3. Now suppose the revolution rate of the input disk gradually increases by a small amount to a new rate. The positional marker will appear to walk around the disk. The output first senses the increased rate of the input through an increase in the phase error. Then, after some delay, the rate of the output gradually increases to track the input. Both positional markers appear to be walking around each disk at the same rate until the strobotac is adjusted for the higher input and output rate. Then the strobe light again freezes the markers, producing a phase error at this higher rate that is larger than before the input rate was increased. This gradual increase in the input rate to the mechanical system simulates a ramp change in the input frequency to the PLL system. The response to the output disk simulates the behavior of the oscillator in the PLL.

If the rate of the input disk is alternately increased and decreased by some small amount compared to the nominal revolution rate, the positional markers will appear to walk both clockwise and counter clockwise, momentarily appearing stationary when the strobing light rate equals the disk revolution rate. This "walking" represents a changing phase error which is occurring at the modulation rate. Thus the phase error can be thought of as a useable demodulated output signal.

The disk-spring mechanical system is a helpful analog for visualizing frequency, phase, transient, and steady-state responses in the electronic phase locked loop system. In this example, the positions of the disk marker and rotation rates are analogous to phase and frequency in the electronic PLL system. The spring acts as a phase comparator to constantly sense the relative positions or phases of the disks. The torque developed in this spring acts as the driving force or input signal to turn the second disk.

Thus the spring torque simulates a voltage which controls the rate or frequency of the output disk or oscillator. Hence the second disk is analogous to a voltage-controlled oscillator (VCO). The large mass of the disks together with their angular momentum slows down the systems response time and simulates a low-pass filter in the electronic PLL system. This describes the lagging of the VCO free-running frequency to the input signal in an analog phase locked loop.

EXAMPLES OF PLL APPLICATIONS

Now consider the action of the voltage controlled oscillator, phase comparator and low pass filter in the PLL. The VCO generates a signal that is periodic. Normally, the rate or frequency of the VCO is primarily determined by the value of a capacitance connected to this oscillator. This action of starting the VCO running by itself is analogous to disconnecting the spring from one of the shafts in the mechanical system and starting the output disk rotating at a constant rate through some external means such as a motor. In the PLL system this frequency is called the oscillator's *free running frequency,* (f_o'), because it occurs when the system is unlocked and there is no coupling between input and output frequencies. With the PLL, the VCO frequency can be shifted above and below f_o' by applying a voltage to the optional fine tune input.* This signal generator property is just one of the many uses of the PLL. Specifically with integrated circuit PLLs, frequency ranges from less than 1.0Hz to more than 50MHz can be produced just by selecting the right value of capacitance from a chart on the data sheet.

Selecting f_o' and then changing it by a control voltage makes the VCO well suited for converting digital data that is represented by two different voltage levels into two different frequencies. A "1" voltage level can be related to a frequency called a mark, and an "0" level to a frequency called a space. This technique called *frequency shift keying,* or (FSK), is typical of data being transmitted over telephone and radio links where it is impractical to use dc voltage level shifts. Essentially this is what a modem (modulator-demodulator) does as it converts data to tones to go out of the system into a transmission link. Then it reverses the process and converts received tones to "1"'s and "0"'s at the receiver for the system to use. Sometimes confusion arises because different names are used for the same thing. For example,

A shift up in frequency = "1" = Mark
A shift down in frequency = "0" = Space

If voice or music is applied to the VCO instead of digital data, the oscillator's frequency will move or modulate with the voice or music. This is frequency modulation (FM) and is simply moving the frequency in relation to some input voltage which represents intelligence. Of course as in the modem case the process has to be reversed and the PLL can do this also. The PLL is a complete working system that can be used to

*Some oscillators have frequencies controlled by an input current rather than a voltage and are referred to as current-controlled oscillators (CCO).

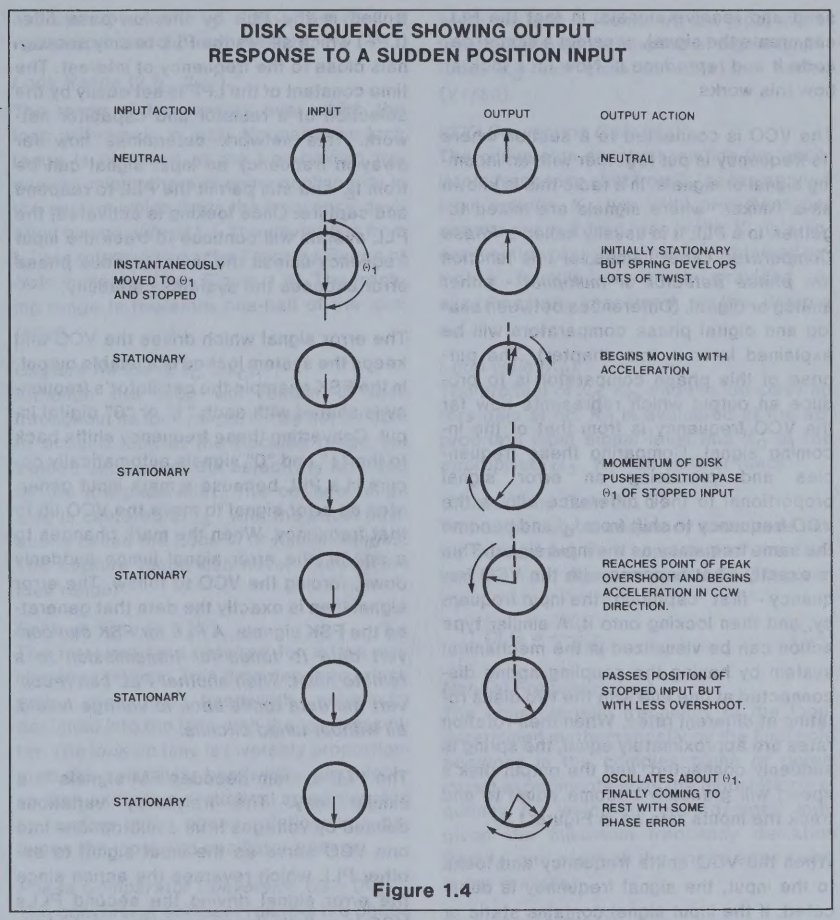

DISK SEQUENCE SHOWING OUTPUT
RESPONSE TO A SUDDEN POSITION INPUT
INPUT ACTION
INPUT
OUTPUT
OUTPUT ACTION
NEUTRAL
NEUTRAL
INSTANTANEOUSLY MOVED TO θ1 AND STOPPED
θ1
INITIALLY STATIONARY BUT SPRING DEVELOPS LOTS OF TWIST.
STATIONARY
BEGINS MOVING WITH ACCELERATION
STATIONARY
MOMENTUM OF DISK PUSHES POSITION PASE θ1 OF STOPPED INPUT
STATIONARY
REACHES POINT OF PEAK OVERSHOOT AND BEGINS ACCELERATION IN CCW DIRECTION.
STATIONARY
PASSES POSITION OF STOPPED INPUT BUT WITH LESS OVERSHOOT.
STATIONARY
OSCILLATES ABOUT θ1. FINALLY COMING TO REST WITH SOME PHASE ERROR

Figure 1.4

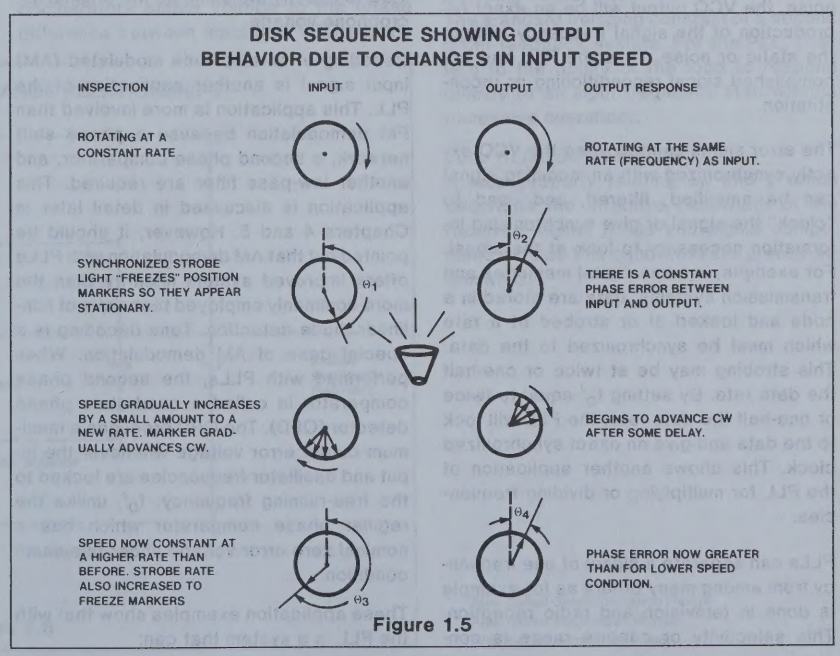

DISK SEQUENCE SHOWING OUTPUT
BEHAVIOR DUE TO CHANGES IN INPUT SPEED
INSPECTION
INPUT
OUTPUT
OUTPUT RESPONSE
ROTATING AT A CONSTANT RATE
ROTATING AT THE SAME RATE (FREQUENCY) AS INPUT.
θ2
SYNCHRONIZED STROBE LIGHT "FREEZES" POSITION MARKERS SO THEY APPEAR STATIONARY.
θ1
THERE IS A CONSTANT PHASE ERROR BETWEEN INPUT AND OUTPUT.
SPEED GRADUALLY INCREASES BY A SMALL AMOUNT TO A NEW RATE. MARKER GRADUALLY ADVANCES CW.
BEGINS TO ADVANCE CW AFTER SOME DELAY.
θ4
SPEED NOW CONSTANT AT A HIGHER RATE THAN BEFORE. STROBE RATE ALSO INCREASED TO FREEZE MARKERS
θ3
PHASE ERROR NOW GREATER THAN FOR LOWER SPEED CONDITION.

Figure 1.5

send and receive signals. In fact the PLL can create the signal, or select a signal, decode it and reproduce it. Now let's look at how this works.

The VCO is connected to a section where its frequency is put together with an incoming signal or signals. In a radio this is known as a "mixer" where signals are mixed together. In a PLL it is usually called a *Phase Comparator*. Other names for this function are *phase detector* or *multiplier* - either analog or digital. (Differences between analog and digital phase comparators will be explained later in this chapter). The purpose of this phase comparator is to produce an output which represents how far the VCO frequency is from that of the incoming signal. Comparing these frequencies and producing an error signal proportional to their difference allows the VCO frequency to shift from f_O' and become the same frequency as the input signal. This is exactly what happens with the VCO frequency - first "capturing" the input frequency, and then locking onto it. A similar type action can be visualized in the mechanical system by having the coupling spring disconnected at one end with the two disks rotating at different rates. When their rotation rates are approximately equal, the spring is suddenly connected, and the output disk's speed will gradually become equal to and track the inputs rate as in Figure 1.5.

When the VCO shifts frequency and locks to the input, the signal frequency is duplicated. If the input signal contains static or noise, the VCO output will be an exact reproduction of the signal frequency without the static or noise. Thus the PLL has accomplished signal reconditioning or reconstitution.

The error signal used to keep the VCO exactly synchronized with an incoming signal can be amplified, filtered, and used to "clock" the signal or give synchronizing information necessary to look at the signal. For example, in some digital memories and transmission systems, data are stored in a code and looked at or strobed at a rate which must be synchronized to the data. This strobing may be at twice or one-half the data rate. By setting f_O' equal to twice or one-half the data rate, the PLL will lock to the data and give an exact synchronized clock. This shows another application of the PLL for multiplying or dividing frequencies.

PLLs can separate a signal of one frequency from among many others as for example is done in television and radio reception. This selectivity or capture range is controlled in the PLL by the low-pass filter (LPF) which allows the PLL to only see signals close to the frequency of interest. The time constant of the LPF is set easily by the selection of a resistor and capacitor network. This network determines how far away in frequency an input signal can be from f_O' and still permit the PLL to respond and capture. Once locking is activated, the PLL system will continue to track the input frequency unless the instantaneous phase error exceeds the systems capability.

The error signal which drives the VCO and keeps the system locked is a usable output. In the FSK example the oscillator's frequency is shifted with each "1" or "0" digital input. Converting these frequency shifts back to the "1" and "0" signals automatically occurs in a PLL because a mark input generates an error signal to move the VCO up to that frequency. When the mark changes to a space, the error signal jumps suddenly down, forcing the VCO to follow. The error signal then is exactly the data that generated the FSK signals. *A PLL for FSK can convert data to tones for transmission to a remote point. Then another PLL can reconvert the data tones back to voltage levels, all without tuned circuits.*

The PLL system decodes FM signals in a similar way. The frequency variations caused by voltages from a microphone into one VCO serve as the input signal to another PLL which reverses the action since the error signal driving the second PLLs VCO is exactly the same as the original microphone voltage.

Decoding of an amplitude modulated (AM) input signal is another application of the PLL. This application is more involved than FM demodulation because a phase shift network, a second phase comparator, and another low-pass filter are required. This application is discussed in detail later in Chapters 4 and 5. However, it should be pointed out that AM demodulation with PLLs offers improved system linearity than the more commonly employed technique of nonlinear diode detection. Tone decoding is a special case of AM demodulation. When performed with PLLs, the second phase comparator is called a quadrature phase detector (QPD). The QPD produces a maximum output error voltage whenever the input and oscillator frequencies are locked to the free-running frequency, f_O', unlike the regular phase comparator which has a nominal zero error voltage under this same condition.

These application examples show that with the PLL is a system that can:

1 Generate a signal
2 Modulate a signal (encode)
3 Select a signal from among many
4 Demodulate (decode)
5 Recreate (reconstitute) a signal frequency with reduced noise
6 Multiply and divide frequency

TYPES OF PLLS

Generally speaking the monolithic PLLs can be classified into two groups - digital and analog. While both perform as PLLs, the digital circuits are more suitable for synchronization of digital signals, clock recovery from encoded digital data streams, and other digital applications. Analog monolithic PLLs are used quite extensively in communication systems since they maintain linear relationships between input and output quantities.

The phase comparator is perhaps the most important part of the PLL system since it is here that the input and VCO frequencies are simultaneously compared. Some digital PLLs employ a two-input Exclusive-Or gate as the phase comparator. When the digital loop is locked to f_O', there is an inherent phase error of 90° that is represented by asymmetry in the output waveform. Also the phase comparators output has a frequency component of twice the reference frequency. Because of the large logic voltage swings in digital systems, extensive filtering must be performed to remove the harmonic frequencies. For this reason, other types of digital phase comparators achieve locking by synchronizing the "edges" of the input and VCO frequency waveshapes. The phase comparator produces an error voltage that is proportional to the time difference between the edges, i.e., the phase error. This edge-triggering technique for the phase comparator produces lower output noise than with the Exclusive-Or approach. However time jitter on the input and VCO frequencies is translated into phase error jitter that may require additional filtering within the loop.

Triggering on the edges of digital signals means that only frequency (or period) is important and not duty cycle. This is a key consideration in PLL applications utilizing counters where waveshapes usually aren't symmetrical, i.e., 50% duty cycle. For the TTL family, it is easier to provide the edge matching function on the falling edges ("1" to "0") transition of the waveform. CMOS, I^2L, and ECL are better suited for leading edge triggering ("0" to "1").

Analog PLLs utilize a phase comparator which functions as a four-quadrant analog multiplier to mix the input and VCO signals. Since this mixing is true analog multiplica-

tion, the phase comparators output is a function of input and VCO signal amplitudes, frequencies, phase relationships, and duty cycles. The inherent linearity afforded by this analog multiplication makes the monolithic analog PLL well suited for many general purpose and communication system applications.

Another way of distinguishing between digital and analog phase comparators is by thinking of the similarities and differences between voltage comparators and operational amplifiers. Voltage comparators are specially designed for digital applications where response time between output levels has been minimized at the expense of system linearity. Feedback is seldom used to maintain linear system relationships, with the comparator normally running open loop. Op amps, on the other hand, are designed for a linear input-output relationship, with negative feedback being employed to further improve the system linearity.

PLL TERMINOLOGY

The following is a brief glossary of frequently encountered terms in PLL literature.

Free-running Frequency (f_o', ω_o').
Also called the *center frequency*, this is the frequency at which the loop VCO operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f_o and ω_o which are used for the general oscillator frequency. (Many references use f_o and ω_o for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context). The appropriate units for f_o' and ω_o' are Hz and radians per second respectively.

Lock Range ($2f_L$, $2\omega_L$).*
The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency unless there is some nonlinearity in the system which limits the frequency deviation on one side of f_o'. The deviations from f_o' are referred to as the *Tracking Range* or *Hold-in Range*. (See Figure 1.6). The tracking range is therefore one-half of the lock range.

Capture Range ($2f_c$, $2\omega_c$).**
Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The capture range also is centered at f_o' with the equal deviations called the *Lock-in* or *Pull-in Ranges*. The capture range can never exceed the lock range.

Lock-up Time (t_L).***
The transient time required for a free running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the low-pass filter. The lock-up time is inversely proportional to the selectivity bandwidth. Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

Phase Comparator Conversion Gain (K_d).
The conversion constant relating the phase comparators output voltage to the phase difference between input and VCO signals when the loop is locked. At low input signal levels, K_d is also a function of signal amplitude. K_d has units of volts per radian (V/rad).

VCO Conversion Gain (K_o).
The conversion constant relating the oscillators frequency shift from f_o' to the applied input voltage. K_o has units of radians per second per volt (rad/sec/volt). K_o is a linear function of ω_o' and must be obtained using a formula or graph provided or experimentally measured at the desired ω_o'.

Loop Gain (K_v)
The product of K_d, K_o, and the low-pass filters gain at dc. K_d is evaluated at the appropriate input signal level and K_o at the appropriate ω_o'. K_v has units of $(sec)^{-1}$.

Closed Loop Gain (CLG)
The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by

$$CLG = \frac{K_v}{1+K_v} \qquad (1.4)$$

Natural Frequency (ω_n).
The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f_o' and at which the phase error swing is the greatest.

Damping Factor (ζ).
The standard damping constant of a second order feedback system. For the PLL, ζ refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

Loop Noise Bandwidth (B_L).
A loop property relating ω_n and ζ which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

LOCK AND CAPTURE RANGE RELATIONSHIPS

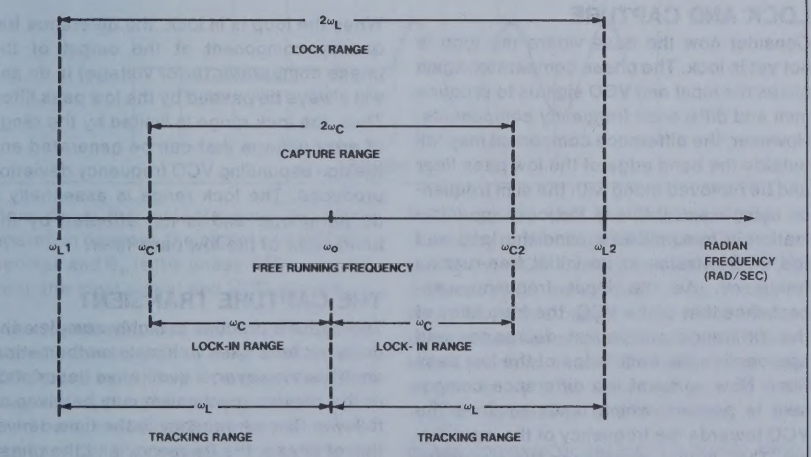


Figure 1.6

* Also called Synchronization Range.
** Also called Acquisition Range.
*** Also called Acquisition Time.

INTRODUCTION

The phase locked loop is a feedback system comprised of a phase comparator, a low pass filter and an error amplifier in the forward signal path and a voltage-controlled oscillator (VCO) in the feedback path. The block diagram of a basic PLL system is shown in Figure 2.1. Detailed analysis of the PLL as a feedback control system is discussed extensively in the literature (2-8). Perhaps the single most important point to realize when designing with the PLL is that it is a feedback system and, hence, is characterized mathematically by the same equations that apply to other, more conventional feedback systems. However, the parameters in the equations are somewhat different since the feedback error signal in the phase locked system is a phase rather than a current or voltage signal, as is usually the case in conventional feedback systems.

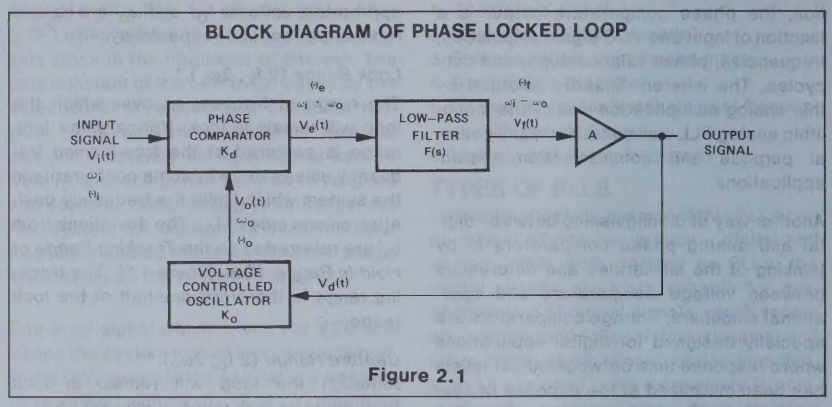


Figure 2.1

PHASE LOCKED LOOP OPERATION

The basic principle of the PLL operation can be briefly explained as follows:

With no signal input applied to the system, the VCO control voltage $V_d(t)$ is equal to zero. The VCO operates at a set frequency, f_o' (or the equivalent radian frequency ω_o') which is known as the free-running frequency. When an input signal is applied to the system, the phase comparator compares the phase and the frequency of the input with the VCO frequency and generates an error voltage $V_e(t)$ that is related to the phase and the frequency difference between the two signals. This error voltage is then filtered, amplified, and applied to the control terminal of the VCO. In this manner, the control voltage $V_d(t)$ forces the VCO frequency to vary in a direction that reduces the frequency difference between ω_o and the input signal. If the input frequency ω_i is sufficiently close to ω_o, the feedback nature of the PLL causes the VCO to synchronize or lock with the incoming signal. Once in lock, the VCO frequency is identical to the input signal except for a finite phase difference.

This net phase difference of Θ_e where

$$\Theta_e = \Theta_o - \Theta_i \qquad (2.1)$$

is necessary to generate the corrective error voltage V_d to shift the VCO frequency from its free-running value to the input signal frequency ω_i and, thus, keep the PLL in lock. This self-correcting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked. The range of frequencies over which the PLL can maintain lock with an input signal is defined as the "lock range" of the system. The band of frequencies over which the PLL can acquire lock with an incoming signal is known as the "capture range" of the system and is never greater than the lock range.

Another means of describing the operation of the PLL is to observe that the phase comparator is in actuality a multiplier circuit that mixes the input signal with the VCO signal. This mix produces the sum and difference frequencies $\omega_i \pm \omega_o$ shown in Figure 2.1. *When the loop is in lock,* the VCO duplicates the input frequency so that the difference frequency component $(\omega_i - \omega_o)$ is zero; *hence, the output of the phase comparator contains only a dc component.* The low pass filter removes the sum frequency component $(\omega_i + \omega_o)$ but passes the dc component which is then amplified and fed back to the VCO. Notice that when the loop is in lock, the difference frequency component is always dc, so the lock range is independent of the band edge of the low pass filter.

LOCK AND CAPTURE

Consider now the case where the loop is not yet in lock. The phase comparator again mixes the input and VCO signals to produce sum and difference frequency components. However, the difference component may fall outside the band edge of the low pass filter and be removed along with the sum frequency component. If this is the case, no information is transmitted around the loop and the VCO remains at its initial free-running frequency. As the input frequency approaches that of the VCO, the frequency of the difference component decreases and approaches the band edge of the low pass filter. Now some of the difference component is passed, which tends to drive the VCO towards the frequency of the input signal. This, in turn, decreases the frequency of the difference component and allows more information to be transmitted through the low pass filter to the VCO. This is essentially a positive feedback mechanism which causes the VCO to snap into lock with the input signal. With this mechanism in mind, the term "capture range" can again be defined as *the frequency range centered about the VCO initial free-running frequency over which the loop can acquire lock with the input signal.* The capture range is a measure of how close the input signal must be in frequency to that of the VCO to acquire lock. The "capture range" can assume any value within the lock range and depends primarily upon the band edge of the low pass filter together with the closed loop gain of the system. It is this signal capturing phenomenon which gives the loop its frequency selective properties.

It is important to distinguish the "capture range" from the "lock range" which can, again, be defined as *the frequency range usually centered about the VCO initial free-running frequency over which the loop can track the input signal once lock has been achieved.*

When the loop is in lock, the difference frequency component at the output of the phase comparator (error voltage) is dc and will always be passed by the low pass filter. Thus, the lock range is limited by the range of error voltage that can be generated and the corresponding VCO frequency deviation produced. The lock range is essentially a dc parameter and is not affected by the band edge of the low pass filter.

THE CAPTURE TRANSIENT

The capture process is highly complex and does not lend itself to simple mathematical analysis. However, a qualitative description of the capture mechanism may be given as follows. Since frequency is the time derivative of phase, the frequency and the phase errors in the loop can be related as

$$\Delta\omega = \frac{d\Theta_e}{dt} \qquad (2.2)$$

ASYNCHRONOUS ERROR BEAT FREQUENCY DURING THE CAPTURE PROCESS:

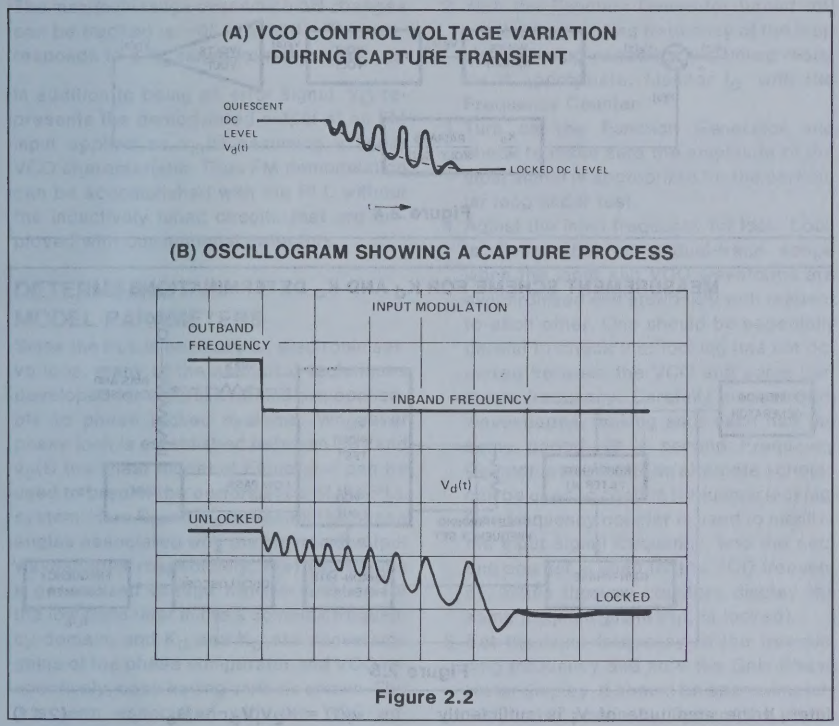


Figure 2.2

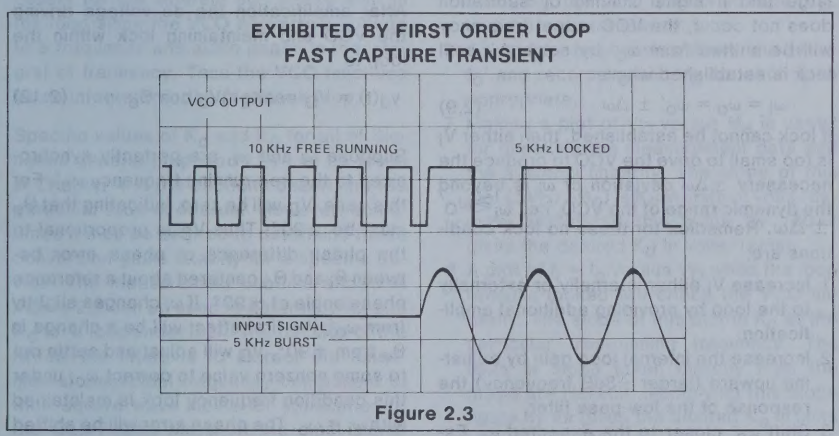

EXHIBITED BY FIRST ORDER LOOP FAST CAPTURE TRANSIENT
VCO OUTPUT
10 KHz FREE RUNNING
5 KHz LOCKED
INPUT SIGNAL 5 KHz BURST

Figure 2.3

where $\Delta\omega$ is the instantaneous frequency separation between the signal and VCO frequencies and Θ_e is the phase difference between the input signal and VCO signals.

If the feedback loop of the PLL were opened between the low pass filter and the VCO control input, then for a given condition of ω_o and ω_i the phase comparator output would be a sinusoidal beat note at a fixed frequency $\Delta\omega$. If ω_i and ω_o were sufficiently close in frequency, this beat note would appear at the filter output with negligible attenuation.

Now suppose that the feedback loop is closed by connecting the low pass filter output to the VCO control terminal. The VCO frequency will be modulated by the beat note. When this happens, $\Delta\omega$ itself will become a function of time. If during this modulation process, the VCO frequency moves closer to ω_i (i.e., decreasing $\Delta\omega$), then $\frac{d\Theta_e}{dt}$ decreases and the output of the phase comparator becomes a slowly varying function of time. Similarly, if the VCO is modulated away from ω_i, $\frac{d\Theta_e}{dt}$ increases and the error voltage becomes a rapidly varying function of time. Under this condition the beat note waveform no longer looks sinusoidal; it looks like a series of aperiodic cusps, depicted schematically in Figure 2.2(a). Because of its asymmetry, the beat note waveform contains a finite dc component that pushes the average value of the VCO toward ω_i, and lock is established. When the system is in lock, $\Delta\omega$ is equal to zero and only a steady-state dc error voltage remains.

Figure 2.2(b) displays an oscillogram of the loop error voltage $V_d(t)$ in an actual PLL system during the capture process. Note that as lock is approached, $\Delta\omega$ is reduced, the low pass filter attenuation becomes less, and the amplitude of the beat note increases.

The total time taken by the PLL to establish lock is called *the pull-in time*. Pull-in time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low pass filter bandwidth. Under certain conditions, the pull-in time may be shorter than the period of the beat note and the loop can lock without an oscillatory error transient.

A specific case to illustrate this is shown in Figure 2.3. The 565 PLL is shown acquiring lock within the first cycle of the input signal. The PLL was able to capture in this short time because it was operated as a first order loop (no low pass filter) and the input tone-burst frequency was within its lock and capture range.

EFFECT OF THE LOW PASS FILTER

In the operation of the loop, the low pass filter serves a dual function:

First, by attenuating the high frequency error components at the output of the phase comparator, it enhances the interference-rejection characteristics; second, it provides a short-term memory for the PLL and ensures a rapid recapture of the signal if the system is thrown out of lock due to a noise transient. Decreasing the low pass filter bandwidth has the following effects on system performance:

a The capture process becomes slower, and the pull-in time increases.
b The capture range decreases.
c Interference-rejection properties of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low pass filter.
d The transient response of the loop (the response of the PLL to sudden changes

of the input frequency within the capture range) becomes underdamped.

The last effect also produces a practical limitation on the low pass loop filter bandwidth and roll-off characteristics from a stability standpoint. These points will be explained further in the following analysis.

MATHEMATICALLY DEFINING PLL OPERATION

As mentioned previously, the phase comparator is basically an analog multiplier that forms the product of an RF input signal, $v_i(t)$, and the output signal, $v_o(t)$, from the VCO. Refer to Figure 2.1 and assume that the two signals to be multiplied can be described by

$$v_i(t) = V_i \sin \omega_i t \qquad (2.3)$$

$$v_o(t) = V_o \sin (\omega_o t + \Theta_e) \qquad (2.4)$$

where ω_i, ω_o, and Θ_e are the frequency and phase difference (or phase error) characteristics of interest. The product of these two signals is an output voltage given by

$$v_e(t) = K_1 V_i V_o (\sin \omega_i t)\,[\sin (\omega_o t + \Theta_e)] \qquad (2.5)$$

where K_1 is an appropriate dimensional constant. Note that the amplitude of $v_e(t)$ is directly proportional to the amplitude of the input signal V_i. The two cases of an unlocked loop ($\omega_i \neq \omega_o$) and of a locked loop ($\omega_i = \omega_o$) are now considered separately.

Unlocked State ($\omega_i \neq \omega_o$)

When the two frequencies to the phase comparator are not synchronized, the loop is not locked. Furthermore the phase angle difference Θ_e in Equations 2.4 and 2.5 is meaningless for this case since it can be eliminated by appropriately choosing the time origin.

Using trigonometric identities, Equation 2.5 can be rewritten as

$$v_e(t) = \frac{K_1 V_i V_o}{2}\,[\cos(\omega_i - \omega_o)t - \cos(\omega_i + \omega_o)t] \qquad (2.6)$$

When $v_e(t)$ is passed through the low pass filter, F(s), the sum frequency component is removed, leaving

$$v_f(t) = K_2 V_i V_o \cos (\omega_i - \omega_o)t \qquad (2.7)$$

where K_2 is a constant. After amplification, the control voltage for the VCO appears as

$$v_d(t) = AK_2 V_i V_o \cos (\omega_i - \omega_o)t \qquad (2.8)$$

This equation shows that a beat frequency effect is established between ω_i and ω_o, causing the VCOs frequency to deviate by $\pm\Delta\omega$ from ω_o' in proportion to the signal amplitude ($AK_2V_iV_o$) passing through the filter. If the amplitude of V_i is sufficiently large and if signal limiting or saturation does not occur, the VCO output frequency will be shifted from ω_o' by some $\Delta\omega$ until lock is established where

$$\omega_i = \omega_o = \omega_o' \pm \Delta\omega \qquad (2.9)$$

If lock cannot be established, then either V_i is too small to drive the VCO to produce the necessary $\pm\Delta\omega$ deviation or ω_i is beyond the dynamic range of the VCO, i.e., $\omega_i \gtrless \omega_o \pm \Delta\omega$. Remedies for these no lock conditions are:

1. Increase V_i either internally or externally to the loop by providing additional amplification.
2. Increase the internal loop gain by adjusting upward (larger −3dB frequency) the response of the low-pass filter.
3. Shift ω_o' closer to the expected ω_i. Establishing frequency lock leads to the second case where $\omega_i = \omega_o$.

Locked State ($\omega_i = \omega_o$)

When ω_i and ω_o are frequency synchronized, the output signal from the phase comparator for $\omega_i = \omega_o = \omega$ and a phase shift of Θ_e is

$$v_e(t) = K_1 V_i V_o (\sin \omega t)(\sin \omega t + \Theta_e) = \frac{K_1 V_i V_o}{2}\,[\cos \Theta_e - \cos (2\omega t + \Theta_e)] \qquad (2.10)$$

The low pass filter removes the high frequency, ac component of $v_e(t)$, leaving only the dc component. Thus,

$$v_f(t) = K_2 V_i V_o \cos \Theta_e \qquad (2.11)$$

After amplification the dc voltage driving the VCO and maintaining lock within the loop is

$$v_d(t) = V_D = AK_2 V_i V_o \cos \Theta_e \qquad (2.12)$$

Suppose ω_i and ω_o are perfectly synchronized to the free-running frequency ω_o'. For this case, V_D will be zero, indicating that Θ_e must be $\pm 90°$. Thus V_D is proportional to the phase difference or phase error between Θ_i and Θ_o centered about a reference phase angle of $\pm 90°$. If ω_i changes slightly from ω_o', the first effect will be a change in Θ_e from $\pm 90°$. V_D will adjust and settle out to some nonzero value to correct ω_o; under this condition frequency lock is maintained with $\omega_i = \omega_o$. The phase error will be shifted by some amount $\Delta\Theta$ from the reference phase angle of $\pm 90°$. This concept can be simplified by redefining Θ_e as

$$\Theta_e = \Theta_r \pm \Delta\Theta \qquad (2.13)$$

where Θ_r is the inherent, reference phase shift of $\pm 90°$ and $\Delta\Theta$ is the departure from this reference value. Now the VCO control voltage becomes

$$V_D = AK_2 V_i V_o \cos (\Theta_r \pm \Delta\Theta) = \pm AK_2 V_i V_o \sin \Delta\Theta \qquad (2.14)$$

Since the sine function is odd, a momentary change in $\Delta\Theta$ contains information about

LINEAR MODEL OF PLL SYSTEM

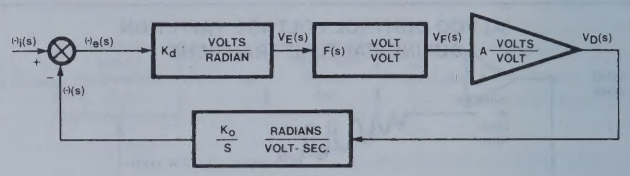


Figure 2.4

MEASUREMENT SCHEME FOR K_d AND K_o DETERMINATIONS

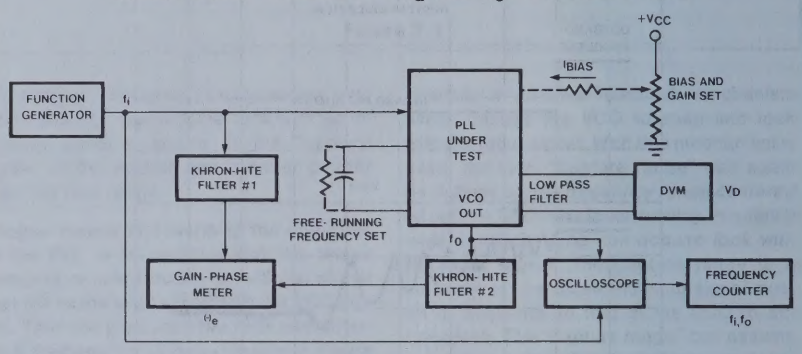


Figure 2.5

which way to adjust the VCO frequency to correct and maintain the locked condition. The maximum range over which $\Delta\Theta$ changes can be tracked is $-90°$ to $+90°$. This corresponds to a Θ_e range from 0 to 180°.

In addition to being an error signal, V_D represents the demodulated output of an FM input applied as $v_{in}(t)$ assuming a linear VCO characteristic. Thus FM demodulation can be accomplished with the PLL without the inductively tuned circuits that are employed with conventional detectors.

DETERMINING PLL MODEL PARAMETERS

Since the PLL is basically an electronic servo loop, many of the analytical techniques developed for control systems are applicable to phase locked systems. Whenever phase lock is established between $v_i(t)$ and $v_o(t)$ the linear model of Figure 2.4 can be used to predict the performance of the PLL system. Here Θ_i and Θ_o represent the phase angles associated with the input and output waveshapes respectively; F(s) represents a generalized voltage transfer function for the low pass filter in the s complex frequency domain; and K_d and K_o are conversion gains of the phase comparator and VCO respectively, each having units as shown. The 1/s term associated with the VCO accounts for the inherent 90° phase shift in the loop since the VCO converts a voltage to a frequency and since phase is the integral of frequency. Thus the VCO functions as an integrator in the feedback loop.

Specific values of K_d and K_o for all of Signetics general purpose PLLs can be found in Chapter 4 in the sections describing the particular loop of interest. However, sometimes it may be desired to determine these conversion gains exactly for a specific device. The measurement scheme shown in Figure 2.5 can be used to determine K_d and K_o for a loop under lock. The function of the Khron-Hite filters is to extract the fundamental sinusoidal frequency component of their square wave inputs for application to the Gain-Phase Meter. If the input signal from the Function Generator is sinusoidal, then the first Khron-Hite filter may be eliminated. It is recommended to use high impedance oscilloscope probes so as to not distort the input or VCO waveshapes, thereby potentially altering their phase relationships. The frequency counter can be driven from the scope as shown, or connected directly to the input or VCO provided its input impedance is large.

The procedure to follow for obtaining K_d and K_o is as follows:

1 Established the desired external bias and gain conditions for the PLL under test.
2 With the Function Generator turned off, set the free-running frequency of the loop via the timing capacitor and timing resistor if appropriate. Monitor f_o' with the Frequency Counter.
3 Turn on the Function Generator and check to make sure the amplitude of the input signal is appropriate for the particular loop under test.
4 Adjust the input frequency for lock. Lock is discernable on a dual-trace scope when the input and VCO waveforms are synchronized and stationary with respect to each other. One should be especially careful to check that locking has not occurred between the VCO and some harmonic frequency. Carefully inspect both waveshapes, making sure each has the same period. (If a second Frequency Counter is available, an alternate scheme can be used to confirm frequency locking. One frequency counter is used to monitor the input signal frequency, and the second counter is used for the VCO frequency. When the two counters display the same frequency, the PLL is locked).
5 Set the input frequency to the free-running frequency and note the Gain-Phase Meter display. It should be approximately 90°, $\pm$ 10° nominally. Record the phase error, Θ_e, the VCO control voltage, V_D, and the input frequency, f_i.
6 Adjust f_i for frequencies above and below f_o' and record Θ_e and V_D for each f_i as appropriate.
7 Making a plot of V_D versus Θ_e is useful for checking the measurement data and the systems linearity. The slope of this plot ($\Delta V_D / \Delta\Theta_e$) is K_d in units of volts/degree. Multiplying this slope by $180/\pi$ gives the desired K_d in volts/radian.
8 A plot of $f_i = f_o$ versus V_D while the loop remains locked will check the VCO linearity. The slope of this plot is K_o at the particular free-running frequency. The units of slope taken directly from the graph are Hz/volt. Multiplying this slope figure by 2π gives the desired K_o in units of radians/volt-sec.

K_d is generally constant over wide frequency ranges, but is linearily related to the input signal amplitude. K_o is constant with input signal level but does vary linearily with f_o'. Often it is convenient to specify a normalized K_o as

$$K_{o(norm)} = \frac{K_o}{f_o'} \quad \frac{\text{radians}}{\text{volt}} \qquad (2.15)$$

The K_o value at any desired free-running frequency then can be estimated as

$$K_o \text{ (@ any } f_o') = K_{o(norm)}\, f_o' \qquad (2.16)$$

The loop gain for the PLL system is

$$K_v = K_d K_o A \qquad (2.17)$$

(Often when the gain A is due to an amplifier internal to the IC, A will be included in either K_d or K_o. This is further illustrated in Chapter 4 for the 565 PLL).

MODELING THE PLL SYSTEM WITH VARIOUS LOW PASS FILTERS

The open loop transfer function for the PLL is

$$T(s) = \frac{K_v F(s)}{s} \qquad (2.18)$$

Using linear feedback analysis techniques, the closed loop transfer characteristics H(s) can be related to the open loop performance as

$$H(s) = \frac{T(s)}{1+T(s)} \qquad (2.19)$$

and the roots of the characteristic system polynominal can be readily determined by root-locus techniques.

From these equations, it is apparent that the transient performance and frequency response of the loop is heavily dependent upon the choice of filter and its corresponding transfer characteristic, F(s).

Zero Order Filter - F(s) = 1

The simplest case is that of the first order loop where F(s) = 1 (no filter). The closed loop transfer function then becomes

$$T(s) = \frac{K_v}{s + K_v} \qquad (2.20)$$

This transfer function gives the root locus as a function of the total loop gain K_v and the corresponding frequency response shown in Figure 2.6(a). The open loop pole at the origin is due to the integrating action of the VCO. Note that the frequency response is actually the amplitude of the difference frequency component versus modulating frequency when the PLL is used to track a frequency modulated input signal. Since there is no low pass filter in this case, sum frequency components are also present at the phase comparator output and must be filtered outside of the loop if the difference frequency component (demodulated FM) is to be measured.

First Order Filter

With the addition of a single pole low pass filter F(s) of the form

$$F(s) = \frac{1}{1+\tau_1 s} \qquad (2.21)$$

where $\tau_1 = R_1 C_1$, the PLL becomes a second order system with the root locus shown in Figure 2.6(b). Again an open loop pole is located at the origin because of the integrating action of the VCO. Another open loop pole is positioned on the real axis at

$-1/\tau_1$ where τ_1 is the time constant of the low pass filter.

One can make the following observations from the root locus characteristics of Figure 2.6(b):

a As the loop gain K_V increases for a given choice of τ_1, the imaginary part of the closed loop poles increase; thus, the natural frequency of the loop increases and the loop becomes more and more underdamped.
b If the filter time constant is increased, the real part of the closed loop poles becomes smaller and the loop damping is reduced.

As in any practical feedback system, excess shifts or non-dominant poles associated with the blocks within the PLL can cause the root loci to bend toward the right half plane as shown by the dashed line in Figure 2.6(b). This is likely to happen if either the loop gain or the filter time constant is too large and may cause the loop to break into sustained oscillations.

First Order Lag-Lead Filter

The stability problem can be eliminated by using a lag-lead type of filter, as indicated in Figure 2.6(c). This type of a filter has the transfer function

$$F(s) = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s} \qquad (2.22)$$

where $\tau_2 = R_2C$ and $\tau_1 = R_1C$. By proper choice of R_2, this type of filter confines the root locus to the left-half plane and ensures stability. The lag-lead filter gives a frequency response dependent on the damping, which can now be controlled by the proper adjustment of τ_1 and τ_2. In practice, this type of filter is important because it allows the loop to be used with a response between that of the first and second order loops and it provides an additional control over the loop transient response. If $R_2 = 0$, the loop behaves as a second order loop and as $R_2 \rightarrow \infty$, the loop behaves as a first order loop due to a pole-zero cancellation. However, as first-order operation is approached, the noise bandwidth increases and interference rejection decreases since the high frequency error components in the loop are now attenuated to a lesser degree.

Second and Higher Order Filters

Second and higher order filters as well as active filters occasionally are designed and incorporated within the PLL to achieve a particular response not possible or easily obtained with zero or first order filters. Chapters 4 and 5 contain several applications of these approaches. Adding more poles and more gain to the closed loop transfer function reduces the inherent stability of the loop. Thus the designer must exercise extreme care and utilize complex stability analysis if second order (and higher) filters or active filters are to be considered.

CALCULATING LOCK AND CAPTURE RANGES

In terms of the basic gain expression in the system, the lock range of the PLL ω_L can be shown to be numerically equal to the dc loop gain

$$2\omega_L = 4\pi f_L = 2K_V F(0) \qquad (2.23)$$

where F(0) is the value of the low pass filters transfer function at dc.

Since the capture range ω_C denotes a transient condition, it is not as readily derived as the lock range. However, an approximate expression for the capture range can be written as

$$2\omega_C = 4\pi f_C \simeq 2K_V \left|F(j\omega_C)\right| \qquad (2.24)$$

where $F(j\omega_C)$ is the magnitude of the low pass filters transfer function evaluated at ω_C. Solution of Equation 2.24 frequently involves a "trial and error" process since the capture range is a function of itself. Note that at all times the capture range is smaller than the lock range.

For the simple first-order lag filter of Figure 2.6 (b) the capture range can be approximated as

$$2\omega_C \simeq 2\sqrt{\frac{\omega_L}{\tau_1}} = 2\sqrt{\frac{K_V}{\tau_1}} \qquad (2.25)$$

This approximation is valid for

$$\tau_1 >> \frac{1}{2\omega_L} \qquad (2.26)$$

Equations 2.23 and 2.24 show that the capture range increases as the low pass filter time constant is decreased, whereas the lock range is unaffected by the filter and is determined solely by the loop gain.

Figure 2.7 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly over a broad frequency range. The vertical scale is the corresponding loop error voltage. In Figure 2.7(a), the input frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency ω_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input and causes a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of VCO conversion gain ($1/K_O$) and goes through zero as $\omega_i = \omega_o'$. The loop tracks the input until the input frequency reaches ω_2, corresponding to the upper edge of the lock range. The PLL then loses lock and the error voltage drops to zero. If the input frequency is swept slowly back, the cycle repeats itself, but is inverted, as shown in Figure 2.7(b). The loop recaptures the signal at ω_3 and tracks it down to ω_4. The total capture and lock ranges of the system are:

$$2\omega_C = \omega_3 - \omega_1 \qquad (2.27)$$

and

$$2\omega_L = \omega_2 - \omega_4 \qquad (2.28)$$

Note that, as indicated by the transfer characteristics of Figure 2.7, the PLL system has an inherent selectivity about the free-running frequency, ω_o'. It will respond only to the input signal frequencies that are separated from ω_o' by less than ω_C or ω_L, depending on whether the loop starts with or without an initial lock condition. The linearity of the frequency-to-voltage conversion characteristics for the PLL is determined solely by the VCO conversion gain. Therefore, in most PLL applications, the VCO is required to have a highly linear voltage-to-frequency transfer characteristic.

DETERMINING LOOP RESPONSE

The transient response of a PLL can be calculated using the model of Figure 2.4 and Equations 2.18 and 2.19 as starting points. Combining these equations gives

$$H(s) = \frac{\Theta_o(s)}{\Theta_i(s)} = \frac{K_V F(s)}{s + K_V F(s)} \qquad (2.29)$$

The phase error which keeps the system in lock is

$$\Theta_e(s) = \Theta_i(s) - \Theta_o(s) \qquad (2.30)$$

Define a phase error transfer function

$$E(s) = \frac{\Theta_e(s)}{\Theta_i(s)} = 1 - \frac{\Theta_o(s)}{\Theta_i(s)} = 1 - H(s) \qquad (2.31)$$

As an example of the utilization of these equations, consider the most common case of a loop employing a simple first-order lag filter where

$$F(s) = \frac{1}{1 + s\tau_1} \qquad (2.32)$$

For this filter, Equations 2.29 and 2.31 become

$$H(s) = \frac{K_V/\tau_1}{s^2 + s/\tau_1 + K_V/\tau_1} \qquad (2.33)$$

$$E(s) = \frac{s(s + 1/\tau_1)}{s^2 + s/\tau_1 + K_V/\tau_1} \qquad (2.34)$$

Both equations are second order and have the same denominator which can be expressed as

$$D(s) = s^2 + s/\tau_1 + K_V/\tau_1 = s^2 + 2\zeta\omega_n s + \omega_n^2 \qquad (2.35)$$

where ω_n and ζ are respectively the systems undamped natural frequency and damping factor defined as

$$\omega_n = \sqrt{K_V/\tau_1} \qquad (2.36)$$

ROOT LOCUS AND FREQUENCY RESPONSE PLOTS

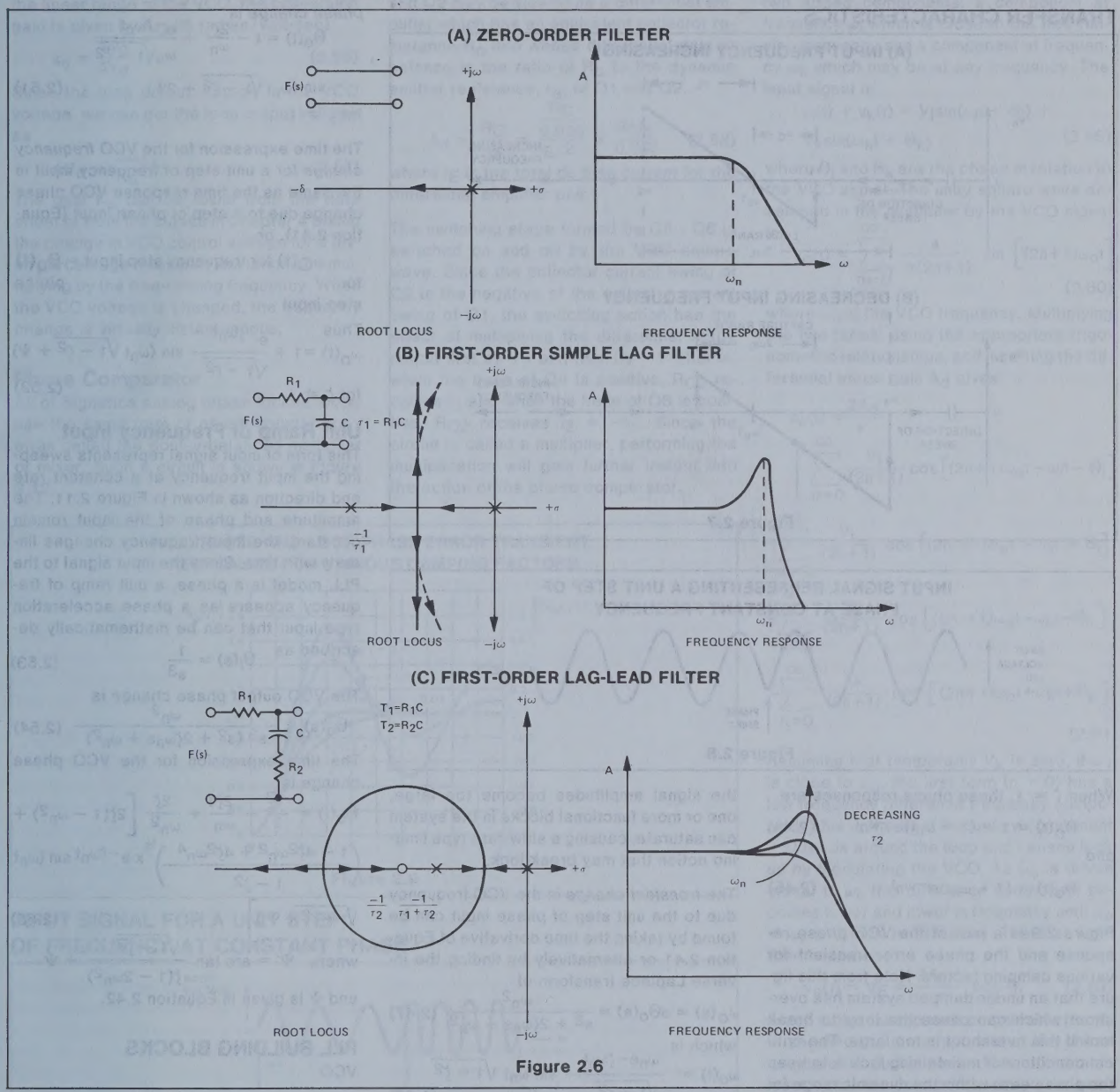


Figure 2.6

$$\zeta = \frac{1}{2\sqrt{K_V \tau_1}} = \frac{\omega_n}{2K_V} \quad (2.37)$$

The system is considered overdamped for $\zeta < 1.0$, and critically damped $\zeta = 1.0$.

Now examine this PLL systems response to various types of inputs.

Step of Phase Input

Consider a unit step of phase as the input signal. This input is shown in Figure 2.8 and can be thought of as simply shifting the time axis by a unit step (one radian or one degree depending upon the working units) while maintaining the same input frequency. Mathematically this input has the form

$$\Theta_i(s) = \frac{1}{s} \quad (2.38)$$

The phase of VCO output and the systems phase error are represented by

$$\Theta_o(s) = \frac{H(s)}{s} = \frac{\omega_n^2}{s(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad (2.39)$$

$$\Theta_e(s) = \frac{E(s)}{s} = \frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.40)$$

Taking the inverse Laplace transform gives the transient response for these phase expressions.

$$\Theta_o(t) = 1 + \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin(\omega_n t\sqrt{1-\zeta^2} + \Psi) \quad (2.41)$$

where $\Psi = \arctan \frac{\sqrt{1-\zeta^2}}{\zeta}$ (2.42)

and $\zeta \neq 1$.

$$\Theta_e(t) = \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin(\omega_n t\sqrt{1-\zeta^2} + \Psi) \quad (2.43)$$

TYPICAL PLL FREQUENCY-TO-VOLTAGE TRANSFER CHARACTERISTICS

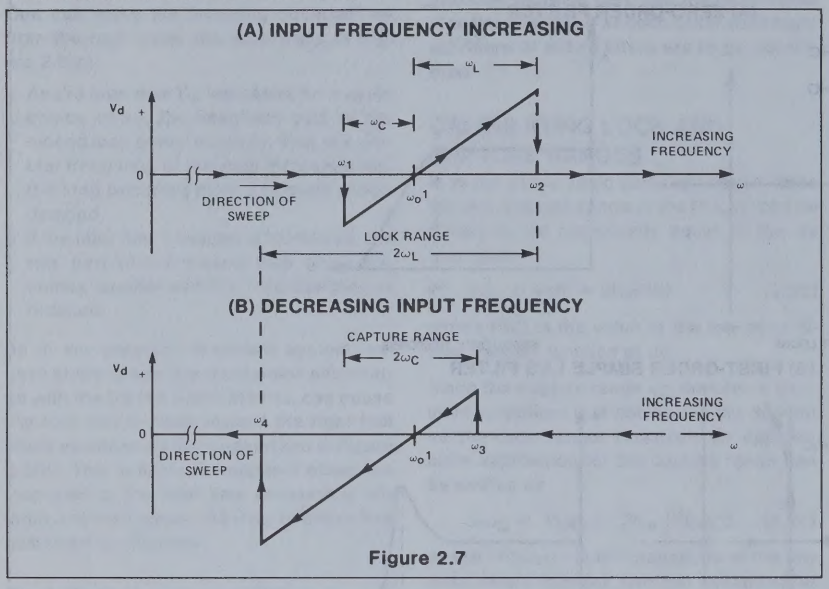


Figure 2.7

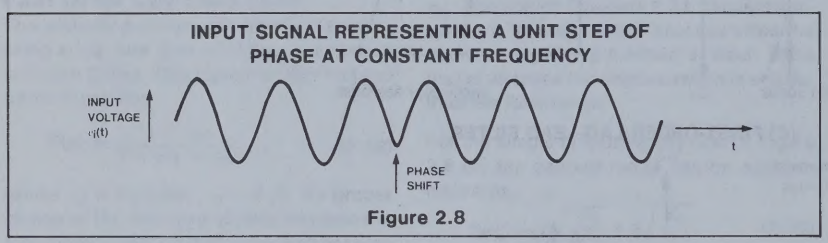


Figure 2.8

When $\zeta = 1$, these phase responses are

$$\Theta_o(t) = 1 - (1 - \omega_n t)e^{-\omega_n t} \quad (2.44)$$

and

$$\Theta_e(t) = (1 + \omega_n t)e^{-\omega_n t} \quad (2.45)$$

Figure 2.9 is a plot of the VCO phase response and the phase error transient for various damping factors. Note from this figure that an under-damped system has overshoot which can cause the loop to break lock if this overshoot is too large. The critical condition for maintaining lock is to keep the phase error within the dynamic range for the phase comparator of $-\pi/2$ to $\pi/2$ radians. For the under-damped case, the peak phase-error overshoot is

$$\Theta_{e(max)} = e^{-\zeta\pi/\sqrt{1-\zeta^2}} \quad (2.46)$$

which must be less than $\pi/2$ to maintain lock. Lock can also be broken for the over-damped and critically-damped loops if the input phase shift is too large where the phase error exceeds $\pm\pi/2$ radians.

The analysis and equations given are based upon the small-signal model of Figure 2.4. If the signal amplitudes become too large, one or more functional blocks in the system can saturate, causing a slew-rate type limiting action that may break lock.

The *transient change* in the VCO frequency due to the unit step of phase input can be found by taking the time derivative of Equation 2.41 or alternatively by finding the inverse Laplace transform of

$$\omega_o(s) = s\Theta_o(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.47)$$

which is

$$\omega_o(t) = \frac{\omega_n e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin \omega_n t\sqrt{1-\zeta^2} \quad (2.48)$$

Unit Step of Frequency Input

This type of input occurs when the input frequency is instantaneously changed from one frequency to another as is done in FSK and modem applications. For this input as shown in Figure 2.10,

$$\Theta_i(s) = \frac{1}{s^2} \quad (2.49)$$

The VCO output phase is

$$\Theta_o(s) = \frac{\omega_n^2}{s^2(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad (2.50)$$

The transient time expression for the *VCO phase change* is

$$\Theta_o(t) = t - \frac{2\zeta}{\omega_n} + \frac{e^{-\zeta\omega_n t}}{\omega_n\sqrt{1-\zeta^2}} \sin(\omega_n t\sqrt{1-\zeta^2} + 2\Psi) \quad (2.51)$$

for $\zeta \neq 1$.

The time expression for the VCO *frequency change* for a unit step of frequency input is the same as the time response VCO phase change due to a step of phase input (Equation 2.41), or

$\omega_O(t)$ for frequency step input = $\Theta_O(t)$ for phase step input

Thus

$$\omega_o(t) = 1 + \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin(\omega_n t\sqrt{1-\zeta^2} + \Psi) \quad (2.52)$$

for $\zeta \neq 1$.

Unit Ramp of Frequency Input

This form of input signal represents sweeping the input frequency at a constant rate and direction as shown in Figure 2.11. The amplitude and phase of the input remain constant; the input frequency changes linearly with time. Since the input signal to the PLL model is a phase, a unit ramp of frequency appears as a phase acceleration type input that can be mathematically described as

$$\Theta_i(s) = \frac{1}{s^3} \quad (2.53)$$

The VCO output phase change is

$$\Theta_o(s) = \frac{\omega_n^2}{s^3(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad (2.54)$$

The time expression for the VCO phase change is

$$\Theta_o(t) = \frac{t^2}{2} - \frac{2\zeta t}{\omega_n} + \frac{2\zeta}{\omega_n^2}\left[2\zeta(1-\omega_n^2) + \left(\frac{1 - 4\zeta^2\omega_n^2 + 4\zeta^2\omega_n^4}{1-\zeta^2}\right)^{1/2} x\, e^{-\zeta\omega_n t} \sin(\omega_n t\sqrt{1-\zeta^2} + \Psi')\right] \quad (2.55)$$

where $\Psi' = \arctan\dfrac{\sqrt{1-\zeta^2}}{\zeta(1-2\omega_n^2)} + \Psi$

and Ψ is given in Equation 2.42.

PLL BUILDING BLOCKS

VCO

Since three different forms of VCO have been used in the Signetics PLL series, the VCO details will not be discussed until the individual loops are described in Chapter 4. However, a few general comments about VCOs are in order.

When the PLL is locked to a signal, the VCO voltage is a function of the frequency of the input signal. Since the VCO control voltage is the demodulated output during FM demodulation, it is important that the VCO voltage-to-frequency characteristic be lin-

ear so that the output is not distorted. Over the linear range of the VCO, the conversion gain is given by K_O (in radian/volt-sec)

$$k_o = \frac{\Delta\omega_o}{\Delta V_d} \quad (2.56)$$

Since the loop output voltage is the VCO voltage, we can get the loop output voltage as

$$\Delta V_d = \frac{\Delta\omega_o}{K_o} \quad (2.57)$$

The gain K_O can be found from the data sheet or from the curves in Chapter 4 taking the change in VCO control voltage for a given percentage frequency deviation and multiplying by the free-running frequency. When the VCO voltage is changed, the frequency change is virtually instantaneous.

Phase Comparator

All of Signetics analog phase locked loops use the same form of phase comparator - often called the doubly-balanced multiplier or mixer. Such a circuit is shown in Figure 2.12.

The input stage formed by transistors Q1 and Q2 may be viewed as a differential amplifier which has an equivalent collector resistance R_C and whose differential gain at balance is the ratio of R_C to the dynamic emitter resistance, r_e, of Q1 and Q2.

$$A_d = \frac{R_C}{r_e} = \frac{R_C}{\frac{0.026}{I_E/2}} = \frac{R_C I_E}{0.052} \quad (2.58)$$

where I_E is the total dc bias current for the differential amplifier pair.

The switching stage formed by Q3 - Q6 is switched on and off by the VCO square wave. Since the collector current swing of Q2 is the negative of the collector current swing of Q1, the switching action has the effect of multiplying the differential stage output first by +1 and then by −1. That is, when the base of Q4 is positive, R_{C2} receives i_1 and when the base of Q6 is positive, R_{C2} receives $i_2 = -i_1$. Since the circuit is called a multiplier, performing the multiplication will gain further insight into the action of the phase comparator.

VCO PHASE AND LOOP PHASE ERROR TRANSIENT RESPONSES FOR VARIOUS DAMPING FACTORS

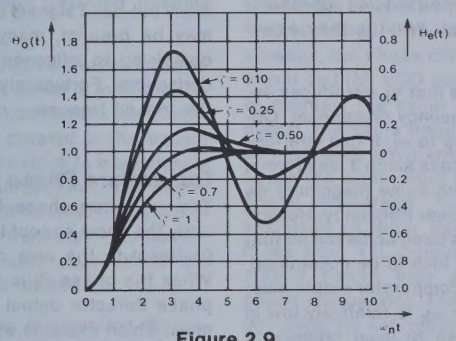


Figure 2.9

INPUT SIGNAL FOR A UNIT STEP OF FREQUENCY AT CONSTANT PHASE

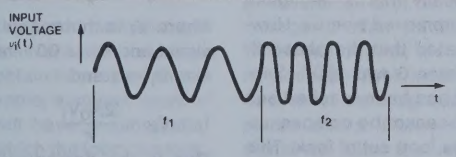


Figure 2.10

INPUT SIGNAL FOR A UNIT RAMP OF FREQUENCY INPUT

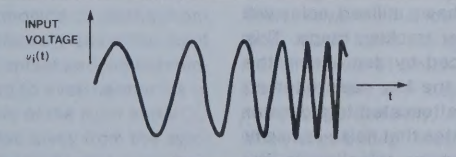


Figure 2.11

Consider an input signal which consists of two added components: a component at frequency ω_i which is close to the free-running frequency and a component at frequency ω_k which may be at any frequency. The input signal is

$$v_i(t) + v_k(t) = V_i\sin(\omega_i t + \Theta_i) + V_k\sin(\omega_k t + \Theta_k) \quad (2.59)$$

where Θ_i and Θ_k are the phase in relation to the VCO signal. The unity square wave developed in the multiplier by the VCO signal is

$$v_o(t) = \sum_{n=0}^{\infty} \frac{4}{\pi(2n+1)} \sin\left[(2n+1)\omega_o t\right] \quad (2.60)$$

where ω_o is the VCO frequency. Multiplying the two terms, using the appropriate trigonometric relationships, and inserting the differential stage gain A_d gives:

$$v_e(t) = \frac{2A_d}{\pi}\left[\sum_{n=0}^{\infty} \frac{V_i}{(2n+1)} \cos\left[(2n+1)\omega_o t - \omega_i t - \Theta_i\right] - \sum_{n=0}^{\infty} \frac{V_i}{(2n+1)} \cos\left[(2n+1)\omega_o t + \omega_i t + \Theta_i\right] + \sum_{n=0}^{\infty} \frac{V_k}{(2n+1)} \cos\left[(2n+1)\omega_o t - \omega_k t - \Theta_k\right] - \sum_{n=0}^{\infty} \frac{V_k}{(2n+1)} \cos\left[(2n+1)\omega_o t + \omega_k t + \Theta_k\right]\right] \quad (2.61)$$

Assuming that temporarily V_k is zero, if ω_1 is close to ω_o, the first term (n = 0) has a low frequency difference frequency component. This is the beat frequency component that feeds around the loop and causes lock up by modulating the VCO. As ω_o is driven closer to ω_i, this difference component becomes lower and lower in frequency until $\omega_o = \omega_i$ and lock is achieved. The first term then becomes

$$v_e(t) = V_E = \frac{2A_d V_i}{\pi} \cos\Theta_i \quad (2.62)$$

which is the usual phase comparator formula showing the dc component of the phase comparator during lock. This component must equal the voltage necessary to keep the VCO at ω_o. It is possible for ω_o to equal ω_i momentarily during the lock up process and, yet, for the phase to be incorrect so that ω_o passes through ω_i without lock being achieved. This explains why lock is usually not achieved instantaneously, even when $\omega_i = \omega_o$ at t = 0.

If $n \neq 0$ in the first term, the loop can lock when $\omega_i = (2n+1)\omega_o$, giving the dc phase comparator component

$$V_e(t) = V_E = \frac{2A_d V_i}{\pi(2n+1)} \cos\Theta_i \quad (2.63)$$

INTEGRATED PHASE COMPARATOR CIRCUIT

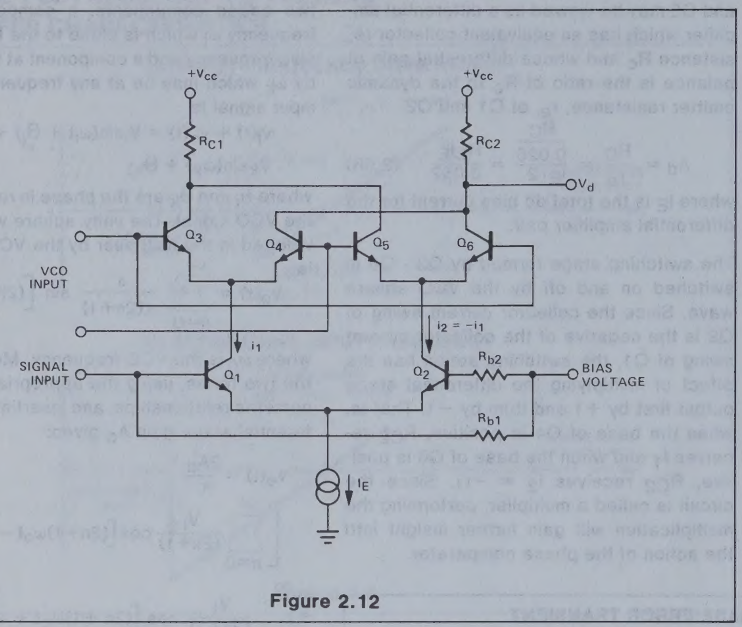


Figure 2.12

showing that the loop can lock to odd harmonics of the free-running frequency. The $(2n + 1)$ term in the denominator shows that the phase comparators output is lower for harmonic lock, which explains why the lock range decreases as higher and higher odd harmonics are used to achieve lock.

Note also that the phase comparators output during lock is (assuming A_d is constant) also a function of the input amplitude V_i. Thus, for a given dc phase comparator output V_E, an input amplitude decrease must be accompanied by a phase change. Since the loop can remain locked only for Θ_i between 0 and 180°, the lower V_i becomes, the more the lock range is reduced.

Note from the second term that during lock the lowest possible frequency is $\omega_o + \omega_i = 2\omega_i$. A sum frequency component is always present at the phase comparator output. This component is usually greatly attenuated by the low pass filter capacitor connected to the phase comparator output. However, when rapid tracking is required (as with high-speed FM detection or FSK-frequency shift keying), the requirement for a relatively high frequency cutoff in the low pass filter may leave this component unattenuated to the extent that it interferes with detection. At the very least, additional filtering may be required to remove this component. Components caused by $n \neq 0$ in the second term are both attenuated and of much higher frequency, so they may be neglected.

Suppose that other frequencies represented by V_k are present. What is their effect for $V_k \neq 0$?

The third term shows that V_k introduces another difference frequency component. Obviously, if ω_k is close to ω_i, it can interfere with the locking process since it may form a beat frequency of the same magnitude as the desired locking beat frequency. However, suppose lock has been achieved so that $\omega_o = \omega_i$. In order for lock to be maintained, the average phase comparator output must be constant. If $\omega_o = \omega_k$ is relatively low in frequency, the phase Θ_i must change to compensate for this beat frequency. Broadly speaking, any signal in addition to the signal to which the loop is locked causes a phase variation. Usually this is negligible since ω_k is often far removed from ω_i. However, it has been stated that the phase Θ_i can move only between 0 and 180°. Suppose the phase limit has been reached and V_k appears. Since it cannot be compensated for, it will drive the loop out of lock. This explains why extraneous signals can result in a decrease in the lock range. If V_k is assumed to be an instantaneous noise component, the same effect occurs. When the full swing of the loop is being utilized, noise will decrease the lock or tracking range. This effect can be reduced by decreasing the cutoff frequency of the low pass filter so that the $\omega_o - \omega_k$ is attenuated to a greater extent, which illustrates that noise immunity and out-band frequency rejection is improved (at the expense of capture range since $\omega_o - \omega_i$ is likewise attenuated) when the low pass filter capacitor is large.

The third term can have a dc component when ω_k is an odd harmonic of the locked frequency so that $(2n + 1)(\omega_o - \omega_1)$ is zero and Θ_k makes its appearance. This will have an effect on Θ_1 which will change the Θ_1 versus frequency ω_1. This is most noticeable when the waveform of the incoming signal is, for example, a square wave. The Θ_k term will combine with the Θ_i term so that the phase is a linear function of input frequency. Other waveforms will give different phase versus frequency functions. When the input amplitude V_i is large and the loop gain is large, the phase will be close to 90° throughout the range of VCO swing, so this effect is often unnoticed.

The fourth term is of little consequence except that if ω_k approaches zero, the phase comparator output will have a component at the locked frequency ω_o at the output. For example, a dc offset at the input differential stage will appear as a square wave of fundamental ω_o at the phase comparator output. This is usually small and well attenuated by the low pass filter. Since many out-band signals or noise components may be present, many V_k terms may be combining to influence locking and phase during lock. Fortunately, only those close to the locked frequency need be considered.

Quadrature Phase Detector (QPD)

The quadrature phase detector action is exactly the same except that its output is proportional to the sine of the phase angle. When the phase Θ_i is 90°, the quadrature phase detector output is then at its maximum, which explains why it makes a useful lock or amplitude detector. The output of the quadrature phase detector is given by

$$V_q = \frac{2A_q V_i}{\pi} \sin \Theta_i \qquad (2.64)$$

where V_i is the constant or modulated AM signal and $\Theta_i \approx 90°$ in most cases so that sine $\Theta_i = 1$ and

$$V_q = \frac{2A_q V_i}{\pi} \qquad (2.65)$$

This is the demodulation principle of the autodyne receiver and the basis for the 567 tone decoder operation.

INITIAL PLL SETUP CHOICES

In a given application, maximum PLL effectiveness can be achieved if the designer understands the tradeoffs which can be made. Generally speaking, the designer is free to select the frequency, lock range, capture range, and input amplitude.

FREE-RUNNING FREQUENCY SELECTION

Setting the center or free-running frequency is accomplished by selecting one or two external components. The center frequency is usually set in the center of the expected input frequency range. Since the loops ability to capture is a function of the *difference* between the incoming and free-running frequencies, the band edges of the capture range are *always* an equal distance (in Hz) from the center frequency. Typically, the lock range is also centered about the free-running frequency. Occasionally, the center frequency is chosen to be offset from the incoming frequency so that the tracking range is limited on one side. This permits rejection of an adjacent higher or lower frequency signal without paying the penalty for narrow band operation (reduced tracking speed).

All of Signetics loops use a phase comparator in which the input signal is multiplied by a unity square wave at the VCO frequency. The odd harmonics present in the square wave permit the loop to lock to input signals at these odd harmonics. Thus, the center frequency may be set to, say, 1/3 or 1/5 of the input signal. The tracking range however, will be considerably reduced as the higher harmonics are utilized.

The foregoing phase comparator discussion would suggest that the PLL cannot lock to subharmonics because the phase comparator cannot produce a dc component if ω_i is less than ω_o.

The loop can lock to both odd harmonic and subharmonic signals in practice because such signals often contain harmonic components at ω_o. For example, a square wave of fundamental $\omega_o/3$ will have a substantial component at ω_o to which the loop can lock. Even a pure sine wave input signal can be used for harmonic locking if the PLL input stage is overdriven (the resultant internal limiting generates harmonic frequencies). Locking to even harmonics or subharmonics is the least satisfactory since the input or VCO signal must contain second harmonic distortion. If locking to even harmonics is desired, the duty cycle of the input and VCO signals must be shifted away from the symmetrical to generate substantial even harmonic content.

In evaluating the loop for a potential application, it is best to actually compute the magnitude of the expected signal component nearest ω_o. This magnitude can be used to estimate the capture and lock ranges.

All of Signetics loops are stabilized against center frequency drift due to power supply variations. Both the 565 and the 567 are temperature compensated over the entire military temperature range (−55 to +125°C). To benefit from this inherent stability, however, the designer must provide equally stable (or better) external components. For maximum cost effectiveness in some noncritical applications, the designer may wish to trade some stability for lower cost external components.

GUIDELINES FOR LOCK RANGE CONTROL

Two things limit the lock range. First, any VCO can swing only so far; if the input signal frequency goes beyond this limit, lock will be lost. Second, the voltage developed by the phase comparator is proportional to the product of *both* the phase and the amplitude of the in-band component to which the loop is locked. If the signal amplitude decreases, the phase difference between the signal and the VCO must increase in order to maintain the same output voltage and, hence, the same frequency deviation. The 564 contains an internal limiter circuit between the signal input and one input to the phase comparator. This circuit limits the amplitude of large input signals such as those from TTL outputs to approximately 100mV before they are applied to the phase comparator. The limiter significantly improves the AM rejection of the PLL for input signal amplitudes greater than 100mV.

It often happens with low input amplitudes that even the full ±90° phase range of the phase comparator cannot generate enough voltage to allow tracking wide deviations. When this occurs, the effective lock range is reduced. Weak input signals cause a reduction of tracking capability and greater phase errors. Conversely, a strong input signal will allow the use of the entire VCO swing capability and keeps the VCO phase (referred to the input signal) very close to 90° throughout the range. Note that the lock range does not depend on the low pass filter. However, if a low pass filter *is* in the loop, it will have the effect of limiting the maximum *rate* at which tracking can occur. Obviously, the LPF capacitor voltage cannot change instantly, so lock may be lost when large enough step changes occur. Between the constant frequency input and the step-change frequency input is some limiting frequency slew rate at which lock is just barely maintained. When tracking at this rate, the phase difference is at its limit of 0° or 180°. It can be seen that if the LPF cutoff frequency is low, the loop will be unable to track as fast as if the LPF cutoff frequency is higher. *Thus, when maximum tracking rate is needed, the LPF should have a high cutoff frequency.* However, a high cutoff frequency LPF will attenuate the sum frequencies to a lesser extent so that the output contains a significant and often bothersome signal at twice the input frequency. The phase comparators output contains both sum and difference frequencies. During lock, the difference frequency is zero, but the sum frequency of twice the locked frequency is still present. This sum frequency component can then be filtered out with an external low pass filter.

INPUT LEVEL AMPLITUDE SELECTION

Whenever amplitude limiting of the in-band signal occurs, whether in the loop input stages or prior to the input, the lock and capture ranges become independent of signal amplitude.

Better noise and out-band signal immunity is achieved when the input levels are below the limiting threshold since the input stage is in its linear region and the creation of cross-modulation components is reduced. Higher input levels will allow somewhat faster operation due to greater phase comparator gain and will result in a lock range which becomes constant with amplitude as the phase comparator gain becomes constant. Also, high input levels will result in a linear phase versus frequency characteristic.

CAPTURE RANGE CONTROL

There are two main reasons for making the low pass filter time constant large. First, a large time constant provides an increased memory effect in the loop so that it remains at or near the operating frequency during momentary fading or loss of signal. Second, the large time constant integrates the phase comparators output so that increased immunity to noise and out-band signals is obtained.

Besides the lower tracking rates attendant to large loop filters, other penalties must be paid for the benefits gained. The capture range is reduced and the capture transient becomes longer. Reduction of capture range occurs because the loop must utilize the magnitude of the difference frequency component at the phase comparator to drive the VCO towards the input frequency.

If the LPF cutoff frequency is low, the difference component amplitude is reduced and the loop cannot swing as far. Thus, the capture range is reduced.

LOCK-UP TIME AND TRACKING SPEED CONTROL

In tracking applications, lock-up time is normally of little consequence, but occasions do arise when it is desirable to keep lock-up time short to minimize data loss when noise or extraneous signals drive the loop out of lock. Lock-up time is of great importance in tone decoder type applications. Tracking speed is important if the loop is used to demodulate an FM signal. Although the following discussion dwells largely on lock-up time, the same comments apply to tracking speeds.

No simple expression is available which adequately describes the acquisition or lock-up time. This may be appreciated when we review the following factors which influence lock-up time.

a Input phase
b Low pass filter characteristic
c Loop damping
d Deviation of input frequency from center frequency
e In-band input amplitude
f Out-band signals and noise
g Center frequency

Fortunately, it is usually sufficient to know how to improve the lock-up time and what must be sacrificed to get faster lock-up. Consider an operational loop or tone decoder where occasionally the lock-up transient is too long. What can be done to improve the situation-keeping in mind the factors that influence lock?

a Initial phase relationship between incoming signal and VCO - This is the greatest single factor influencing the lock time. If the initial phase is wrong, it first drives the VCO frequency *away* from the input frequency so that the VCO frequency must walk back on the beat notes. Figure 3.1 gives a typical distribution of lock-up times with the input pulse initiated at random phase. The only way to overcome this variation is to send phase information all the time so that a favorable phase relationship is guaranteed at t = 0. For example, a number of PLLs or tone decoders may be weakly locked to low amplitude harmonics of a pulse train and the transmitted tone phase related to the same pulse train. Usually, however, the incoming phase cannot be controlled.

b Low pass filter - The larger the low pass filter time constant, the longer will be the lock-up time. The lock-up time can be reduced by decreasing the filter time constant, but in doing so, some of the noise immunity and out-band signal rejection will be sacrificed. This is unfortunate since this is what necessitated the use of a large filter in the first place. Also present will be a sum frequency (twice the VCO frequency) component at the low pass filter and greater phase jitter resulting from out-band signals and noise. In the case of the tone decoder (where control of the capture range is required since it specifies the device bandwidth) a lower value of low pass capacitor automatically increases the bandwidth. Speed is gained only at the expense of added bandwidth.

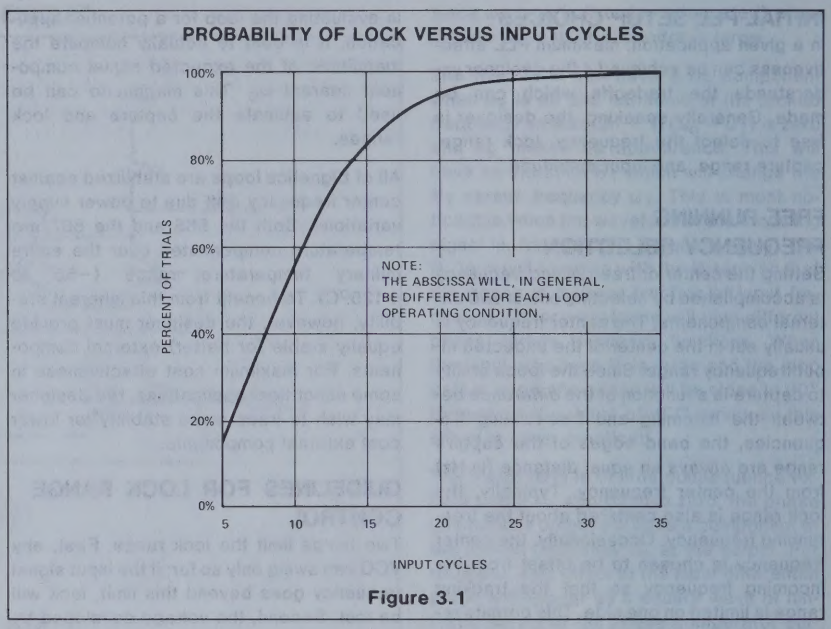


Figure 3.1

c Loop damping - A simple first-order low pass filter of the form

$$F(s) = \frac{1}{1 + s\tau} \qquad (3.1)$$

produces a loop damping of

$$\zeta = \frac{1}{2}\sqrt{\frac{1}{\tau K_V}} \qquad (3.2)$$

Damping can be increased not only by reducing τ, as discussed above, but also by reducing the loop gain K_V. Using the loop gain reduction to control bandwidth or capture and lock ranges achieves better damping for narrow bandwidth operation. The penalty for this damping is that more phase comparator output is required for a given deviation so that phase errors are greater and noise immunity is reduced. Also, more input drive may be required for a given deviation.

d Input frequency deviation from free-running frequency - Naturally, the further an applied input signal is from the free-running frequency of the loop, the longer it will take the loop to reach that frequency due to the charging time of the low pass filter capacitor. Usually, however, the effect of this frequency deviation is small compared to the variation resulting from the initial phase uncertainty. Where loop damping is very low, however, it may be predominant.

e In-band input amplitude - Since input amplitude is one factor in the phase comparators gain K_d and since K_d is a factor in the loop gain K_V, damping is also a function of input amplitude. When the input amplitude is low, the lock-up time may be limited by the rate at which the low pass capacitor can charge with the reduced phase comparator output (see d above).

f Out-band signals and noise - Low levels of extraneous signals and noise have little effect on the lock-up time, neither improving or degrading it. However, large levels may overdrive the loop input stage so that limiting occurs, at which point the in-band signal starts to be suppressed. The lower effective input level can cause the lock-up time to increase, as discussed in e above.

g Center frequency - Since lock-up time can be described in terms of the number of cycles to lock, fastest lock-up is achieved at higher frequencies. Thus, whenever a system can be operated at a higher frequency, lock will typically take place faster. Also, in systems where different frequencies are being detected,

the higher frequencies *on the average* will be detected before the lower frequencies.

However, because of the wide variation due to initial phase, the reverse may be true for any single trial.

PLL MEASUREMENT TECHNIQUES

This section deals with measurements of PLL operation. The techniques suggested are meant to help the designer in evaluating the performance of the PLL during the initial setup period as well as to point out some pitfalls that may obscure loop evaluation. Recognizing that the test equipment may be limited, techniques are described which require a minimum of standard test items.

The majority of the PLL tests described can be done with a signal generator, a scope and a frequency counter. Most laboratories have these. A low-cost digital voltmeter will facilitate accurate measurement of the VCO conversion gain. Where the need for a FM generator arises, it may be met in most cases by the VCO of a Signetics PLL. Any of the loops may be set up to operate as a VCO by simply applying the modulating voltage to the low pass filter terminal(s). The resulting generator may be checked for linearity by using the counter to check frequency as a function of modulating voltage. Since the VCOs may be modulated right down to dc, the calibration may be done in steps. Moreover, Gardner (3) shows how loop measurements may be made by applying a *constant* frequency to the loop input and the modulating signal to the low pass filter terminal to simulate the effect of a FM input so that a FM generator may be omitted for many measurements.

FREE-RUNNING FREQUENCY

Free-running frequency measurements are easily made by connecting a frequency counter or oscilloscope to the VCO output of the loop. The loop should be connected in its final configuration with the chosen values of input, bypass, and low pass filter capacitors. No input signal should be present. As the free-running frequency is read out, it can be adjusted to the desired value by the adjustment means selected for the particular loop. It is important not to make the frequency measurement directly at the timing capacitor unless the capacity added by the measurement probe is much less than the timing capacitor value since the probe capacity will then cause a frequency error.

When the frequency measurement is to be converted to a dc voltage for production readout or automated testing, a calibrated phase locked loop can be used as a frequency meter.

CAPTURE AND LOCK RANGES

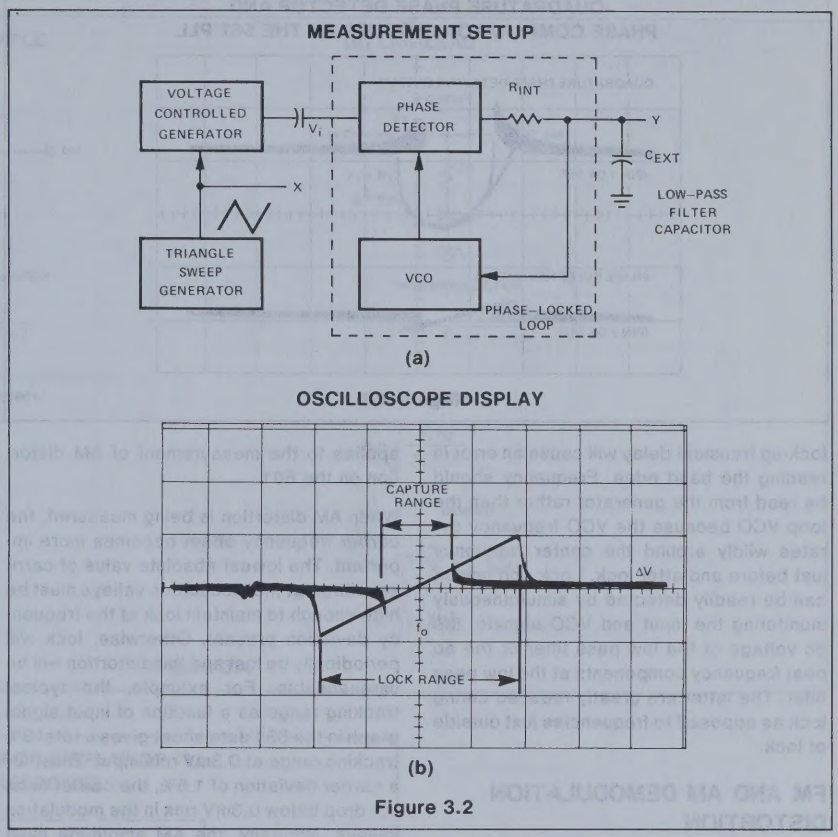


Figure 3.2

CAPTURE AND LOCK RANGES

Figure 3.2(a) shows a typical measurement setup for capture and lock range measurements. The signal input from a variable frequency oscillator is swept linearly through the frequency range of interest and the loop FM output is displayed on a scope or (at low frequencies) X-Y recorder. The sweep voltage is applied to the X axis.

Figure 3.2(b) shows the type of trace which results. The lock range is given by the outer lines on the trace, which are formed as the incoming frequency sweeps away from the center frequency. The inner trace, formed as the frequency sweeps toward the center frequency, designates the capture range. Linearity of the VCO is revealed by the straightness of the trace portion within the lock range. The slope ($\Delta f/\Delta V$) is the conversion gain K_o for the VCO *at the particular free-running frequency.*

By using the sweep technique, the effect on free-running frequency, capture range, and lock range of the input amplitude, supply voltage, low pass filter and temperature can be examined.

Because of the lock-up time duration and variation, the sweep frequency must be very much lower than the free-running frequency, especially when the capture range is below 10% of the free-running frequency. Otherwise, the *apparent* capture and lock range will be a function of sweep frequency. It is best to start sweeping as slow as possible and, if desired, increase the rate until the capture range begins to show an apparent reduction – indicating that the sweep is too fast. Typical sweep frequencies are in the range of 1/1000 to 1/100,000 of the free-running frequency. In the case of the 561 and 567, the quadrature detector output may be similarly displayed on the Y axis, as shown in Figure 3.3 showing the output level versus frequency for one value of input amplitude.

Capture and lock range measurements may also be made by sweeping the generator manually through the band of interest. Sweeping must be done very slowly as the edges of the capture range are approached (sweeping toward center frequency) or the

QUADRATURE PHASE DETECTOR AND
PHASE COMPARATOR OUTPUTS OF THE 567 PLL

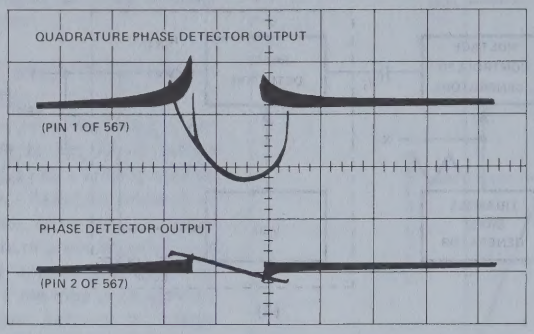


Figure 3.3

lock-up transient delay will cause an error in reading the band edge. Frequency should be read from the generator rather than the loop VCO because the VCO frequency gyrates wildly around the center frequency just before and after lock. Lock and unlock can be readily detected by simultaneously monitoring the input and VCO signals, the dc voltage at the low pass filter or the ac beat frequency components at the low pass filter. The latter are greatly reduced during lock as opposed to frequencies just outside of lock.

FM AND AM DEMODULATION DISTORTION

These measurements are quite straightforward. The loop is simply setup for FM or AM (561 or 567) detection and the test signal is applied to the input. A spectrum analyzer or distortion analyzer (HP333A) can be used to measure distortion at the FM or AM output.

For FM demodulation, the input signal amplitude must be large enough so that lock is not lost at the frequency extremes. The data sheets give the lock (or tracking) range as a function of input signal and the optional range control adjustments. Due to the inherent linearity of the VCOs, it makes little difference whether the FM carrrier is at the free-running frequency or offset slightly as long as the tracking range limits are not exceeded.

The faster the FM modulation in relation to the center frequency, the lower the value of the capacitor in the low pass filter must be for satisfactory tracking. As this value decreases, however, it attenuates the sum frequency component of the phase comparator output less. The demodulated signal will appear to have greater distortion unless this component is filtered out before the distortion is measured. The same comment applies to the measurement of AM distortion on the 561.

When AM distortion is being measured, the carrier frequency offset becomes more important. The lowest absolute value of carrier voltage at the modulation valleys must be high enough to maintain lock at the frequency deviation present. Otherwise, lock will periodically be lost and the distortion will be unreasonable. For example, the typical tracking range as a function of input signal graph in the 561 data sheet gives a total 3% tracking range at 0.3mV rms input. Thus, for a carrier deviation of 1.5%, the carrier must not drop below 0.3mV rms in the modulation valleys. Naturally, the AM amplitude must not be too high or the AM information will be suppressed.

NATURAL FREQUENCY AND DAMPING

Circuits and mathematical expressions for the natural frequencies and dampings are given in Figure 3.4 for two, first-order low pass filters. Because of the integrator action of the PLL in converting frequency to phase, the order of the loop always will be one greater than the order of the LPF. Hence both these first order LPFs produce a second order PLL system.

The natural frequency (ω_n) of a loop in its final circuit configuration can be measured by applying a frequency modulated signal of the desired amplitude to the loop. Figure 3.4 shows that the natural frequency is a function of K_d, which is, in turn, a function of input amplitude. As the modulation frequency (ω_m) is increased, the phase relationship between the modulation and recovered sine wave will go through 90^o at $S_m = \omega_n$ and the output amplitude will peak.

Damping is a function of K_d, K_o, and the low pass filter. Since K_o and K_d are functions of the free-running frequency and input amplitude respectively, damping is highly dependent on the particular operating condition of the loop. Damping estimates for the desired operating condition can be made by applying an input signal which is frequency modulated within the lock range by a square wave. The low pass filter voltage is then monitored on an oscilloscope which is synchronized to the modulating waveform, as shown in Figure 3.5. Figure 3.6 shows typical waveforms displayed. The loop damping can be estimated by comparing the number and magnitude of the overshoots with the graph of Figure 3.7(a) which gives the transient phase error due to a step in input frequency.

D'Azzo and Houpis (9) give an expression for calculating the damping for any underdamped second-order system ($\zeta < 1.0$) when the normalized peak overshoot is known. This expression is

$$M_p = 1 + e^{-\zeta\pi/\sqrt{1-\zeta^2}} \qquad (3.3)$$

Examination of Figure 3.6(a) shows that the normalized peak overshoot of the error voltage is approximately 1.4. Using this value for M_p in Equation 3.3 gives a damping of $\zeta \simeq 0.28$.

Another way of estimating damping is to make use of the frequency response plot measured for the natural frequency (ω_n) measurement. For low damping constants, the frequency response measurement peak will be a strong function of damping. For high damping constants, the 3dB-down point will give the damping. Figure 3.7(b) tabulates some approximate relationships.

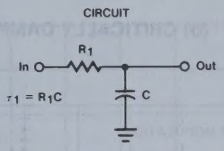
NOISE

The effect of input noise on loop operation is very difficult to predict. Briefly, the input noise components near the center frequency are converted to phase noise. When the phase noise becomes so great that the $\pm 90^o$ permissible phase variation is exceeded, the loop drops out of lock or fails to acquire lock. The best technique is to actually apply the anticipated noise amplitude and bandwidth to the input and then perform the capture and lock range measurements as well as perform operating tests with the anticipated input level and modulation deviations. By including a small safety factor in the loop design to compensate for small processing variations, satisfactory operation can be assured.

FIRST ORDER LOW PASS FILTERS

(A) SIMPLE

CIRCUIT



TRANSFER FUNCTION

$$F(s) = \frac{1}{1 + s\tau_1}$$

NATURAL FREQUENCY

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1}}$$

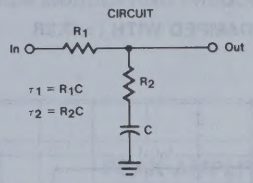
DAMPING

$$\zeta = \frac{\omega_n}{2K_o K_d}$$

(a)

(B) LAG-LEAD

CIRCUIT



TRANSFER FUNCTION

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}$$

NATURAL FREQUENCY

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1 + \tau_2}}$$

DAMPING

$$\zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K_o K_d}\right)$$

(b)

Figure 3.4

MEASUREMENT SETUP FOR DISPLAY OF PLL TRANSIENT RESPONSE

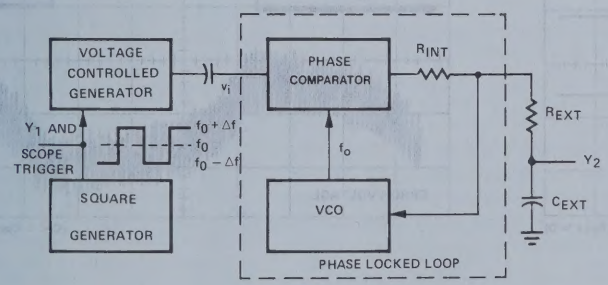
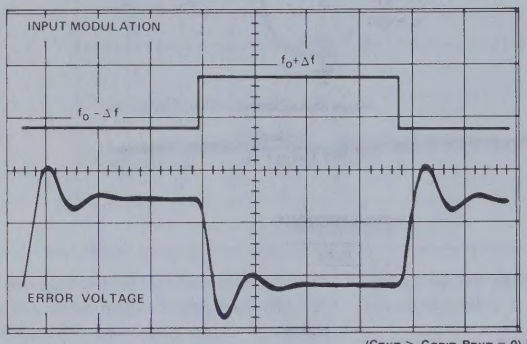


Figure 3.5

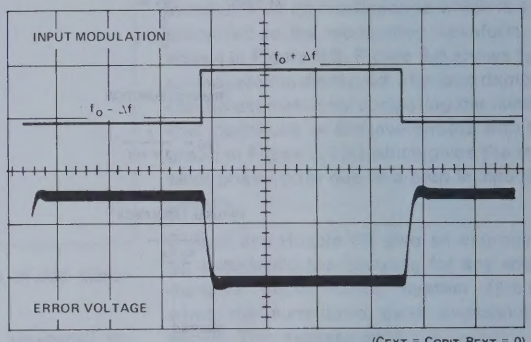
TRANSIENT RESPONSE OF PLL ERROR VOLTAGE TO SQUARE WAVE FREQUENCY MODULATION FOR VARIOUS DAMPING CONDITIONS:

(a) UNDERDAMPED WITH $\zeta \simeq 0.28$



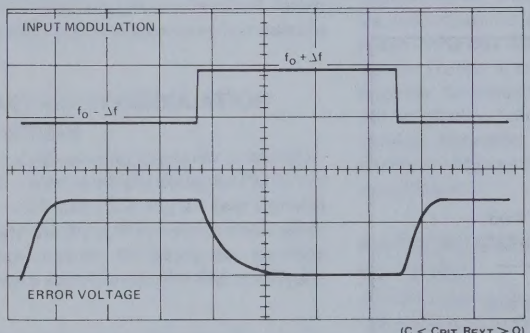
($C_{EXT} > C_{CRIT}$, $R_{EXT} = 0$)

(b) CRITICALLY DAMPED WITH $\zeta \simeq 1.0$



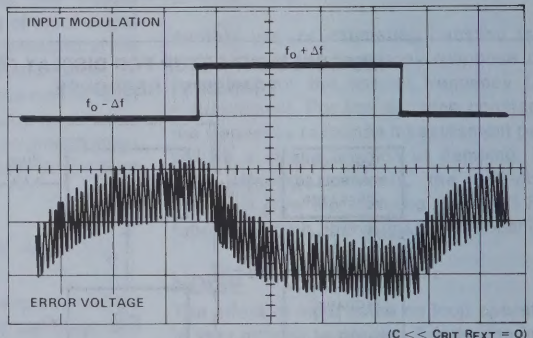
($C_{EXT} = C_{CRIT}$, $R_{EXT} = 0$)

(c) OVERDAMPED WITH $\zeta \simeq 10$



($C < C_{RIT}$, $R_{EXT} > 0$)

(d) HIGHLY OVERDAMPED WITH $\zeta > 10$

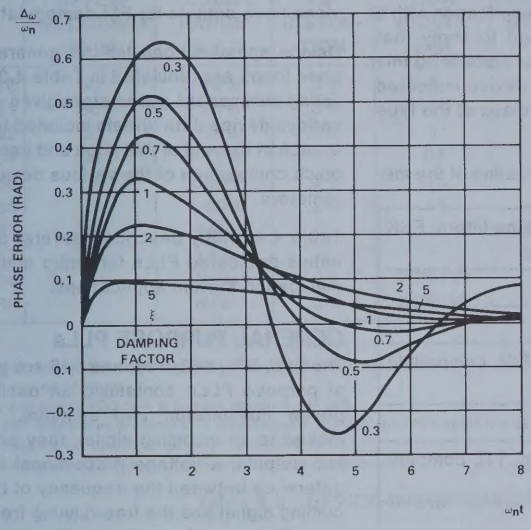


($C << C_{RIT}$, $R_{EXT} = 0$)

Figure 3.6

ESTIMATING THE DAMPING IN A SECOND ORDER PLL

(A) TRANSIENT PHASE ERROR AS AN INDICATION OF DAMPING



(a)

(B) RATIO OF PEAK AMPLITUDE TO LOW FREQUENCY AMPLITUDE OF ERROR VOLTAGE FROM MODULATING FREQUENCY RESPONSE

ζ	PEAK AMPLITUDE / LOW FREQUENCY AMPLITUDE	$\frac{\omega-3db}{\omega_n}$
.3	6.0dB	1.8
.5	3.2dB	2.1
.7	2.2dB	2.5
1.0	1.3dB	4.3
5.0	0.5dB	10

(b)

Figure 3.7

INTRODUCTION

Signetics makes three basic classes of monolithic PLLs: general purpose PLLs, a special purpose PLL for use as a tone decoder, and dedicated PLLs intended for specific audio or communication functions. A *User's Quick Guide* is provided in the following tables which summarize suggested applications, internal features, and device specifications.

Table 4.1 is an applications guide for Signetics general purpose PLLs. While it would be impossible to list every function PLLs are capable of performing, this table identifies principle applications of the various general purpose devices for which they are especially well suited. Furthermore, the identification of a specific application with a certain device is not meant to imply that other PLLs are incapable of performing this function, but only that the device indicated is known to serve a broad class of the type of application cited.

Table 4.2 provides a quick listing of the major internal functional features in the Signetics general purpose PLLs. All PLLs have internal phase comparators, amplifiers, voltage-controlled oscillators, and resistors for the low-pass filter. Also all PLL devices have outputs for FM demodulation.

Device specifications for the general purpose loops are tabulated in Table 4.3. This listing summarizes parameters given on the various device data sheets included for reference at the end of this book and permits a quick comparison of the various device parameters.

Table 4.4 briefly describes several of Signetics dedicated PLLs for audio and communication system applications.

GENERAL PURPOSE PLLs

The 560, 561, 562, 564, and 565 are general purpose PLLs containing an oscillator, phase comparator, and amplifier. When locked to an incoming signal, they provide two outputs: a voltage proportional to the difference between the frequency of the incoming signal and the free-running frequency (FM output), and a square wave oscillator output which, during lock, is equal to the incoming frequency. The 560, 562, and 565 devices are optimized to provide a highly linear frequency-to-voltage transfer characteristic.

The 564 contains additional internal circuitry that makes it particularly attractive for high speed (up to 50MHz) FSK and modem

NE560	FM demodulation, data synchronizer, signal reconstitution, tracking filters, FSK receivers, modems.
NE561	AM demodulation.
NE562	Frequency synthesis plus all NE560 functions[1]
NE564	High-speed modems, FSK transmitters and receivers, TTL and ECL compatible outputs.
NE565	Low frequency FSK.
NE567[2]	Touch-tone® decoder, AM demodulation, communications paging, TTL compatible output.
NE566[3]	FSK transmitters, signal generators.

NOTES

1. The NE562 is identical to the NE560 except that the loop is open between the VCO output and the phase comparator input.
2. Although the NE567 is a special purpose PLL intended for tone decoder applications, it is included here since it serves many general purpose applications related to tone decoding.
3. While the NE566 is not a PLL but a precision voltage-controlled waveform generator, it is included here since it lends itself well to general purpose PLL applications.

Table 4.1 APPLICATIONS GUIDE FOR SIGNETICS GENERAL PURPOSE PLLs

	INTERNAL LOOP CONNECTIONS	FINE-TUNE ADJUST OF f_o WITH RESISTANCE	DIFFERENTIAL VCO OUTPUTS AVAILABLE	OFFSET CONTROL FOR SHIFTING f_o	PHASE COMPARATOR INPUTS AVAILABLE	FILTER CONNECTIONS FOR FM DE-EMPHASIS	OPEN-COLLECTOR OUTPUT	INPUT SIGNAL LIMITER	SCHMITT TRIGGER WITH ADJUSTABLE HYSTERESIS
NE560	Closed[1]	Yes	Yes	Yes	1 Diff. Pair	Yes	No	No	No
NE561	Closed[2]	Yes	No	Yes	1 Diff. FM Pair 1 Single AM	Yes	No	No	No
NE562	Open[3]	Yes	Yes	Yes	2 Diff. Pairs	Yes	No	No	No
NE564	Open[3]	No	No	No	1 Single FM	No	Yes	Yes	Yes
NE565	Open[3]	Yes	Yes	Yes	1 Diff. Pair	No	No	No	No
NE567	Closed[2]	Yes	Yes	No	1 Common Single AM-FM	No	Yes	No	No
NE566	N/A	Yes	No	Yes	N/A	N/A	No	N/A	N/A

NOTES

1. Internal connections are provided between phase comparator, low-pass filter, amplifier, and VCO.
2. Internal connections are provided between phase comparator, low-pass filter, amplifier and VCO. Internal connections also provided for the internal quadrature phase detector.
3. Loop is open between VCO output and phase comparator input.

Table 4.2 INTERNAL FUNCTIONAL FEATURES IN SIGNETICS GENERAL PURPOSE PLLs

	UPPER FREQUENCY (MHz)	MAXIMUM LOCK RANGE (% f_o)	FM DISTORTION	OUTPUT SWING ±5% DEVIATION (VOLTS p-p)	CENTER FREQUENCY STABILITY (PPM/°C)	FREQUENCY DRIFT/W SUPPLY VOLTAGE (%/V)	INPUT RESISTANCE (Ω)	AM OUTPUT AVAILABLE	TYPICAL SUPPLY CURRENT (mA)	SUPPLY VOLTAGE RANGE (VOLTS)
NE560	30	±15%[1]	.3%	1	±600	.3	2K[2]	No	9	+16 to +26
NE561	30	±15%[1]	.3%	1	±600	.3	2K[2]	Yes	10	+16 to +26
NE562	30	±15%[1]	.5%	1	±600	.3	2K[2]	No	12	+16 to +30
NE564	50	±12%[1]	[5]	.07	±400	3	>50K	No	60	+5 to +12
NE565	.5	±60%	.2%	.15	±200	.2	10K	No	8	±6 to ±12
SE565	.5	±60%	.2%	.15	±100	.1	10K	No	8	±6 to ±12
NE567	.5	14%	[4]	[4]	35 ±60	.7	20K[2]	Yes[4]	7	+4.75 to +9
SE567	.5	14%	[4]	[4]	35 ±60	.5	20K[2]	Yes[4]	6	+4.75 to +9
NE566	1	N/A	.2%	70%/V[3]	±200	2	N/A	N/A	7	+12 to +26
SE566	1	N/A	.2%	70%/V[3]	±100	1	N/A	N/A	7	+12 to +26

NOTES

1. Considerably larger ranges are possible with external control current.
2. Input biased internally.
3. Figure shown is VCO gain in percent deviation per volt.
4. The 567 is designed primarily as a tone decoder. The AM and FM outputs are available, but are not optimized for linear demodulation.
5. FM output is available but not optimized for linear demodulation.

Table 4.3 DEVICE SPECIFICATIONS FOR SIGNETICS GENERAL PURPOSE PLLs

applications. In addition to a VCO, phase comparator, and amplifier, the 564 contains an input signal limiter, a dc retriever, and a Schmitt trigger with adjustable hysteresis. Also the 564 contains level translation circuits which make the limiter input, the VCO and Schmitt trigger outputs compatible for direct interfacing with the TLL circuits.

The 561 contains a complete PLL as those above, plus an additional multiplier or quadrature phase detector that is required for AM demodulation. In addition to the standard FM and oscillator outputs, the 561 also provides an output voltage which is proportional to the amplitude of the incoming signal (AM output). The 561 is optimized for highly linear FM and AM demodulation.

The 566 is not a phase lock loop, but a precision voltage-controllable waveform generator derived from the oscillator of the 565 general purpose loop. Because of its similarity to the 565 and because it lends itself well to use in, and in conjunction with, phase locked loops, it has been included among the general purpose PLLs.

CIRCUIT DESCRIPTIONS OF THE 560, 561, AND 562 PLLs

The 560, 561 and 562 phase locked loops are all derived from the same monolithic die with different metal interconnections. Each device contains the same VCO, phase comparator, and voltage regulator stage and, hence, the basic loop parameters are the same for all three circuits.

The 560 is the most fundamental of the three circuits, having a block diagram equivalent to that shown in Figure 4.1. The actual circuit diagram is shown in Figure 4.2.

The VCO is a high frequency emitter-coupled multivibrator formed by transistors Q11-Q14. It operates from a regulated 7.7V supply formed by the series combination of the 6.3V Zener diode CR_1 (a reverse-biased base-emitter junction) and the 14V regulated supply. The VCO frequency is thus immune to supply voltage variations. Four constant current sources formed by Q20, Q21, Q23, Q24, and biased by CR_6 and CR_7 supply operating current for the VCO. Voltage control of the frequency is achieved by a differential amplifier, Q22 and Q25. As the base voltage of Q22 increases with respect to the base voltage of Q25, additional current is drawn from the emitters of Q12 and Q13, increasing the charge and discharge current of the timing capacitor C_o. Since the VCO frequency is linearly proportional to the timing capacitor current, the VCO frequency increases. Reducing the base voltage of Q22 with respect to Q25 similarly reduces the VCO frequency. Two Zener diodes and two transistors, CR_4, CR_5, Q5 and Q10, respectively, provide level shifting which allows the VCO to be driven by the outputs of the phase comparator.

The phase comparator is a doubly-balanced multiplier formed by transistors Q6-Q9, Q17 and Q18. One signal input is made to the lower stage, biased at about 4V by means of 2kΩ base resistors. The upper stage is biased and driven directly by the VCO output taken from the collector resistors of Q12 and Q13. A differential output signal is available between the collectors of Q6 (and Q8) and Q7 (and Q9). An external network, together with the 6kΩ collector resistors, comprises the low pass filter. The phase comparator is operated from regulated 14V appearing at the emitter of Q27. A resistor in the collector of Q25 can be shunted with an external capacitor to form a de-emphasis filter. The de-emphasized signal is buffered by emitter follower Q19 before being brought out.

The *TRACK RANGE* input, pin 7 on all three loops, allows the designer to control the total current flowing through the frequency controlling differential amplifier Q22, Q25. This is done by controlling the effective emitter resistance of Q29, the current source for Q22, Q25. Current may be added or subtracted at pin 7 to, respectively, reduce or increase the tracking range.

The 561, shown in Figure 4.3, contains all of the circuitry of the 560 and in addition, has a quadrature phase detector. This enables it to be used as a synchronous AM detector. The quadrature phase detector consists of transistors Q1-Q4 and Q15, Q16 which are biased and driven in the same manner as the loop phase comparator. However, the quadrature detector input is single ended

DEVICE	PROCESS TECHNOLOGY	FEATURES AND APPLICATIONS
8X08 AM/FM Frequency Synthesizer	Combination bipolar and MOS	Uses digital PLL techniques to synthesize AM and FM local oscillator frequencies. Capable of digitally programming 200 AM channels with 10kHz spacing and 2000 FM channels with 100kHz spacing. Operates on a single 5 volt supply with input frequencies up to 80MHz. Requires only one crystal, one capacitor, and two resistors as external components. Easily adapted for electronically scanning both AM and FM bands, reversing scan directions, and storing up to 10 station locations in memory.
μA758 FM Stereo Multiplexer Decoder	Bipolar	Decodes FM stereo multiplex signal into left and right audio channels while suppressing Subsidiary Carrier Authorization (SCA) information that may be present in the input signal. Internal functions provide for automatic monaural-stereo mode switching and drive capability for an external lamp to indicate stereo mode operation. Requires no external tuning coils and only one potentiometer adjustment for complete alignment.
CD4-392 CD-4 Quadraphonic Demodulator	Bipolar	Demodulates CD-4 records into four separate channels while maintaining compatibility for standard monaural and stereo recordings. Monolithic device contains both a PLL carrier recovery system and an audio processing system with performance levels consistent with audiophile standards. PLL carrier recovery system consists of a high gain (60dB) limiting amplifier, two analog multipliers acting as phase and carrier amplitude detectors, and a current controlled oscillator with quadrature phase outputs. PLL techniques are used to demodulate wide band FM signals without critical alignment of reactive components while maintaining low distortion. Also the AFC action or memory of the PLL minimizes audio noise due to carrier drop-outs on worn records.
CG477 CD-4 Quadraphonic Demodulator	Bipolar	Demodulates CD-4 records into four separate channels with a single IC. Maintains compatibility for standard monaural and stero recordings. Circuit contains a low noise preamplifier, a PLL demodulator, a complete 2-band audio expansion system, and the complete audio processing circuitry required for CD-4 demodulation.

Table 4.4 SIGNETICS SPECIAL PURPOSE PLLs

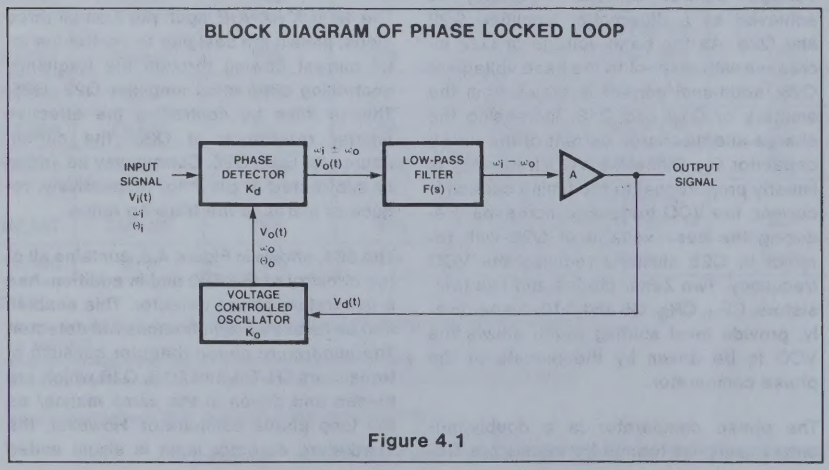


Figure 4.1

CIRCUIT DIAGRAM OF 560

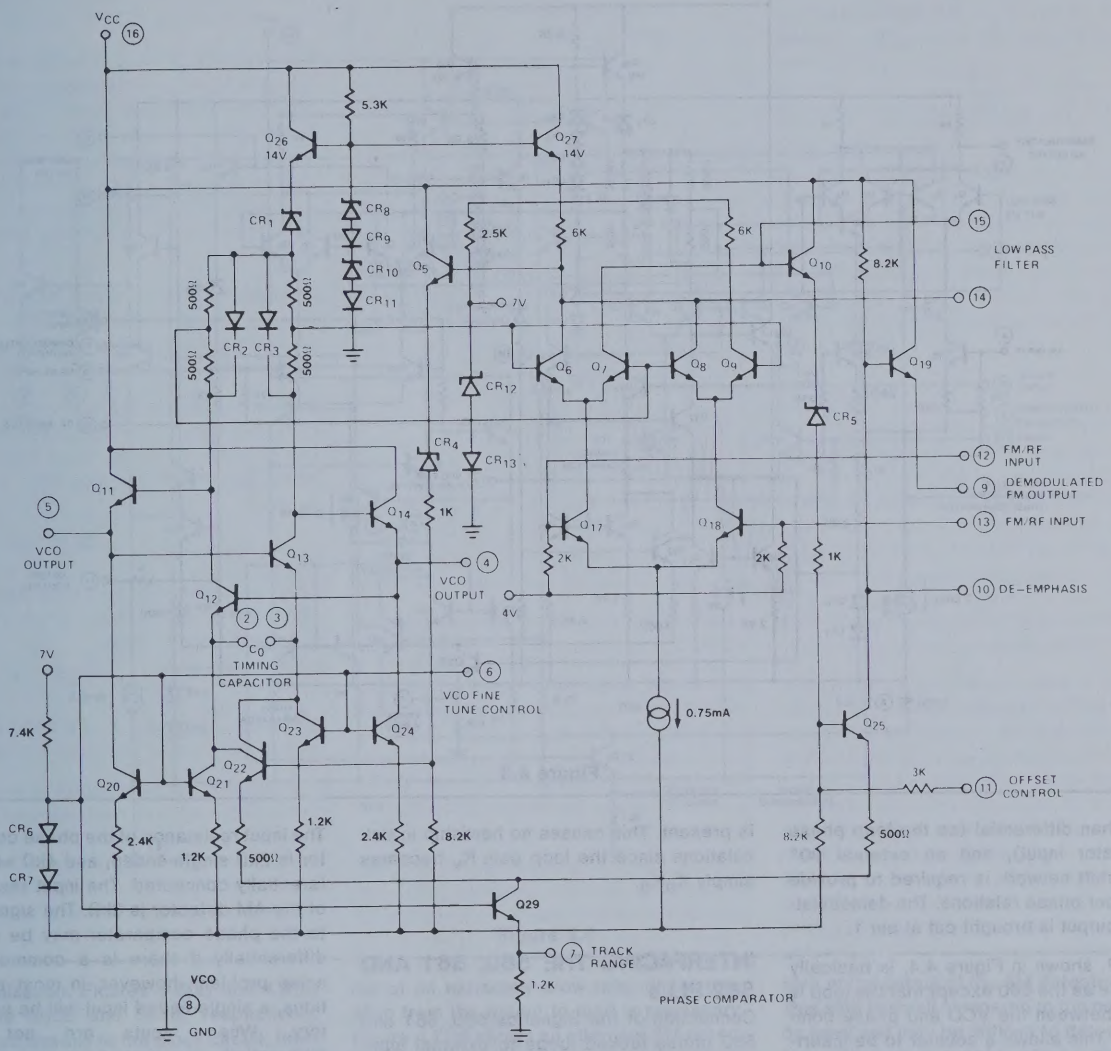


Figure 4.2

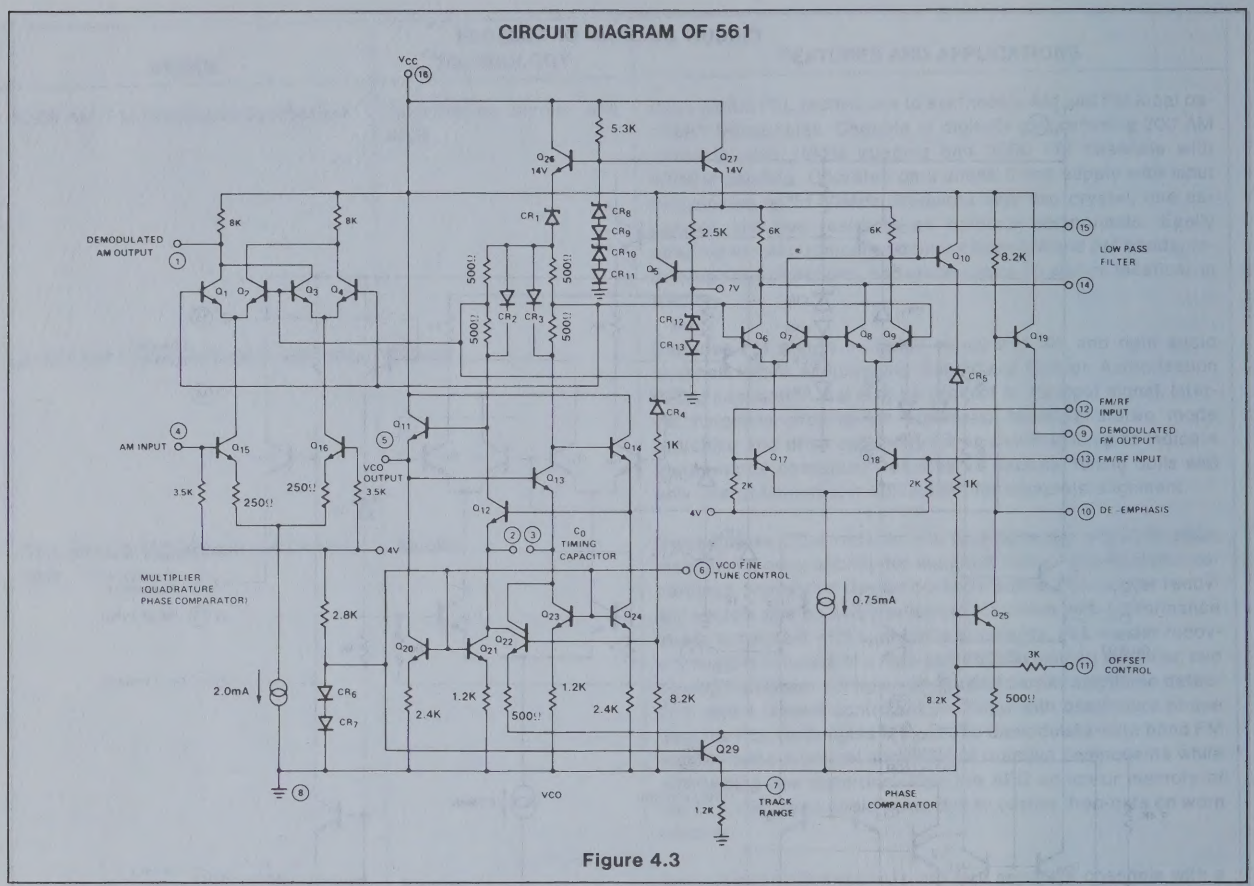


Figure 4.3

rather than differential (as the loop phase comparator input), and an external 90° phase shift network is required to provide the proper phase relations. The demodulated AM output is brought out at pin 1.

The 562, shown in Figure 4.4, is basically the same as the 560 except that the loop is broken between the VCO and phase comparator. This allows a counter to be inserted in the loop for frequency multiplication applications. Transistors Q1-Q4 provide low impedance differential VCO outputs (pins 3 and 4), and the upper stage phase comparator inputs are brought out of the package (pins 2 and 15). A bias voltage is brought out through pin 1 to provide a convenient bias level for the upper stage of the phase comparator.

Figure 4.5 shows the conversion constants (K_o, K_d) for the 560, 561, and 562 Signetics loops. The values given are for the standard connection with no gain reduction or tracking adjustment components connected. The dc amplifier gain A has been included in either the K_o or K_d value, depending on which side of the low pass filter terminals the gain is present. This causes no hardship in calculations since the loop gain K_v becomes simply K_oK_d.

INTERFACING THE 560, 561 AND 562 PLLs

Connection of the Signetics 560, 561 and 562 phase locked loops to external input and output circuitry is readily accomplished; however, as with any electrical system, there are voltage, current and impedance limitations that must be considered.

The inputs of the phase comparators in the 560, 561 and 562 and the AM detector in the 561 are biased internally from a 4V supply; therefore, the input signals must be capacitively coupled to the PLL to avoid interfering with this bias. These coupling capacitors should be selected to give negligible phase shift at the input frequency and impedance of the PLL. (The capacitive impedance at the operating frequency should be as small as possible, compared to the input resistance of the PLL.)

The input resistance of the phase comparator is 2kΩ single-ended, and 4kΩ when differentially connected. The input resistance of the AM detector is 3kΩ. The signal input to the phase comparator may be applied differentially if there is a common-mode noise problem; however, in most applications, a single-ended input will be satisfactory. When inputs are not used differentially, the unused input may be accoupled to ground to double the phase comparator gain at low input amplitudes.

The amplitude of the input signal should be adjusted to give optimum results with the PLL. Signals of less than 0.2mV rms may have an unsatisfactory signal-to-noise ratio; signals exceeding 25mV rms will have reduced AM rejection (less than 30dB). The AM detector will handle input signals up to 200mV peak-to-peak without excessive distortion, and will handle up to 2V peak-to-peak where distortion is not a factor.

Interfacing of the available outputs is best described by referring to the following diagrams. Figure 4.6 shows the PLL VCO output as a clock circuit for logic pulse

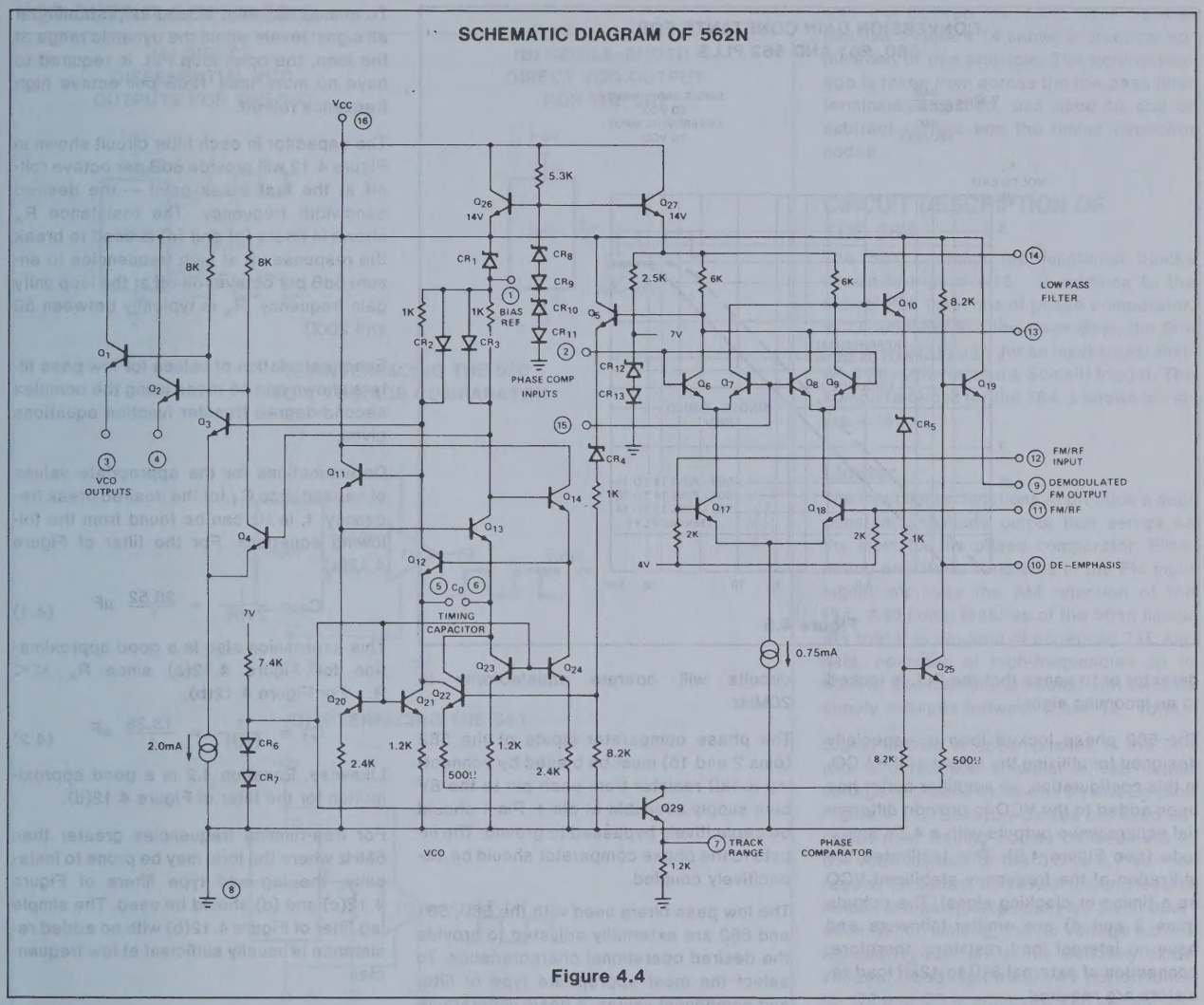


Figure 4.4

synchronization. Figures 4.6(a) and 4.6(b) show the 560B and 561B, respectively, connected directly to the clock circuit; however, this configuration may be limited by low voltage and the possibility of too large a capacitive load swamping the oscillator. Figures 4.6(c) and 4.6(d) show the PLL clock output for the 560B and 561B respectively, using the μA710 Voltage Comparator as a buffer amplifier to provide an output voltage swing suitable for driving logic circuits. The power supply for circuits utilizing the μA710 is split (+12V and −6V dc).

In Figure 4.7(a) the 560 is a FM demodulator used for the detection of audio information on frequency modulated carriers. Since the lower frequency limit of this type of information is approximately 1.0Hz, capacitive coupling may be used. However, in some applications where carrier shifts occur at an extremely slow rate, direct coupling from the output to load is necessary. Figure 4.7(b) shows an alternate FM detector output configuration which should be used if a different output is desirable. In this case, the output is removed at pins 14 and 15. These pins are the terminals of the low pass filter and are in the line containing the demodulated signal. The signal level (single-ended) is about one-sixth of that at pin 9 so that additional amplification may be required. Additional receiving modes are illustrated in Figure 4.8 for the 561 only. Figure 4.8(a) shows the 561 output when used as an AM detector; note the straight capacitive coupling. Figure 4.8(b) shows the 561 used as a continuous wave detector. Since this version of the circuit is for the detection of CW or AM signals, external circuitry must be incorporated for use with CW inputs. With a CW input applied, there will be a dc shift at the output of the AM detector, pin 1. This shift is small compared to the no-signal dc level and may be difficult to detect in relation to power supply voltage changes. Therefore, a reference must be generated to track any power supply voltage variations and to compensate for internal PLL thermal drift. This is best accomplished by simulating a portion of the PLL internal structure. The 2N3565 npn transistor is used as a constant-current source. Its reference voltage is obtained from an internal PLL bias source at pins 12 and 13, with the current level established by the 6.8kΩ resistor. The 6.2kΩ resistor and the 2.5kΩ potentiometer simulate the PLL output resistance. The differential amplifier, composed of the two 2N3638 pnp transistors, amplifies the dc output and allows it to drive a npn transistor referenced to ground. This type of circuit may also be used as a tone

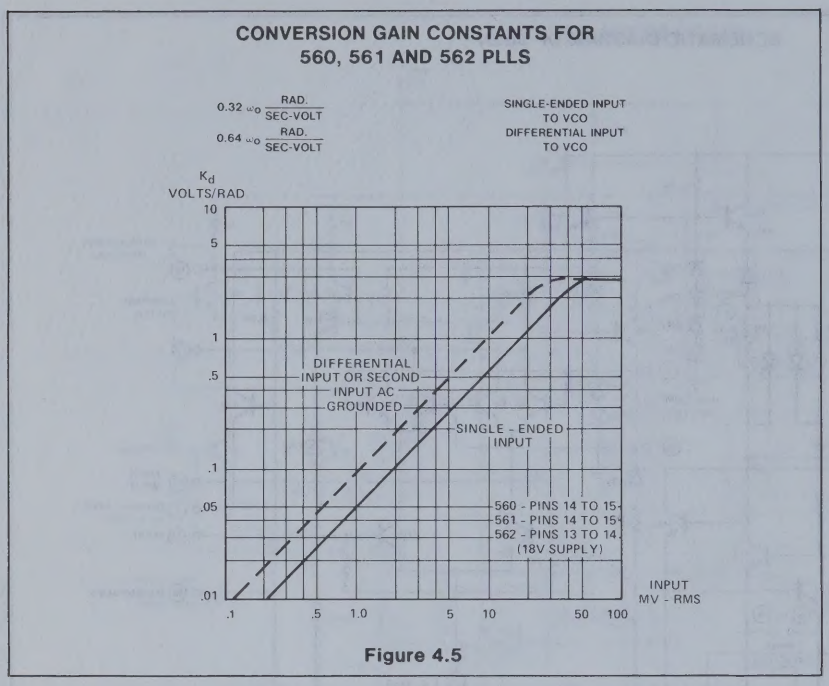


Figure 4.5

detector or to sense that the PLL is locked to an incoming signal.

The 562 phase locked loop is especially designed for utilizing the output of the VCO. In this configuration, an amplifier-buffer has been added to the VCO to provide differential square wave outputs with a 4.5V amplitude (see Figure 4.9). This facilitates the utilization of the frequency stabilized VCO as a timing or clocking signal. The outputs (pins 3 and 4) are emitter-followers and have no internal load resistors; therefore, connection of external 3kΩ to 12kΩ load resistors are required.

It is essential that the resistance from each pin to ground be equal in order to maintain output waveform symmetry and to minimize frequency drift. When connecting the VCO output to the phase comparator (pins 3 to 2 for single-ended connection), capacitive coupling should be used. If a signal exceeding 2V is to be applied, a 1kΩ resistor should be placed in series with the coupling capacitor. This resistor may be part of the load resistance of 12kΩ, by using two resistors (1kΩ and 11kΩ) to form the VCO load, as shown in Figure 4.10.

The output from the VCO is a minimum of 3V peak-to-peak, but has an average level of 12V dc; that is, it oscillates from 10.5 to 13.5V. To utilize this output with logic circuits, some means of voltage level shifting must be used. Figure 4.11 shows two methods of accomplishing level shifting. These circuits will operate satisfactorily to 20MHz.

The phase comparator inputs of the 562 (pins 2 and 15) must be biased by connecting a 1kΩ resistor from each pin to the 8V bias supply available at pin 1. Pin 1 should be capacitively bypassed to ground. The inputs to the phase comparator should be capacitively coupled.

The low pass filters used with the 560, 561 and 562 are externally adjusted to provide the desired operational characteristics. To select the most appropriate type of filter and component values, a basic understanding of filter operation is required.

An FM signal to be demodulated is matched in the phase comparator with the voltage controlled oscillator signal, which is tuned to the FM center frequency. Any resulting phase difference between these two signals is the demodulated FM signal. This demodulated signal is normally at frequencies between dc and upper audio frequencies.

The choice of low pass filter response gives a degree of design freedom in determining the capture range or selectivity of the loop. The attenuation of the high frequency error components at the output of the phase comparator enhances the interference rejection characteristics of the loop. The filter also provides a short-term memory for the PLL that ensures rapid recapture of the signal if the system is thrown out of lock due to a noise transient.

To ensure absolute closed loop stability at all signal levels within the dynamic range of the loop, the open loop PLL is required to have no more than 12dB per octave high frequency roll-off.

The capacitor in each filter circuit shown in Figure 4.12 will provide 6dB per octave roll-off at the first break point — the desired bandwidth frequency. The resistance R_X shown in filters (c) and (d) is used to break the response up at high frequencies to ensure 6dB per octave roll-off at the loop unity gain frequency. R_X is typically between 50 and 200Ω.

Exact calculation of values for low pass filters shown can be made using the complex second-degree transfer function equations given.

Determinations for the appropriate values of capacitance C_1 for the desired break frequency, f, in Hz can be found from the following equations. For the filter of Figure 4.12(a)

$$C_1 = \frac{1}{2\pi fR} = \frac{26.52}{f}\ \mu F \qquad (4.1)$$

This expression also is a good approximation for Figure 4.12(c) since $R_X << R$. For Figure 4.12(b),

$$C_1 = \frac{1}{4\pi fR} = \frac{13.26}{f}\ \mu F \qquad (4.2)$$

Likewise, Equation 4.2 is a good approximation for the filter of Figure 4.12(d).

For free-running frequencies greater than 5MHz where the loop may be prone to instability, the lag-lead type filters of Figure 4.12(c) and (d) should be used. The simple lag filter of Figure 4.12(b) with no added resistance is usually sufficient at low frequencies.

LOW PASS FILTER CONNECTIONS

The frequency range of the 560, 561 and 562 phase locked loops may be extended to 60MHz by the addition of two 10kΩ resistors from the timing capacitor terminals to the negative power supply (ground in this case) as shown in Figure 4.13. The inclusion of a 5kΩ potentiometer between these 10kΩ resistors and the negative supply provides a simple method of fine tuning.

The internal control voltage feedback loop can also be easily broken on the 560, 561 and 562. The key in this case is to bias the range control terminal (pin 7) to +2V which turns off the internal controlled current source. Now the phase comparator output voltage will have no effect on the charging current which sets the VCO frequency. Then an external feedback loop can be built

VCO OUTPUT INTERFACING:

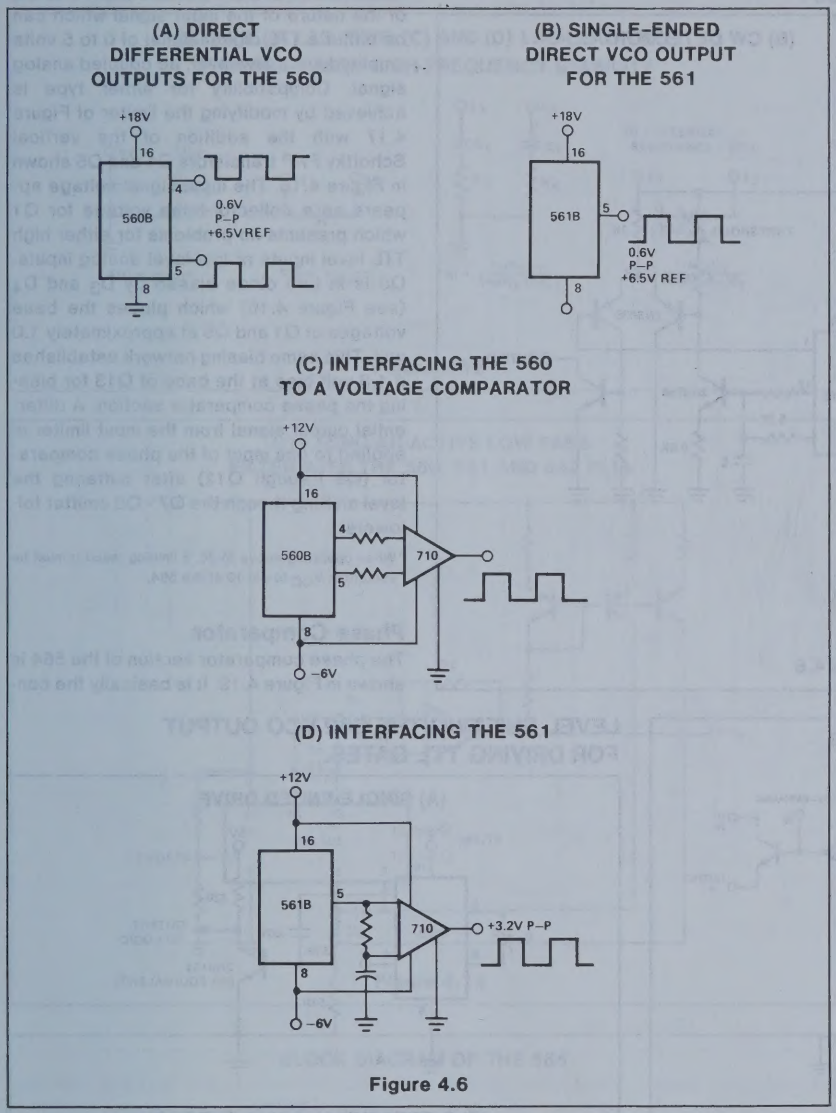


Figure 4.6

FM DETECTOR INTERFACING

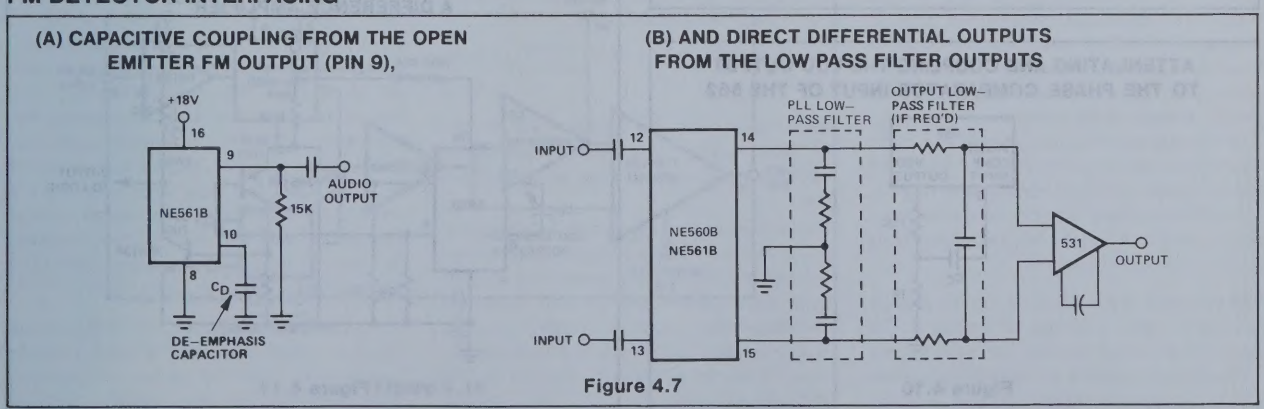


Figure 4.7

with the desired low pass filter transfer function. Figure 4.14 shows a practical application of this principle. The control voltage is taken from across the low pass filter terminals, amplified, and used to add or subtract current into the timing capacitor nodes.

CIRCUIT DESCRIPTION OF THE 564

The 564 contains the functional blocks shown in Figure 4.15. In addition to the normal PLL functions of phase comparator, VCO, amplifier and low-pass filter, the 564 has internal circuitry for an input signal limiter, a dc retriever, and a Schmitt trigger. The complete circuit for the 564 is shown in Figure 4.16.

Limiter

The input limiter functions to produce a near constant amplitude output that serves as the input for the phase comparator. Eliminating amplitude variations in the FM input signal improves the AM rejection of the PLL. Additional features of the 564s limiter are that it is capable of accepting TTL signals, operates at high-frequencies up to 50MHz, and remains functional with variable supply voltages between 5 and 12* volts.

Signal limiting is accomplished in the 564 with a differential amplifier whose output voltage is clipped by diodes D_1 and D_2 (see Figure 4.17). Schottky diodes are used because their limiting occurs between 0.3 to 0.4 volts instead of the 0.6 to 0.7 volt for regular IC diodes. This lower limiting level is helpful in biasing, especially for 5 volt operation. When limiting, the dc voltage across R_2 and R_3 remains at the Schottky diode voltage. Good high-frequency performance for Q2 and Q3 is achieved with current levels in the low mA range. Current-source biasing is established via the current mirror of D_5 and Q4 (See Figure 4.16).

DETECTOR INTERFACING WITH THE 561

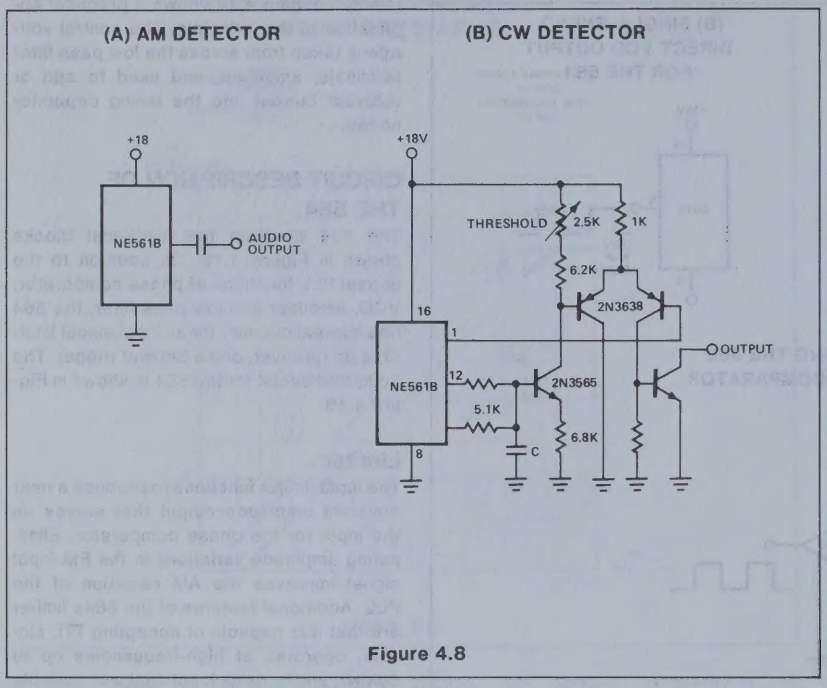


Figure 4.8

Base biasing for Q3 is of concern because of the nature of the input signal which can be either a TTL digital signal of 0 to 5 volts amplitude or a low-level, ac coupled analog signal. Compatibility for either type is achieved by modifying the limiter of Figure 4.17 with the addition of the vertical Schottky PNP transistors Q1 and Q5 shown in Figure 4.18. The input signal voltage appears as a collector-base voltage for Q1 which presents no problems for either high TTL level inputs or low-level analog inputs. Q5 is in turn diode biased by D_3 and D_4 (see Figure 4.16) which places the base voltages of Q1 and Q5 at approximately 1.0 volt. This same biasing network establishes a 1.3 volt bias at the base of Q13 for biasing the phase comparator section. A differential output signal from the input limiter is applied to one input of the phase comparator (Q9 through Q12) after buffering the level shifting though the Q7 - Q8 emitter followers.

*When operating above 5Vdc, a limiting resistor must be used from V_{CC} to pin 10 of the 564.

Phase Comparator

The phase comparator section of the 564 is shown in Figure 4.19. It is basically the con-

BLOCK DIAGRAM OF 562

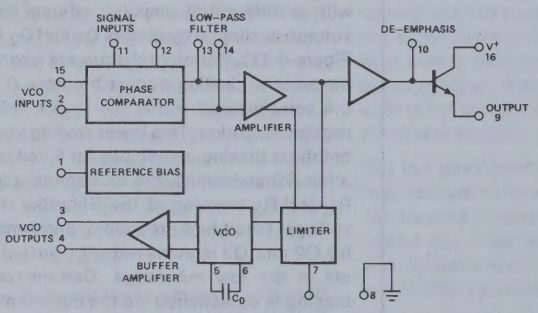


Figure 4.9

ATTENUATING AND COUPLING THE VCO OUTPUT TO THE PHASE COMPARATOR INPUT OF THE 562

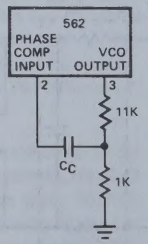


Figure 4.10

LEVEL SHIFTING THE 562 VCO OUTPUT FOR DRIVING TTL GATES.

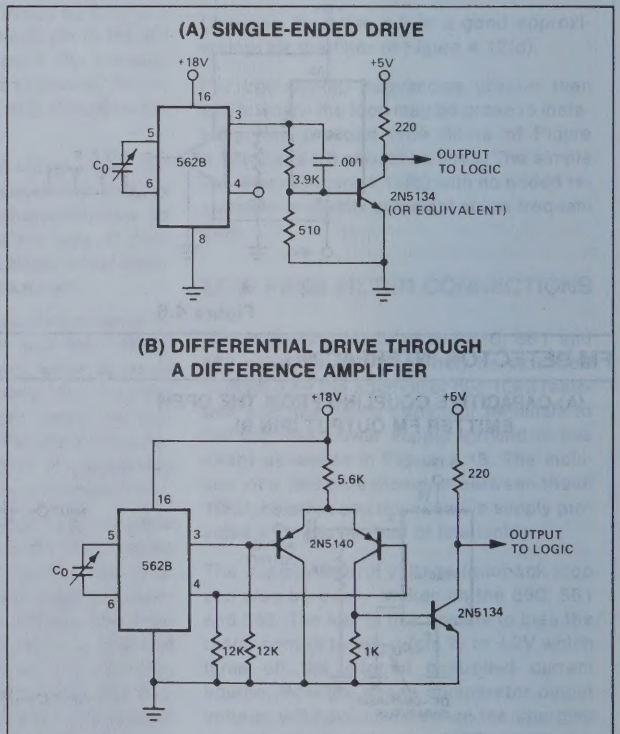


Figure 4.11

LOW PASS FILTER CONNECTIONS

(A) AND (B) LAG TYPE; (C) AND (D) LAG-LEAD TYPE FOR INCREASED HIGH-FREQUENCY STABILITY

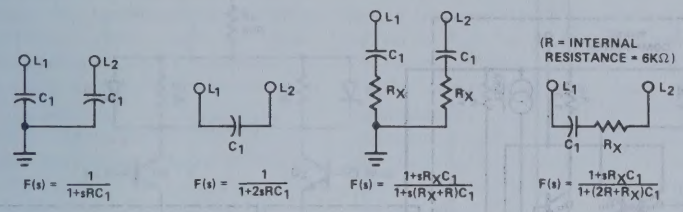


Figure 4.12

CONNECTIONS FOR EXTENDING THE OPERATING FREQUENCY TO 60 MHz

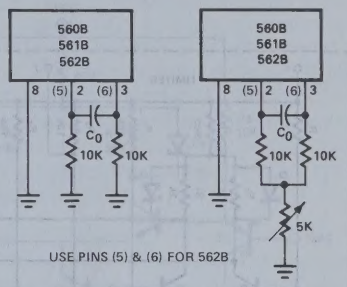


Figure 4.13

UTILIZING AN ACTIVE LOW PASS FILTER WITH THE 560, 561 AND 562 PLLs

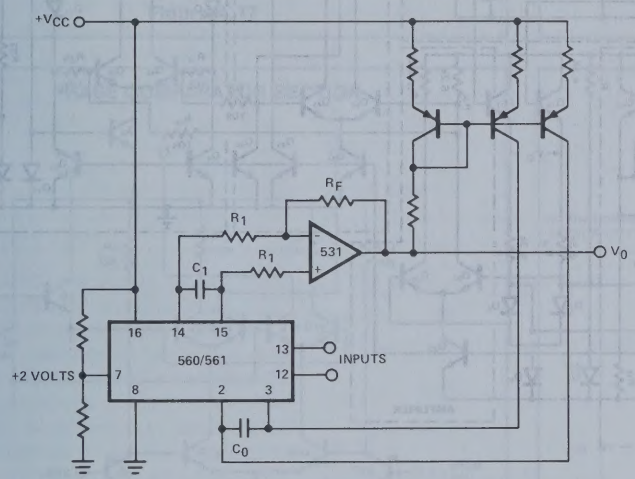


Figure 4.14

BLOCK DIAGRAM OF THE 564

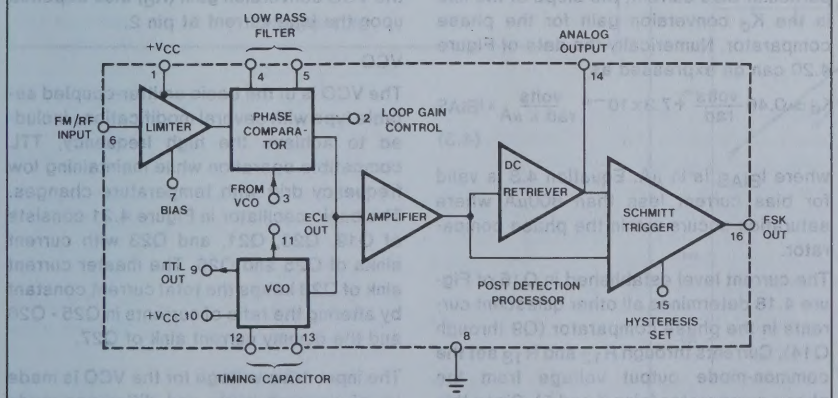


Figure 4.15

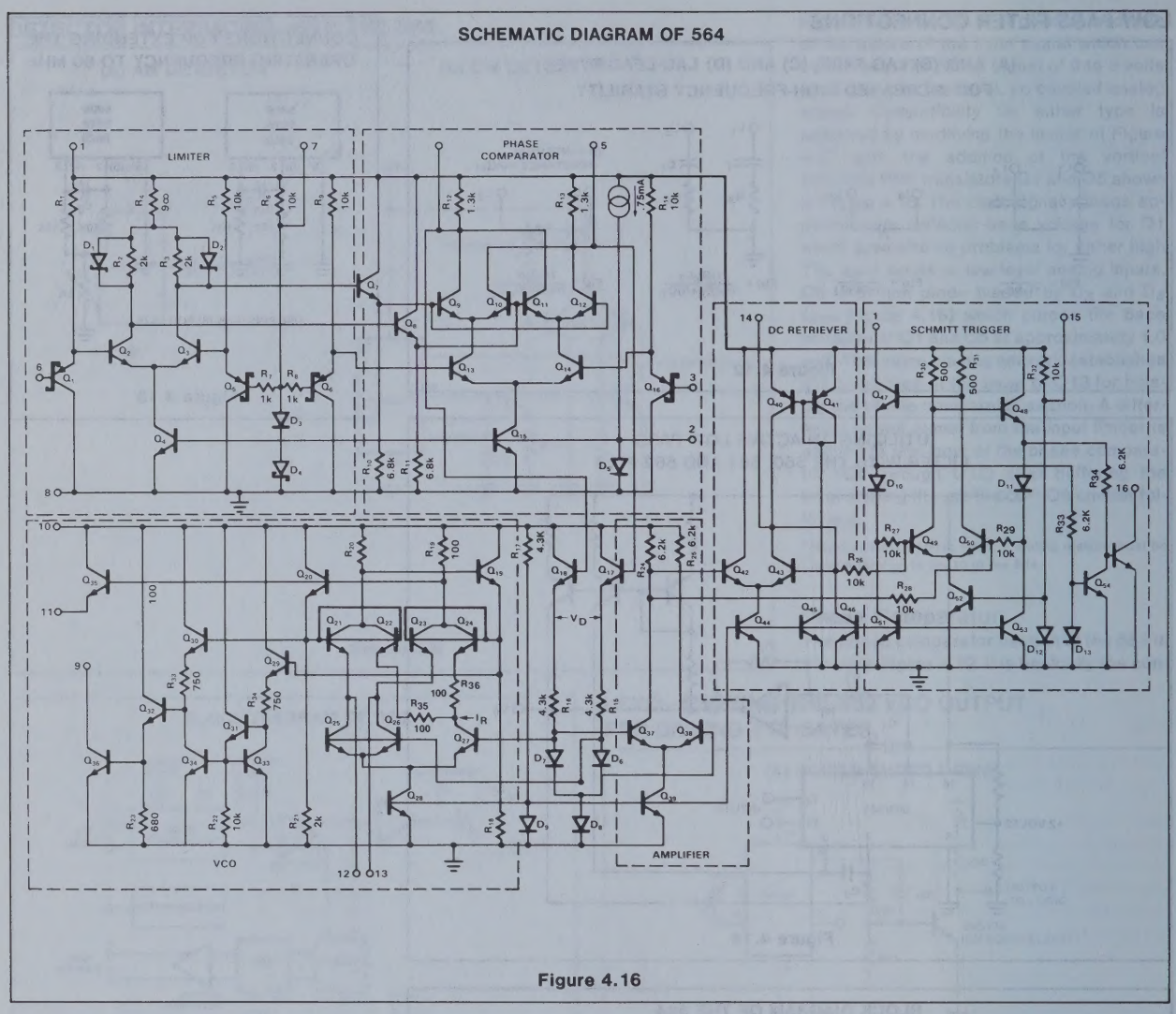


Figure 4.16

ventional, double-balanced mixer commonly used in PLL circuits with a few exceptions. The transconductance, g_m, for the Q13 - Q14 differential amplifier is directly proportional to the mirror current in Q15. Thus by externally sinking or sourcing current at pin 2, g_m can be changed to alter the phase comparators conversion gain, K_d. The nominal current injected into this node by the internal current source is 0.75mA for 5 volt operation. If this current is externally removed by gating, the phase comparator can be disabled and the VCO will operate at its free-running frequency.

The variation of K_d with bias current at pin 2 is shown in the experimental results of Figure 4.20. Note the inherent 90° phase error in the loop produces an approximate zero phase comparator output voltage. For any particular bias current, the slope of the line is the K_d conversion gain for the phase comparator. Numerically the data of Figure 4.20 can be expressed as

$$K_d \simeq 0.46 \frac{\text{volts}}{\text{rad}} + 7.3 \times 10^{-4} \frac{\text{volts}}{\text{rad} \times \mu A} \times I_{BIAS} \quad (4.3)$$

where I_{BIAS} is in μA. Equation 4.3 is valid for bias current less than 800μA where saturation occurs within the phase comparator.

The current level established in Q15 of Figure 4.18 determines all other quiescent currents in the phase comparator (Q9 through Q14). Currents through R_{12} and R_{13} set the common-mode output voltage from the phase comparator (pins 4 and 5). Since this common-mode voltage is applied to the VCO to establish its quiescent currents, the VCO conversion gain (K_O) also depends upon the bias current at pin 2.

VCO

The VCO is of the basic emitter-coupled astable type with several modifications included to achieve the high frequency, TTL compatible operation while maintaining low frequency drift with temperature changes. The basic oscillator in Figure 4.21 consists of Q19, Q20, Q21, and Q23 with current sinks of Q25 and Q26. The master current sink of Q28 keeps the total current constant by altering the ratio of currents in Q25 - Q26 and the dummy current sink of Q27.

The input drive voltage for the VCO is made up of common-mode and difference-mode components from the phase comparator. After buffering the level shifting through

BASIC LIMITER STAGE

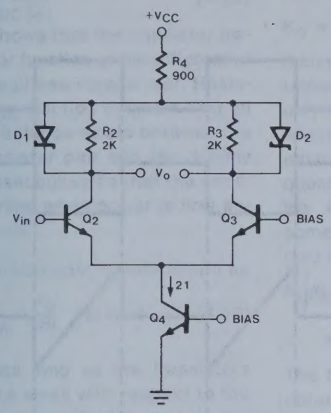


Figure 4.17

LIMITER STAGE WITH INPUT BUFFERING

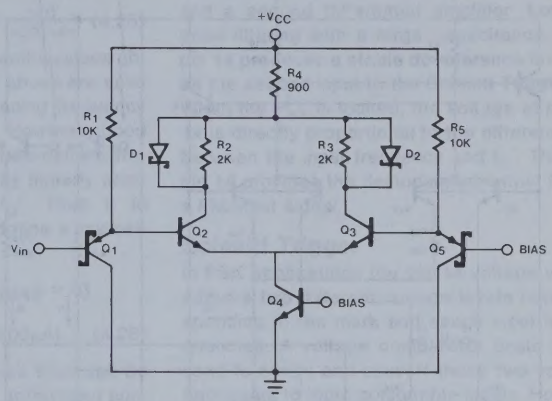


Figure 4.18

PHASE COMPARATOR SECTION

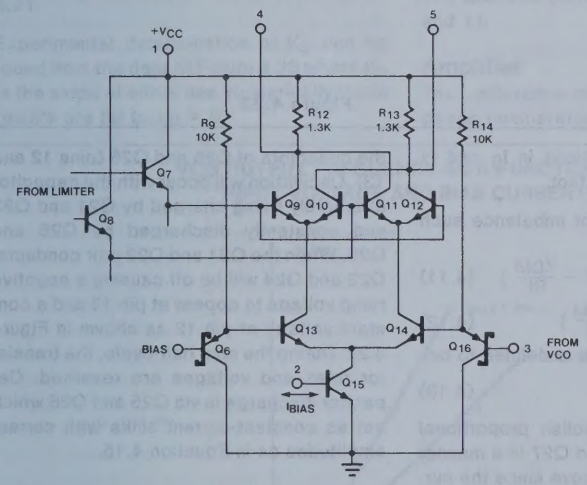


Figure 4.19

VARIATION OF THE PHASE COMPARATOR'S OUTPUT VOLTAGE VERSUS PHASE ERROR AND BIAS CURRENT

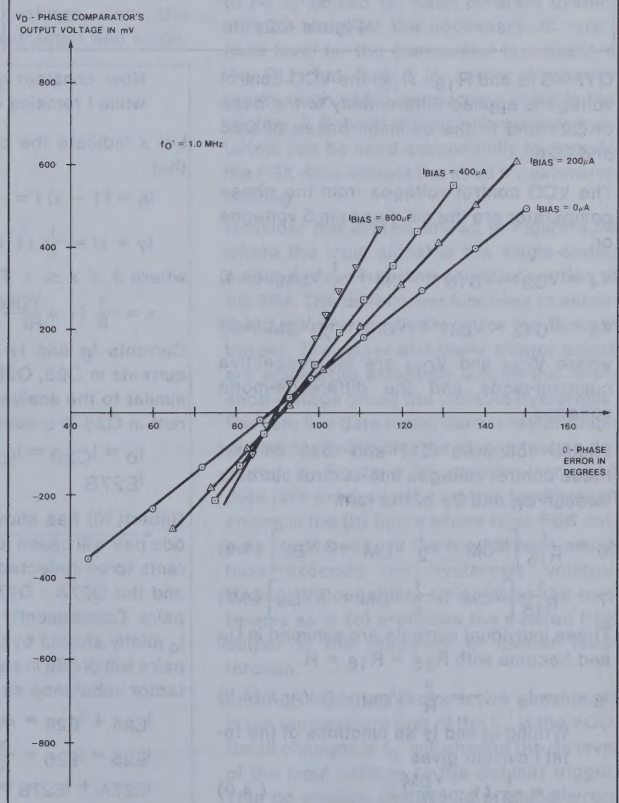


Figure 4.20

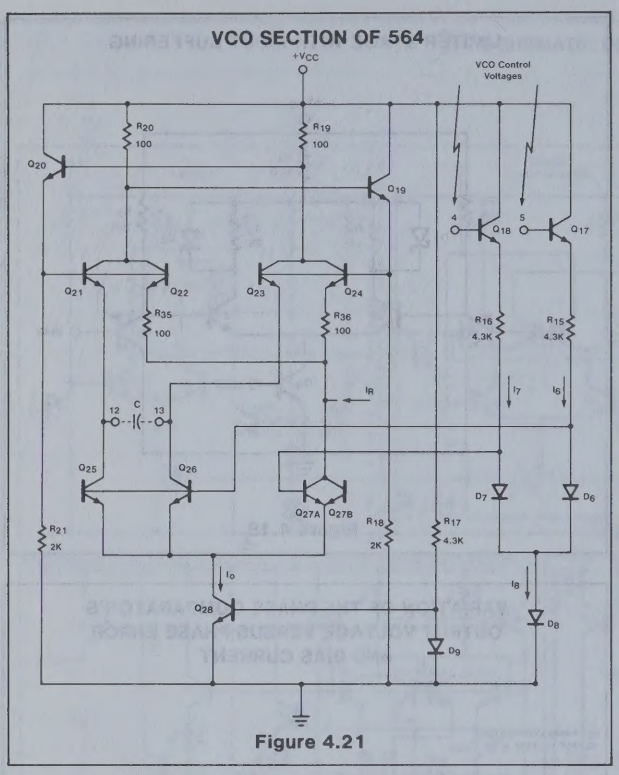


Figure 4.21

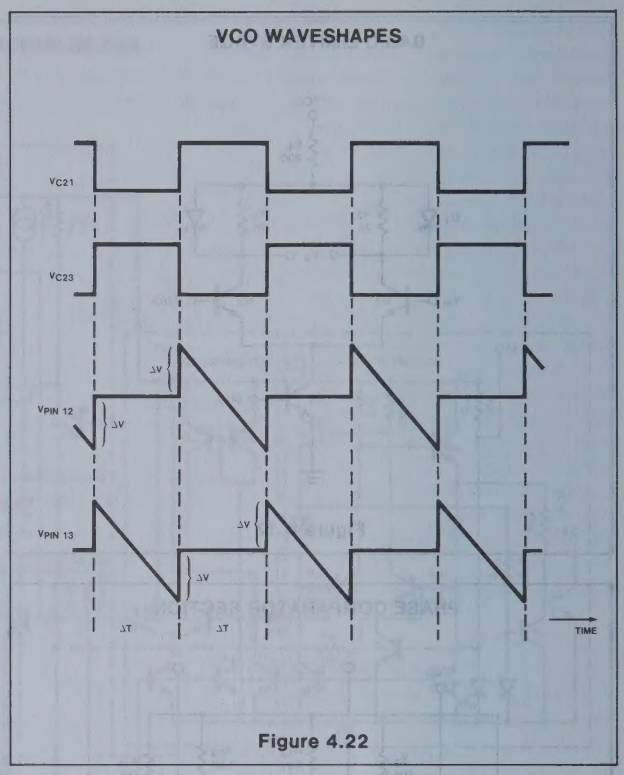


Figure 4.22

Q17 - Q18 and R_{15} - R_{16}, the VCO control voltage is applied differentially to the base of Q27 and to the common bases of Q25 and Q26.

The VCO control voltages from the phase comparator are the pin 4 and pin 5 voltages or

$$V_4 = V_{C9} = V_{B18} = V_{CM} + \frac{1}{2} V_{DM} \quad (4.4)$$

$$V_5 = V_{C12} = V_{B17} = V_{CM} - \frac{1}{2} V_{DM} \quad (4.5)$$

where V_{CM} and V_{DM} are the respective common-mode and the difference-mode voltages.

Emitter followers Q17 and Q18 convert these control voltages into control currents through D_6 and D_7 of the form

$$I_6 = \frac{1}{R_{15}}\left[V_{CM} - \frac{1}{2} V_{DM} - 3 V_{BE}\right] \quad (4.6)$$

$$I_7 = \frac{1}{R_{16}}\left[V_{CM} + \frac{1}{2} V_{DM} - 3 V_{BE}\right] \quad (4.7)$$

These individual currents are summed in D_8 and become with $R_{15} = R_{16} = R$.

$$I_8 = I = I_6 + I_7 = \frac{2}{R}(V_{CM} - 3 V_{BE}) \quad (4.8)$$

Writing I_6 and I_7 as functions of the total I current gives

$$I_6 = \frac{I}{2}\left(1 - \frac{V_{DM}}{RI}\right) \quad (4.9)$$

$$I_7 = \frac{I}{2}\left(1 + \frac{V_{DM}}{RI}\right) \quad (4.10)$$

Now consider variations in I_6 and I_7 while I remains constant.

Let x indicate the current imbalance such that

$$I_6 = (1 - x) I = \frac{I}{2}\left(1 - \frac{V_{DM}}{RI}\right) \quad (4.11)$$

$$I_7 = xI = \frac{I}{2}\left(1 + \frac{V_{DM}}{RI}\right) \quad (4.12)$$

where $0 \leq x \leq 1$. Thus x is defined to be

$$x = \frac{1}{2}\left(1 + \frac{V_{DM}}{RI}\right) \quad (4.13)$$

Currents I_6 and I_7 establish proportional currents in Q25, Q26, and Q27 in a manner similar to the analysis above since the current in Q28 is a constant, or

$$I_o = I_{C28} = I_{E25} + I_{E26} + I_{E27A} + I_{E27B}$$

Gilbert(10) has shown that the D_7 - D_8 diode pair will cause identical differential currents to be reflected in both the Q25 - Q26 and the Q27A - Q27B differential amplifier pairs. Consequently the constant current of I_o jointly shared by the differential amplifier pairs will divide in each pair with the same x factor imbalance as in Equation 4.13.

$$I_{E25} + I_{E26} = xI_o \quad (4.14)$$

$$I_{E25} = I_{E26} = \frac{x}{2} I_o \quad (4.15)$$

$$I_{E27A} + I_{E27B} = (1 - x) I_o \quad (4.16)$$

$$I_{E27A} = I_{E27B} = \left(\frac{1 - x}{2}\right) I_o \quad (4.17)$$

Now consider placing a capacitor between the collectors of Q25 and Q26 (pins 12 and 13). Oscillation will occur with the capacitor alternately being charged by Q21 and Q23 and constantly discharged by Q25 and Q26. When the Q21 and Q22 pair conducts, Q23 and Q24 will be off causing a negative ramp voltage to appear at pin 13 and a constant voltage at pin 12 as shown in Figure 4.22. During the next half-cycle, the transistor roles and voltages are reversed. Capacitor discharge is via Q25 and Q26 which act as constant-current sinks with current amplitudes as in Equation 4.15.

During each half-cycle, the capacitor voltage changes linearily by $2\Delta V$ volts in ΔT seconds where

$$\Delta V = 2R_{20} I_o \left(\frac{x}{2} + \frac{1 - x}{2}\right) = R_{20} I_o \quad (4.18)$$

and

$$\Delta T = \frac{C 2\Delta V}{I_{E25}}. \quad (4.19)$$

Combining these two equations with Equation 4.15 gives a half period of

$$\Delta T = \frac{4C R_{20}}{x} \quad (4.20)$$

Utilizing Equation 4.13 with the ΔT expression gives the desired VCO frequency expression of

$$f_o = f_o'\left(1 + \frac{V_{DM}}{RI}\right) = f_o'\left[\frac{V_{DM}}{2(V_{CM} - 3 V_{BE})}\right] \quad (4.21)$$

where f_o' is the VCOs free-running frequency given by

$$f_o' = \frac{1}{16\ R_{20}\ C} \quad (4.22)$$

Equation 4.21 shows that the oscillator frequency is a linear function of the differential voltage from the phase comparator. Resistors R_{35} and R_{36} function to insure that an initial current imbalance exists between the Q25 - Q26 transistor pair and the dummy Q27. This imbalance insures that the oscillator is self-starting when power is first applied to the circuit.

The VCO conversion gain is determined as

$$K_o = \frac{\partial f_o}{\partial V_{DM}} = \frac{f_o'}{RI} \text{ Hz/volt} \quad (4.23)$$

which is valid as long as the transistors V_{BE} changes are small with respect to the common-mode voltage. Both f_o and K_o are inversely proportional to R which has a strong positive temperature coefficient. An internal current I_R having an equal and opposite negative temperature coefficient is inserted into the VCO as shown in Figure 4.21.

Experimental determination of K_o can be found from the data of Figure 4.23 where K_o is the slope of either line. Numerically these results are for $I_{BIAS} = 0$,

$$K_o = 0.95 \frac{MHz}{volt} = 5.9 \times 10^6 \frac{rad}{volt\text{-}sec} \quad (4.24)$$

and for $I_{BIAS} = 800\mu A$

$$K_o = 1.7 \frac{MHz}{volt} = 10.45 \times 10^6 \frac{rad}{volt\text{-}sec} \quad (4.25)$$

It must be noted that the specific values obtained for K_o in the manner above are valid only for the 1.0MHz free-running frequency where the data was taken. However, good estimates for K_o at other free-running frequencies can be obtained by linearly scaling K_o to the desired f_o'. Thus it is sometimes convenient to define a normalized K_o as

$$K_{o(norm)} = \frac{K_o}{f_o'} = 5.9 \frac{rad}{volt} (I_{BIAS} = 0)$$

$$= 10.45 \frac{rad}{volt} (I_{BIAS} = 800\mu A) \quad (4.26)$$

The K_o estimate for any bias then can be obtained by multiplying the normalized conversion gain by the desired free-running frequency, or

$$K_o \text{ (any } f_o') = K_{o(norm)}\ f_o'. \quad (4.27)$$

The additional VCO circuitry of Q29 through Q36 (Figure 4.16) functions to produce the TTL and ECL compatible outputs at pins 9 and 11.

Amplifier

The difference-mode voltage from the phase comparator is extracted and amplified by the amplifier in Figure 4.16. The single-ended output from this amplifier serves as input signals for both the Schmitt Trigger and a second differential amplifier. Low-pass filtering with a large capacitance at pin 14 produces a stable dc reference level as the second input to the Schmitt Trigger. When the PLL is locked, the voltage at pin 14 is directly proportional to the difference between the input frequency and f_o'. Thus pin 14 provides the demodulated output for a FM input signal.

Schmitt Trigger

In FSK applications the pin 14 voltage will assume two different voltage levels corresponding to the mark and space input frequencies. A voltage comparator could be used to sense and convert these two voltage levels to logic compatible levels. However at high data rates, V_{DM} will contain a considerable amount of carrier signal which can be removed by extensive filtering. Normally this complex filtering requires quite a few components, most all of which are external to the monolithic PLL. Also since the control voltage for the comparator depends upon K_o and the deviations of the mark and space frequencies from f_o', the filtering has to be optimized for each different system utilized. However the necessary dc reference level for the comparator is present in the PLL but buried in carrier frequency feedthrough which appears as noise in the system. A Schmitt trigger with variable hysterisis can be used successfully to decode the FSK data without the need for extensive filtering.

Consider the system shown in Figure 4.24 where the input signal is the single-ended output derived from the amplifier section of the 564. The dc retriever functions to establish a dc reference voltage for the Schmitt trigger. The upper and lower trigger points are adjustable externally around the reference voltage giving the variable hysteresis. For very low data rates, carrier feedthrough will be negligible and the ideal situation depicted in Figure 4.25 results. Increased data rate produces the carrier feedthrough shown in the (b) figure where false FSK outputs result because the feedthrough amplitude exceeds the hysteresis voltage. Having the capability to increase the hysteresis as in (c) produces the desired FSK output in the presence of carrier feedthrough.

Another important factor to be considered is the temperature drift of the f_o' in the VCO. Small changes in f_o' will change the dc level of the input voltage to the Schmitt trigger. This dc voltage shift would produce errors in the FSK output in narrow-band systems where the mark and space deviations in f_{in}

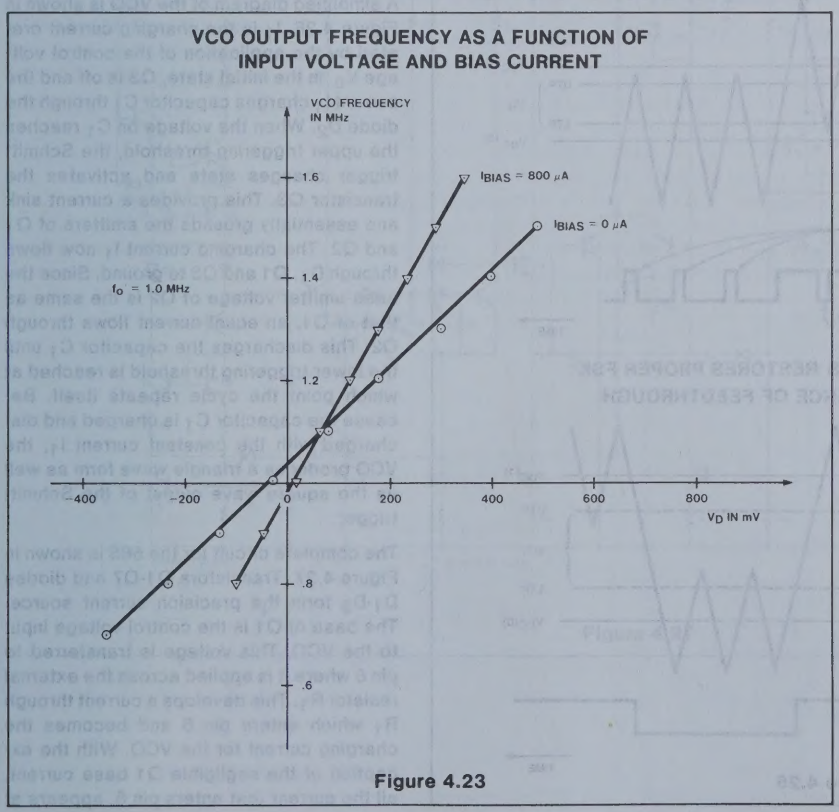


Figure 4.23

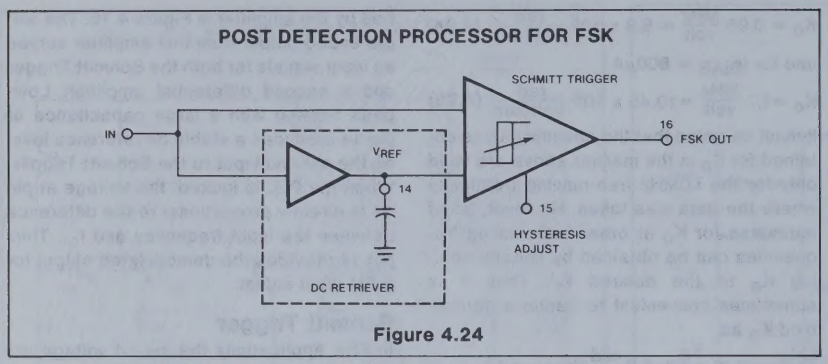


Figure 4.24

WAVESHAPES FOR FSK DECODING IN THE POST DETECTION PROCESSOR

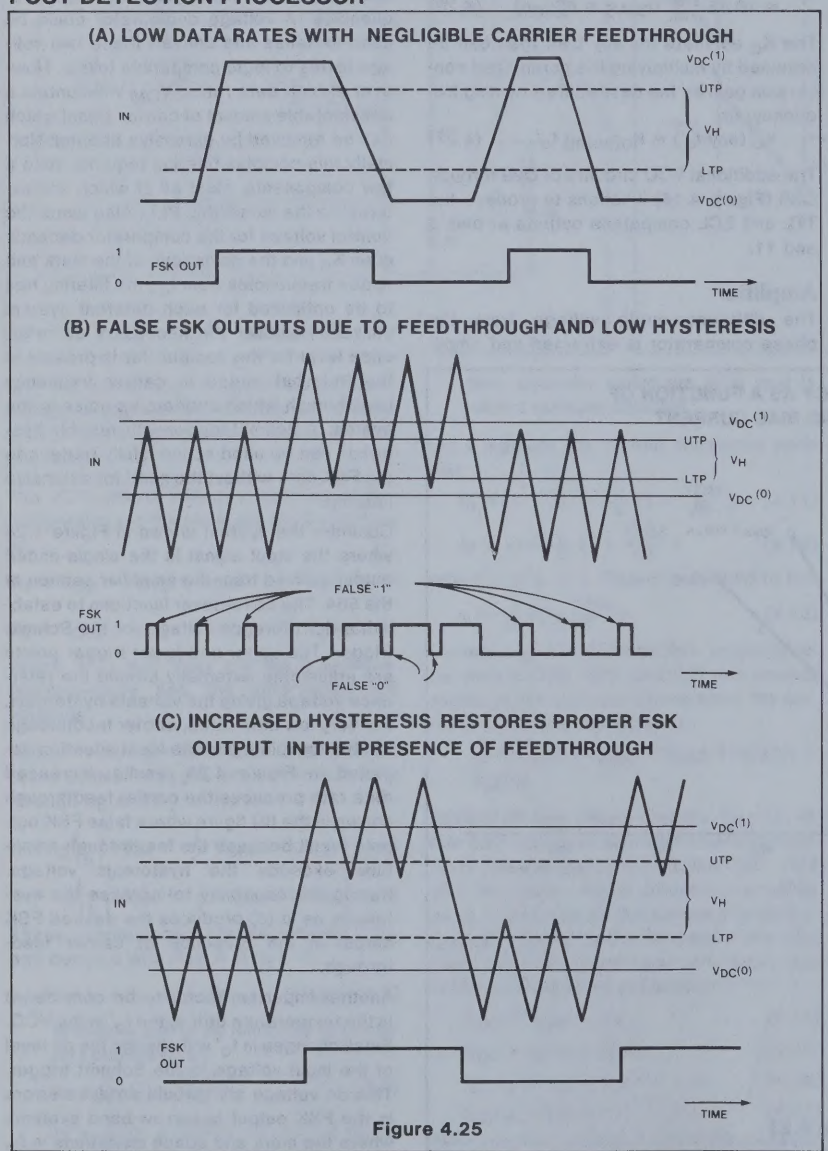


Figure 4.25

are less than the f_o' change with temperature. However this effect can be eliminated if the dc or average value of the amplifier signal is retrieved and used as the reference voltage for the Schmitt trigger. In this manner, variations in the f_o' with temperature do not affect the FSK output.

CIRCUIT DESCRIPTION OF THE 565 PLL

The 565 is a general purpose PLL designed to operate at frequencies below 1MHz. Functionally, the circuit is similar to the 562 in that the loop is broken between the VCO and phase comparator to allow the insertion of a counter for frequency multiplication applications. With the 565, it is also possible to break the loop between the output of the phase comparator and the control terminal of the VCO to allow additional stages of gain or filtering. This is described later in this section.

The VCO is made up of a precision current source and a non-saturating Schmitt trigger. In operation, the current source alternately charges and discharges an external timing capacitor between two switching levels of the Schmitt trigger, which in turn controls the direction of current generated by the current source.

A simplified diagram of the VCO is shown in Figure 4.26. I_1 is the charging current created by the application of the control voltage V_C. In the initial state, Q3 is off and the current I_1 charges capacitor C_1 through the diode D_2. When the voltage on C_1 reaches the upper triggering threshold, the Schmitt trigger changes state and activates the transistor Q3. This provides a current sink and essentially grounds the emitters of Q1 and Q2. The charging current I_1 now flows through D_1, Q1 and Q3 to ground. Since the base-emitter voltage of Q2 is the same as that of Q1, an equal current flows through Q2. This discharges the capacitor C_1 until the lower triggering threshold is reached at which point the cycle repeats itself. Because the capacitor C_1 is charged and discharged with the constant current I_1, the VCO produces a triangle wave form as well as the square wave output of the Schmitt trigger.

The complete circuit for the 565 is shown in Figure 4.27. Transistors Q1-Q7 and diodes D_1-D_3 form the precision current source. The base of Q1 is the control voltage input to the VCO. This voltage is transferred to pin 8 where it is applied across the external resistor R_1. This develops a current through R_1 which enters pin 8 and becomes the charging current for the VCO. With the exception of the negligible Q1 base current, all the current that enters pin 8, appears at

SIMPLIFIED DIAGRAM OF 565 VCO

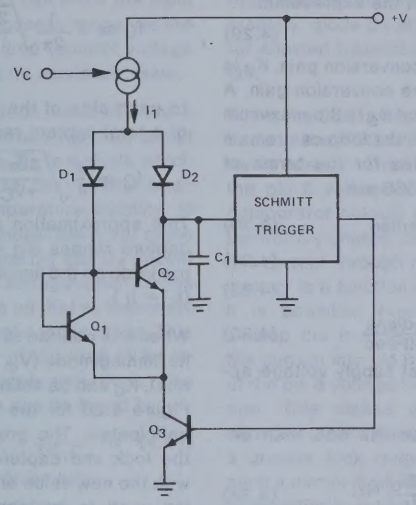


Figure 4.26

the anodes of diodes D_2 and D_3. When Q8 (controlled by the Schmitt trigger) is on, D_3 is reverse biased and all the current flows through D_2 to the duplicating current source Q5-Q7, R_2-R_3 and appears as the capacitor discharge current at the collector of Q5. When Q8 is off, the duplicating current source Q5-Q7, R_2-R_3 floats and the charging current passes through D_3 to charge C_1.

The Schmitt trigger (Q11, Q12) is driven from the capacitor triangle wave form by the emitter follower Q9. Diodes D_6-D_9 prevent saturation of Q11 and Q12, enhancing the switching speed. The Schmitt trigger output is buffered by emitter follower Q13 and is brought out to pin 4, and is also connected back to the current source by the differential amplifier (Q14-Q16).

When operated from dual symmetrical supplies, the square wave on pin 4 will swing between a low level of slightly (0.2V) below ground to a high level of one diode voltage drop (0.7V) below the positive supply. The

CIRCUIT DIAGRAM OF 565

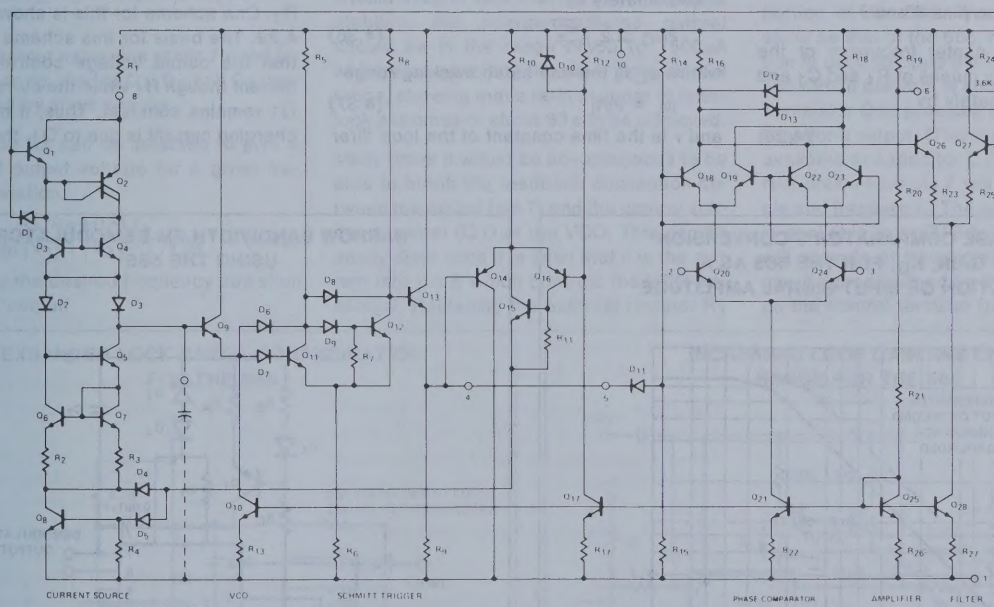


Figure 4.27

triangle wave form on pin 9 is approximately centered between the positive and negative supplies and has an amplitude of 2V with supply voltages of ±5V. The amplitude of the triangle waveform is directly proportional to the supply voltages.

The phase comparator is again of the doubly-balanced modulator type. Transistors Q20 and Q24 form the signal input stage, and must be biased externally. If dual symmetrical supplies are used, it is simplest to bias Q20 and Q24 through external resistors to ground. The switching stage Q18, Q19, Q22 and Q23 is driven from the Schmitt trigger via pin 5 and D_{11}. Diodes D_{12} and D_{13} limit the phase comparator output, and differential amplifier Q26 and Q27 provides increased loop gain.

The loop low pass filter is formed with an external capacitor (connected to pin 7) and the collector resistance R_{24} (typically 3.6KΩ). The voltage on pin 7 becomes the error voltage which is then connected back to the control voltage terminal of the VCO (base of Q1). Pin 6 is connected to a tap on the bias resistor string and provides a reference voltage which is nominally equal to the output voltage on pin 7. This allows differential stages to be both biased and driven by connecting them to pins 6 and 7.

The free-running center frequency of the 565 is adjusted by means of R_1 and C_1 and is given approximately by

$$f_o' \simeq \frac{1.2}{4R_1C_1} \qquad (4.28)$$

When the phase comparator is in the limiting mode ($V_{in} \geq 200mV$ p-p), the lock range can be calculated from the expression:

$$2\omega_L = 2K_oK_dA\Theta_d \qquad (4.29)$$

where K_o is the VCO conversion gain, K_d is the phase comparators conversion gain, A is the amplifier gain, and Θ_d is the maximum phase error over which the loop can remain in lock. Specific values for the terms of Equation 4.29 for the 565 are

$$K_d = \frac{1.4}{\pi} \text{ volts/radian} \qquad (4.30)$$

$$A = 1.4 \qquad (4.31)$$

$$e_d = \frac{\pi}{2} \text{ radians} \qquad (4.32)$$

$$K_o = \frac{50\, f_o'}{V_{CC}} \frac{\text{radians}}{\text{Volt-sec}} \qquad (4.33)$$

where V_{CC} is the total supply voltage applied to the circuit.

The tracking range for the 565 then becomes:

$$f_L \simeq \pm\left|\frac{\omega_L}{2\pi}\right| \simeq \pm \frac{8f_o}{V_{CC}} \text{ Hz.} \qquad (4.34)$$

to each side of the free-running frequency, or a total lock range of:

$$2f_L \simeq \frac{16f_o}{V_{CC}} \text{ Hz} \qquad (4.35)$$

The capture range, over which the loop can acquire lock with the input signal is given approximately by:

$$2\omega_C \simeq 2\sqrt{\frac{\omega_L}{\tau}} \qquad (4.36)$$

where ω_L is the one-sided tracking range

$$\omega_L = 2\pi f_L \qquad (4.37)$$

and τ is the time constant of the loop filter

$$\tau = RC_2 \qquad (4.38)$$

The lock-in range can be written as:

$$f_C \simeq \pm\frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}} = \pm\frac{1}{2\pi}\sqrt{\frac{32\pi f_o'}{V_{CC}}} \qquad (4.39)$$

to each side of the free-running frequency or a total capture range of:

$$f_C \simeq \frac{1}{\pi}\sqrt{\frac{32\pi f_o'}{\tau V_{CC}}} \qquad (4.40)$$

This approximation works well for narrow capture ranges ($f_C = 1/3f_L$ but becomes too large as the limiting case is approached ($f_c = f_L$).

When it is desired to operate the 565 out of its limiting mode ($V_{in} < 200mV$ p-p or 32mV rms), K_d can be estimated from the graph in Figure 4.28 for the specific input voltage anticipated. The previous calculations for the lock and capture ranges remain valid with the new value of K_d from the graph being used to replace the K_dA product in Equation 4.29. In Figure 4.28, the dc amplifier gain A has been included in the K_d value.

For applications where both a narrow lock range and a large output voltage swing are required, it is necessary to inject a constant current into pin 8 and increase the value of R_1. One scheme for this is shown in Figure 4.29. The basis for this scheme is the fact that the output voltage controls only the current though R_1 while the current through Q1 remains constant. Thus, if most of the charging current is due to Q1, the total cur-

PHASE COMPARATOR'S CONVERSION GAIN, K_D, FOR THE 565 AS A FUNCTION OF INPUT SIGNAL AMPLITUDE

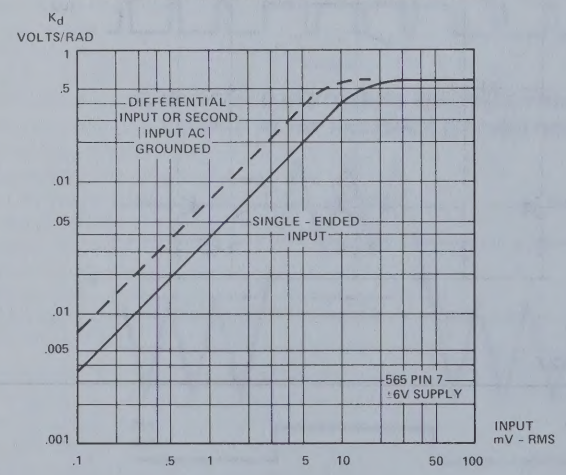


Figure 4.28

NARROW BANDWIDTH FM DEMODULATOR USING THE 565

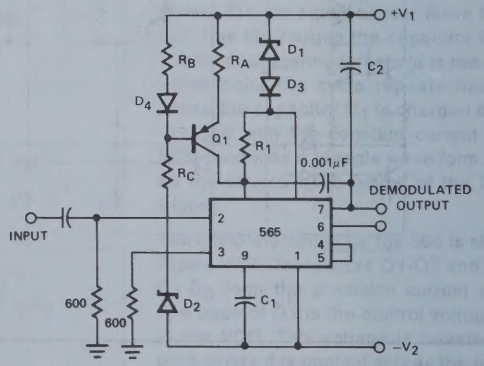


Figure 4.29

rent can be varied only a small amount due to the small change in current through R_1. Consequently, the VCO can track the input signal over a small frequency range yet the output voltage of the loop (control voltage of the VCO) will swing its maximum value.

Diode D_1 is a Zener diode, used to allow a larger voltage drop across R_A than would otherwise be available. D_4 is a diode which should be matched to the emitter-base junction of Q1 for temperature stability. In addition, D_1 and D_2 should have the same breakdown voltages and D_3 and D_4 should be similar so that the voltage seen across R_B and R_C is the same as that seen across pins 10 and 1 of the phase locked loop. This causes the frequency of the loop to be insensitive to power supply variations. The free-running frequency can be found by:

$$f_o' \simeq \frac{2R_B}{(R_B + R_C)\,R_A C_1} + \frac{1}{4R_1 C_1}\ \text{Hz} \quad (4.41)$$

and the total range is given by:

$$2f_L \simeq \frac{22.4V_D(R_B+R_C)R_A f_o'}{(|V_1|+|V_2|-V_z-V_D)\left[8R_BR_1+R_A(R_B+R_C)\right]}\ \text{Hz} \quad (4.42)$$

where V_D is the forward biased diode voltage ($\simeq$0.7V), V_Z is the zener diode breakdown voltage, V_1 is the positive supply voltage, and V_2 is the negative supply voltage.

When the output excursion at pin 7 need be only a volt or so, diodes D_1, D_2 and D_3 may be replaced by short circuits.

The value of R_1 can be selected to give a prescribed output voltage for a given frequency deviation.

$$R_1 = \frac{R_A(R_B+R_C)\,f_o'}{R_B(|V_1|+|V_2|-0.7)\,\Delta f} \quad (4.43)$$

where Δf is the desired frequency deviation per volt of output.

In most instances, R_B and R_A are chosen to be equal so that the voltage drop across them is about 200mV. For best temperature stability, diode D_1 should be a base-collector shorted transistor of the same type as Q1.

When the 565 is connected normally, feedback to the VCO from the phase comparator is internal. That is, an amplifier makes the pin 8 voltage track the pin 7 (phase comparator output) voltage. Since the capacitor C_1 charge current is determined by the current through resistance R_1, the frequency is a function of the voltage at pin 8. It is possible, however, to bypass and swamp the internal loop amplifier so that the current into pin 8 is no longer a function of the pin 8 voltage but only of the pin 7 voltage. This makes a greater charge-discharge current variation possible, allowing a greater lock range. Figure 4.30 shows such a circuit in which the μA741 operational amplifier is set for a differential gain of 5, feeding current to pin 8 through the 33KΩ resistor (simulating a current source). Not only is the tracking range greatly expanded, but the output voltage as a function of frequency is five times greater than normal. In setting up such a circuit, the designer should keep in mind that for best frequency stability, the charge-discharge current should be in the range of 50 to 1500μA which also specifies the pin 8 input current range, showing that a ratio of upper to lower lock extremes of about 30 can be achieved.

Many times it would be advantageous to be able to break the feedback connection between the output (pin 7) and the control voltage terminal (Q1) of the VCO. This can be easily done once it is seen that it is the *current* into pin 8 which controls the VCO frequency. Replacing the external resistor R_1 with a current source, such as in Figure 4.31, effectively breaks the internal voltage feedback connection. The current flowing into pin 8 is now independent of the voltage on pin 8. The output voltage (on pin 7) can now be amplified or filtered and used to drive the current source by a scheme such as that shown in Figure 4.31. This scheme allows the addition of enough gain for the loop to stay in lock over a 100:1 frequency range, or conversely, to stay in lock with a precise phase difference (between input and VCO signals) which is almost independent of frequency variation. Adjustment of the voltage to the non-inverting input of the op amp, together with a large enough loop gain allows the phase difference to be set at a constant value between 0° and 180°. In addition, it is now possible to do special filtering to improve the performance in certain applications. For instance, in frequency multiplication applications it may be desirable to include a notch filter tuned to the sum frequency component to minimize incidental FM without excessive reduction of capture range.

CIRCUIT DESCRIPTION OF THE 566 PLL

The 566 is the voltage controlled oscillator portion of the 565. The basic die is the same as that of the 565; modified metalization is used to bring out only the VCO. The 566 circuit diagram is shown in Figure 4.32. Transistor Q18 provides a buffered triangle waveform output. (The triangle waveform is available at capacitor C_1 also, but any current drawn from pin 7 will alter the duty cycle and frequency.) The square wave output is available from Q19 by pin 4. The circuit will operate at freqencies up to 1MHz and may be programmed by the voltage applied on the control terminal (pin 5), by injecting

EXPANDED LOCK RANGE CONFIGURATION FOR THE 565

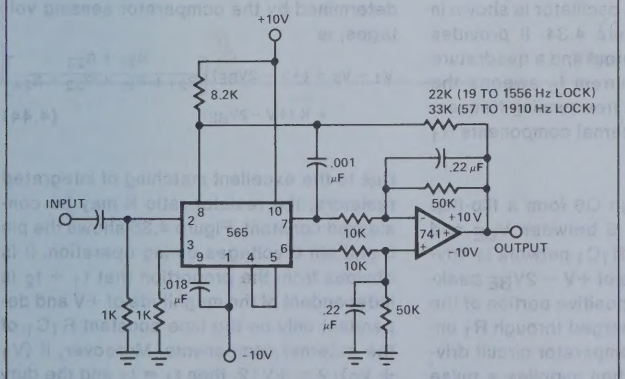


Figure 4.30

INCREASED LOOP GAIN AND LOCK RANGE FOR THE 565

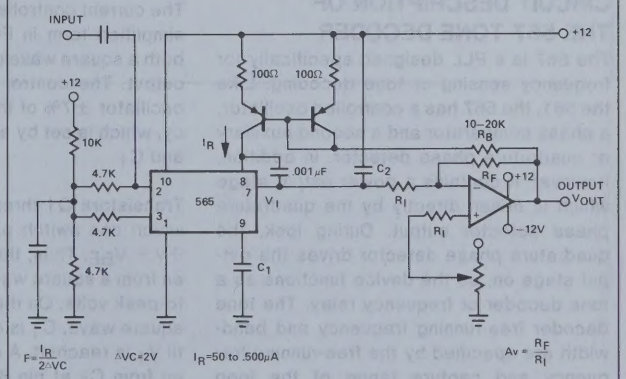


Figure 4.31

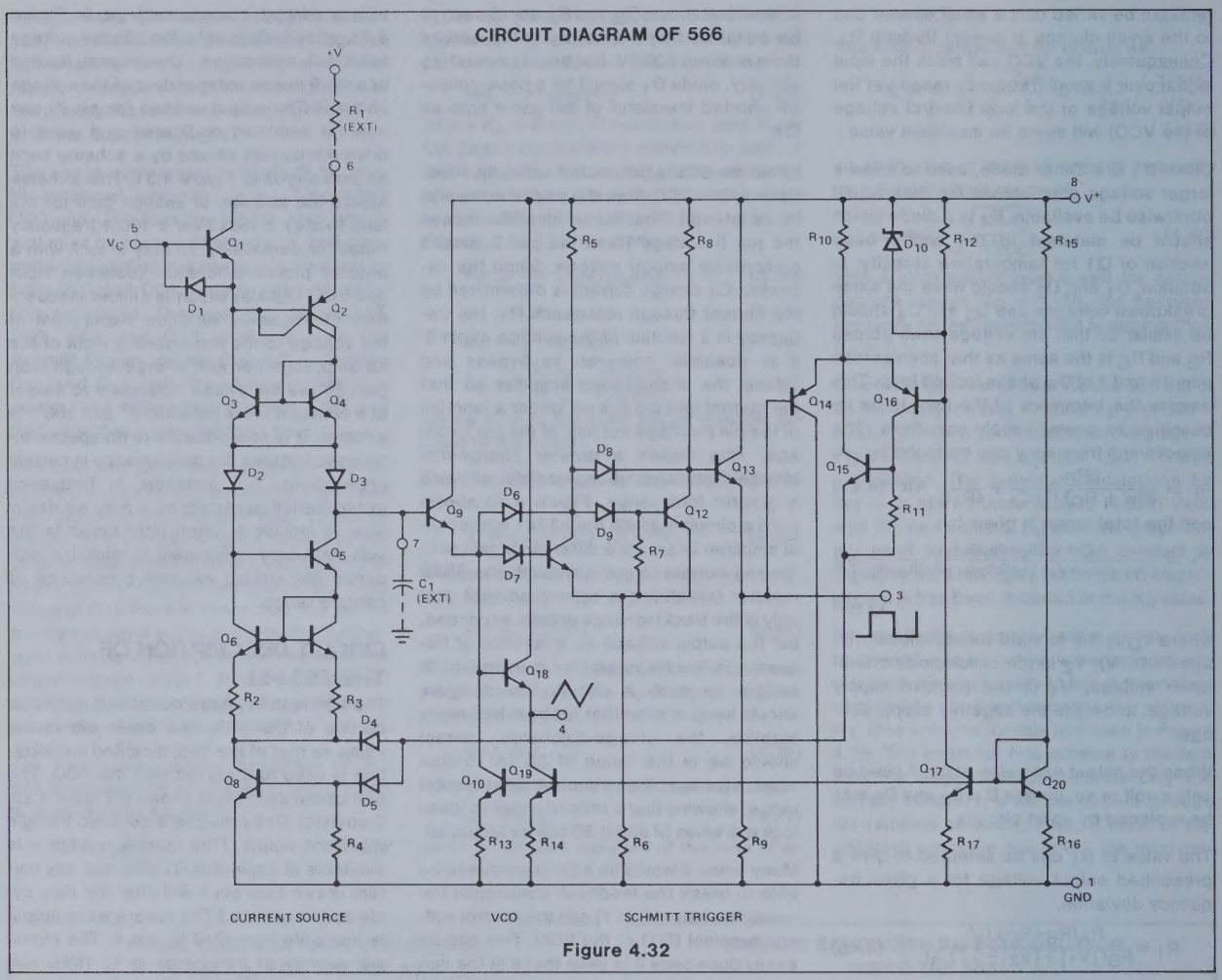


Figure 4.32

current into pin 6, or by changing the value of the external resistor and capacitor (R_1 and C_1).

CIRCUIT DESCRIPTION OF THE 567 TONE DECODER

The 567 is a PLL designed specifically for frequency sensing or tone decoding. Like the 561, the 567 has a controlled oscillator, a phase comparator and a second auxiliary or quadrature phase detector. In addition, however, it contains a power output stage which is driven directly by the quadrature phase detector output. During lock, the quadrature phase detector drives the output stage on, so the device functions as a tone decoder or frequency relay. The tone decoder free-running frequency and bandwidth are specified by the free-running frequency and capture range of the loop portion. Since a tone decoder, by definition, responds to a stable frequency, the lock or tracking range is relatively unimportant except as it limits the maximum attainable capture range. The complete circuit diagram of the 567 is shown in Figure 4.33.

The current controlled oscillator is shown in simplified form in Figure 4.34. It provides both a square wave output and a quadrature output. The control current I_c sweeps the oscillator $\pm 7\%$ of the free-running frequency, which is set by external components R_1 and C_1.

Transistors Q1 through Q6 form a flip-flop which can switch pin 5 between V_{BE} and $+V - V_{BE}$. Thus, the R_1C_1 network is driven from a square wave of $+V - 2V_{BE}$ peak-to-peak volts. On the positive portion of the square wave, C_1 is charged through R_1 until V_1 is reached. A comparator circuit driven from C_1 at pin 6 then supplies a pulse which resets the flip-flop so that pin 5 switches to V_{BE} and C_1 is discharged until V_2 is reached. A second comparator then supplies a pulse which sets the flip-flop and C_1 resumes charging.

The total swing of the capacitor voltage, as determined by the comparator sensing voltages, is

$$V_1 - V_2 = (+V - 2V_{BE})\left[\frac{R_{22} + R_{23}}{R_{21} + R_{22} + R_{23} + R_{24}}\right]$$
$$= K\,(+V - 2V_{BE}) \qquad (4.44)$$

Due to the excellent matching of integrated resistors, the resistor ratio K may be considered constant. Figure 4.35 shows the pin 5 and pin 6 voltages during operation. It is obvious from the proportion that $t_1 + t_2$ is independent of the magnitude of +V and dependent only on the time constant R_1C_1 of the external components. Moreover, if $(V_1 + V_2)/2 = +V/2$, then $t_1 = t_2$ and the duty cycle is 50%. Note that the triangular waveform is phase shifted from the square wave.

CIRCUIT DIAGRAM OF 567

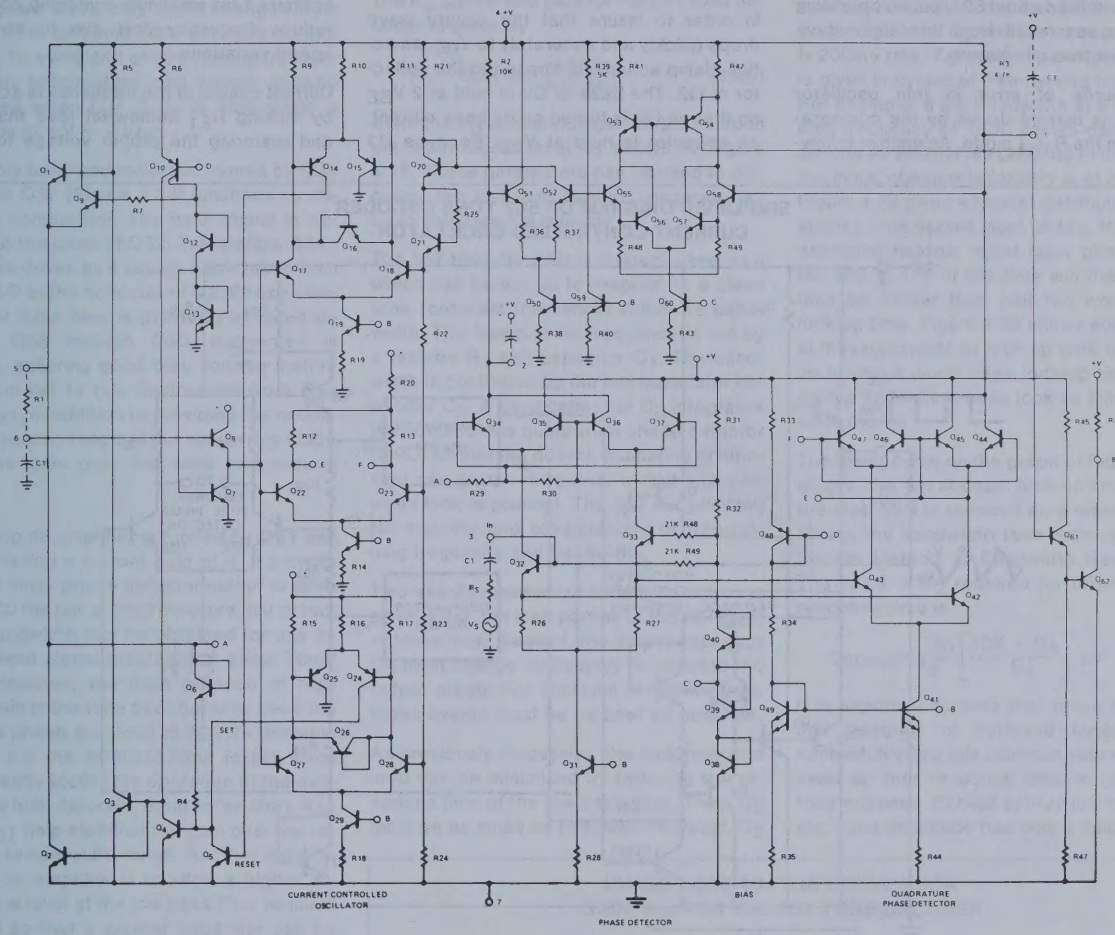


Figure 4.33

A differential stage (Q22 and Q23) amplifies the triangular wave with respect to $(V_1 + V_2)/2$ to provide the quadrature output. (Due to the exponential distortion of the triangle wave, the quadrature output is actually phase shifted about 80°, but no operating compromises result from this slight deviation from true quadrature.)

One source of error in this oscillator scheme is current drawn by the comparators from the R_1C_1 mode. An emitter follower, therefore, is inserted at X to minimize this drain and Q21 placed in series with Q20 to drop the comparator sensing voltage one V_{BE} to compensate for the V_{BE} drop in the emitter follower.

In order to insure that the square wave drops quickly and accurately to V_{BE}, an active clamp scheme is applied to the collector of Q2. The base of Q9 is held at 2 V_{BE} so that as Q2 is turned on its base current, its collector is held at V_{BE}. Because Q2 and Q3 have the same geometry and their base-emitter voltages are the same, the maximum Q2 current when clamped is essentially the same as the collector current of Q3 (as limited by R_5). The flip-flop was optimized for maximum switching speed to reduce frequency drift due to switching speed variations.

Current control of the frequency is achieved by making R_{21} somewhat less than R_{24} and restoring the proper voltage for 50%

SIMPLIFIED DIAGRAM OF 567 TONE DECODER CURRENT-CONTROLLED OSCILLATOR

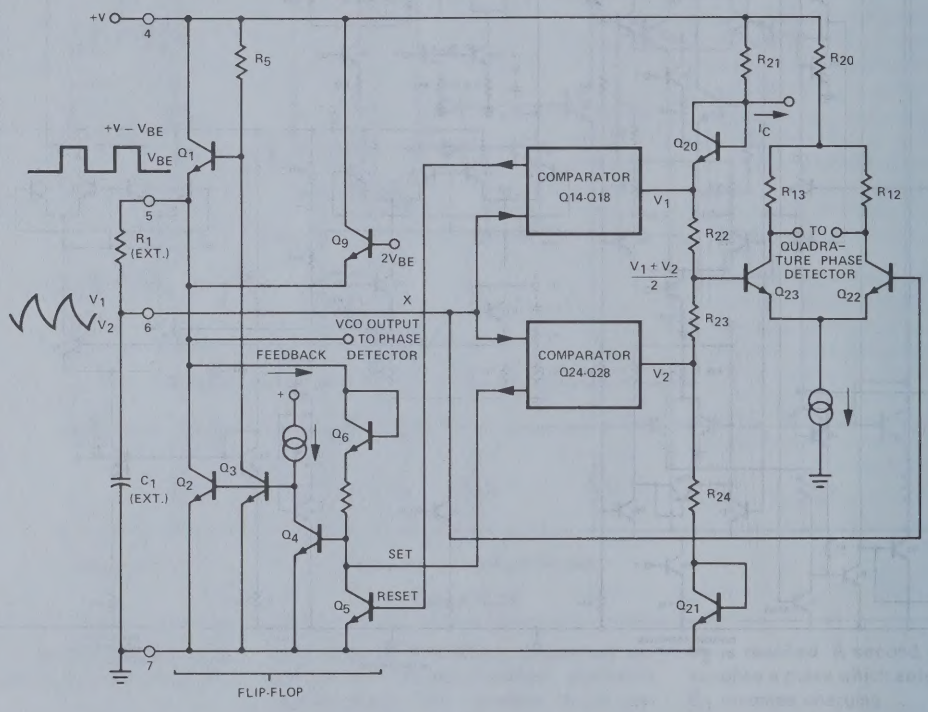


Figure 4.34

CURRENT-CONTROLLED OSCILLATOR WAVESHAPES IN THE 567

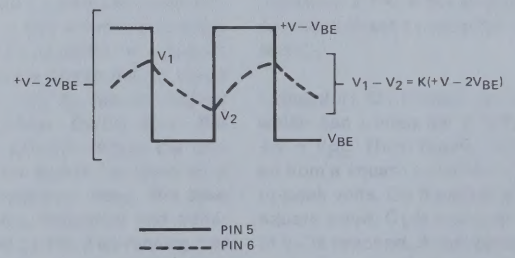


Figure 4.35

duty cycle by drawing I_C of 100μA for the R_{21}, Q20 junction. When I_C is then varied between 0 and 200μA, the frequency changes by $\pm$7%. Because of the slight shift in the voltage levels V_1 and V_2 with I_C, the square wave duty cycle changes from about 47% to about 53% over the control range. To avoid drift of free-running frequency with temperature and supply voltage changes when $I_C \neq 0$, I_C is also made a function of $+V - 2\,V_{BE}$.

A doubly balanced multiplier formed by Q32 through Q37 (Figure 4.33) functions as the phase comparator. The input signal is applied to the base of Q32. Transistors Q34 - Q37 are driven by a square wave taken from the CCO at the collector of Q2. Phase comparator input bias is provided by three diodes, Q38 through Q40, connected in series, assuring good bias voltage matching from run to run. Emitter resistors R_{26} and R_{27}, in addition to providing the necessary dynamic range at the input, help stabilize the gain over the wide temperature range.

The loop dc amplifier is formed by Q51 and Q52. Having a current gain of 8, it permits even a small phase detector output to drive the CCO the full $\pm$7%. Therefore, full detection bandwidth can be obtained for any in-band input signal greater than about 70mV rms. However, the main purpose of high loop gain in the tone decoder is to keep the locked phase as close to $\pi/2$ as possible for all but the smallest input levels since this greatly facilitates operation of the quadrature lock detector. Emitter resistors R_{36} and R_{37} help stabilize the gain over the required temperature range. Another function of the dc amplifier is to allow a higher impedance level at the low pass filter terminal (pin 2) so that a smaller capacitor can be used for a given loop cutoff frequency. Once again, emitter resistors help stabilize the loop gain over the temperature range.

The quadrature phase detector (QPD), formed by a second doubly-balanced multiplier Q42 – Q47, is driven from the quadrature output (E, F, in Figure 4.33) of the CCO. The signal input comes from the emitters of the input transistors Q32 and Q33.

The output stage, Q53 through Q62, compares the average QPD current in the low pass output filter R_3C_3 with a temperature compensated current in R_{39} (forming the threshold voltage V_t).

Since R_3 is slightly lower in value than R_{39}, the output stage is normally off. When the lock and the QPD current I_q occurs, pin 1 voltage drops below the threshold voltage V_t and the output stage is energized.

The uncommitted collector (pin 8) of the power npn output transistor can drive both 100 - 200mA loads and logic elements, including TTL.

The K_O conversion gain for the 567 tone decoder is given by

$$K_O = 0.44\,\omega_o' \frac{\text{radians}}{\text{volt-sec}} \qquad (4.45)$$

while the K_d conversion gain depends upon the input signal level as shown in Figure 4.36. These parameters can be used to calculate the lock and capture range as has been illustrated previously.

The 567 tone decoder is a specialized loop which can be set up to respond to a given tone (constant frequency) within its bandwidth. The free-running frequency is set by a resistor R_1 and capacitor C_1. The bandwidth is controlled by the low pass filter capacitor C_2. A third capacitor C_3 integrates the output of the quadrature phase detector (QPD) so that the dc lock-indicating component can switch the power output stage on when lock is present. The 567 is optimized for stability and predictability of free-running frequency and bandwidth.

Two events must occur before an output is given. First, the loop portion of the 567 must achieve lock. Second, the output capacitor C_3 must charge sufficiently to activate the output stage. For minimum response time, these events must be as brief as possible.

As previously discussed, the lock time of a loop can be minimized by reducing the response time of the low pass filter. Thus, C_2 must be as small as possible. However, C_2 also controls the bandwidth. Therefore, the response time is an inverse function of bandwidth as shown by Figure 4.37, reprinted from the 567 data sheet. The upper curve denotes the expected worst-case response time when the bandwidth is controlled solely by C_2 and the input amplitude is 200mV rms or greater. The response time is given in cycles of free-running frequency. For example, a 2% bandwidth at a free-running frequency of 1000 cycles can require as long as 280 cycles (280ms) to lock when the initial phase relationship is at its worst. Figure 4.38 gives a typical distribution of response time versus input phase. Note that, assuming random initial input phase, only 30/180 = 1/6 of the time will the lock-up time be longer than half the worst case lock-up time. Figure 4.39 shows some actual measurements of lock-up time for a set-up having a worst case lock-up time of 27 cycles and a best-case lock-up time of four input cycles.

The lower curve on the graph of Figure 4.37 shows the worst-case lock-up time when the loop gain is reduced as a means of reducing the bandwidth (see data sheet, Alternate Method of Bandwidth Reduction). The value of C_2 required for this minimum response time is

$$C_{2(min)} = \frac{130}{f_o'}\left[\frac{10K + R_A}{R_A}\right]\mu F \qquad (4.46)$$

It is important to note that noise immunity and rejection of out-band tones suffer somewhat when this minimum value of C_2 is used so that response time is gained at their expense. Except at very low input levels, input amplitude has only a minor effect

PHASE COMPARATOR CONVERSION GAIN, K_D, FOR THE 567 TONE DECODER

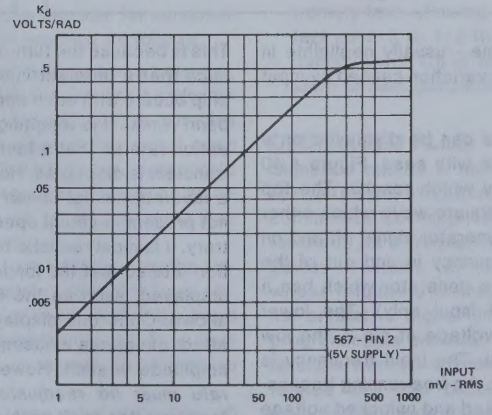


Figure 4.36

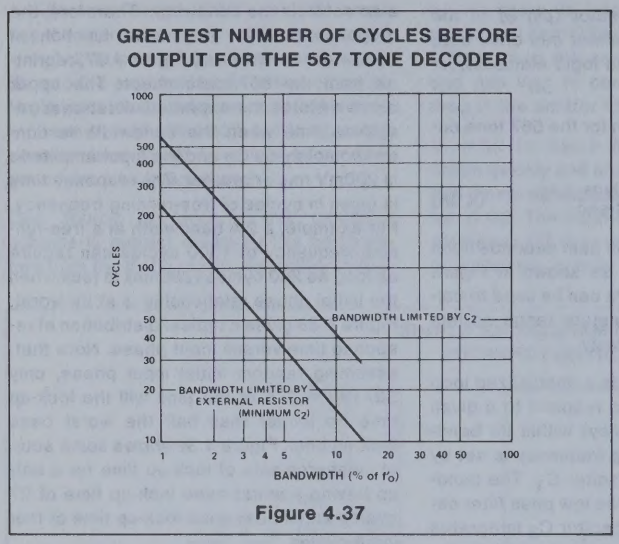


Figure 4.37

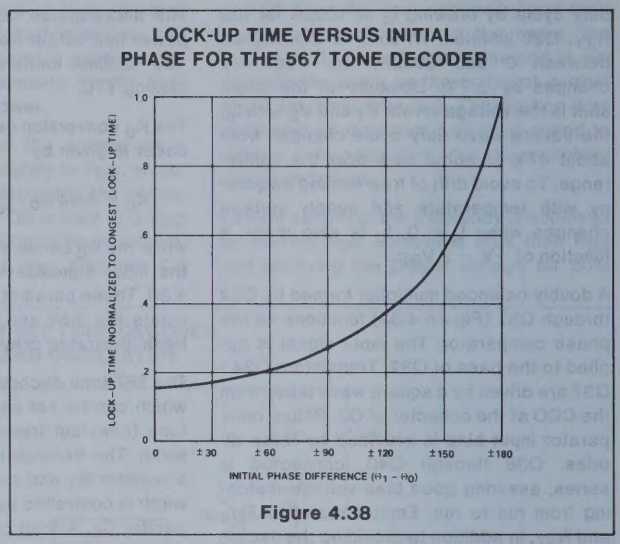


Figure 4.38

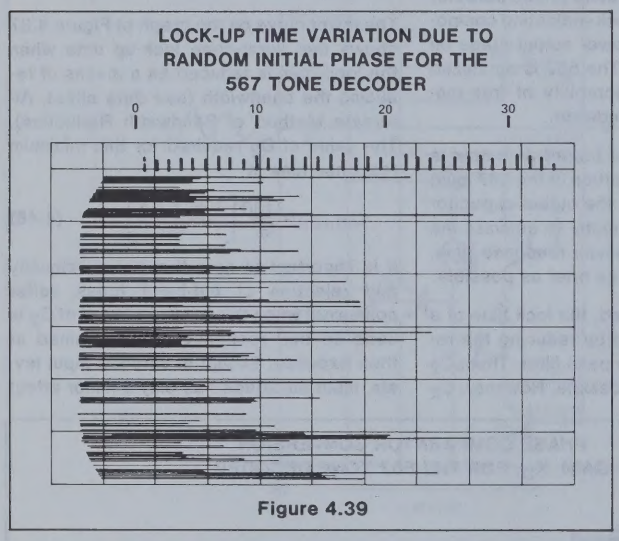


Figure 4.39

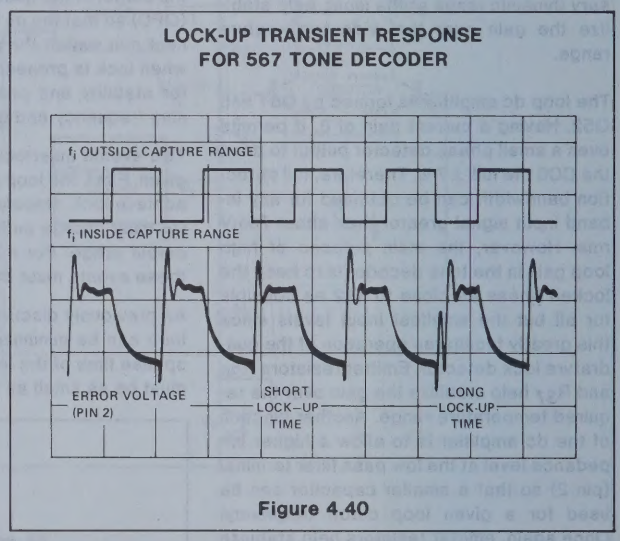

LOCK-UP TRANSIENT RESPONSE FOR 567 TONE DECODER
f_i OUTSIDE CAPTURE RANGE
f_i INSIDE CAPTURE RANGE
ERROR VOLTAGE (PIN 2)
SHORT LOCK-UP TIME
LONG LOCK-UP TIME

Figure 4.40

on the lock-up time - usually negligible in comparison to the variation caused by input phase.

Lock-up transients can be displayed on a two-channel scope with ease. Figure 4.40 shows the display which results. The top trace shows the square wave which either gates the input generator signal off and on (or shifts the frequency in and out of the band if you have a generator which has a frequency control input only). The lower trace shows the voltage at pin 2, the low pass filter voltage. The input frequency is offset slightly from the free-running frequency so that the locked and unlocked voltage are different. It is apparent that, while the C_2 decay during unlock is always the same, the lock transient is different each time. This is because the turn-on repetition rate is such that a different initial phase relationship occurs with each appearance of the in-band signal. It is tempting to adjust the repetition rate so that a fast, constant lock-up transient is displayed. However, in doing so a favorable initial phase is created that is not present in actual operation. On the contrary, it is most realistic to adjust the repetition rate so that the longest lock-up time is displayed, such as the fifth lock transient shows. Once this display is achieved, the effect of various adjustments in C_2 or input amplitude is seen. However, *the repetition rate must be readjusted for worst-case lock-up after each such change.*

Once lock is achieved, the quadrature phase detector output at pin 1 is integrated by C_3 to extract the dc component. As C_3 charges from its quiescent value V_q (see Figure 4.41) to its final value (V_q - ΔV), it passes through the output stage threshold, turning it on. The total voltage change is a function of input amplitude. Since the unadjusted V_q is very close (within 50mV) to V_t, the output stage turns on very soon after lock. Only a small fraction of the output stage time constant ($\tau = 4700C_3$) expires before V_t is crossed so that C_3 does not greatly influence the response time. However, as shown in Figure 4.41(a), the turn-off delay time can be quite long when C_3 is large. Figure 4.41(b) shows how desensitizing the output stage by connecting a high-value resistor between pin 1 and pin 4 (positive supply voltage) can equalize the turn-on and turn-off time. If turn-off delay is im-

EFFECT OF THRESHOLD VOLTAGE ADJUSTMENT ON TONE DECODER TURN-ON AND TURN-OFF DELAY

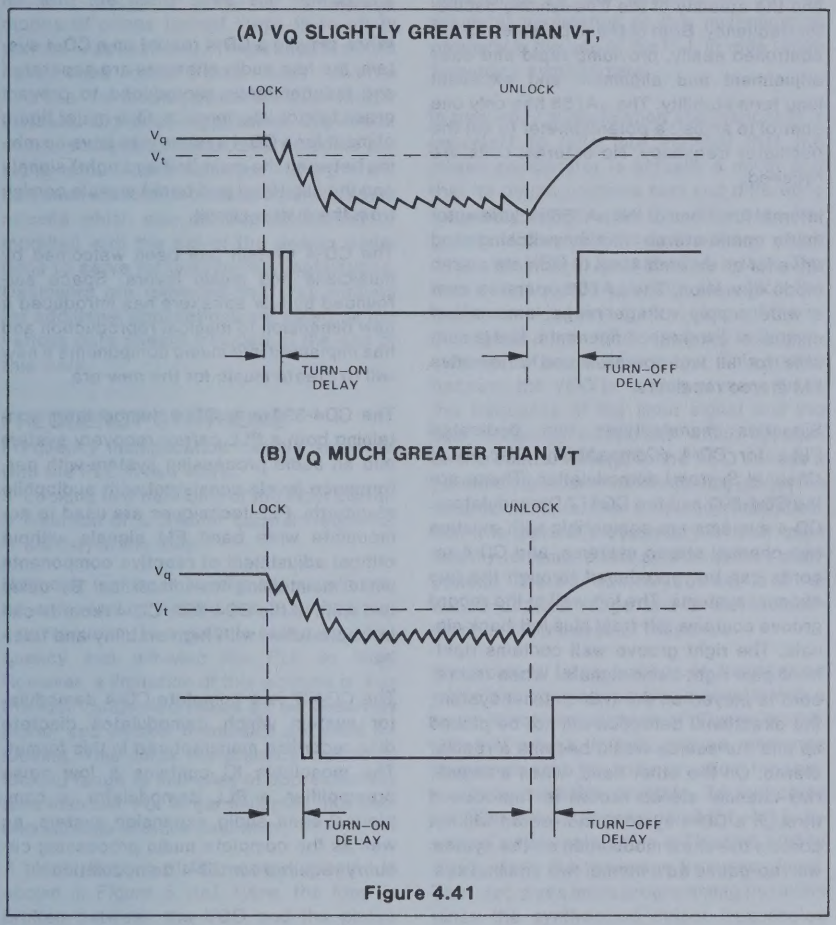


Figure 4.41

portant in the overall response time, then desensitizing can reduce the total delay.

But why not make C_3 very small so that these delays can be totally neglected? The problem here is that the QPD output has a large second harmonic component of the free-running frequency that must be filtered out. Also, noise, outband signals, and difference frequencies formed by close out-band frequencies beating with the VCO frequency appear at the QPD output. All these must be attenuated by C_3 or the output stage will chatter on and off as the threshold is approached. The more noisy the input signal and the larger the near-band signals, the greater C_3 must be to reject them. Thus, there is a complicated relationship between the input spectrum and the size of C_3. What must be done, then, is to make C_3 more than sufficient for proper operation (no false outputs or missed signals) under actual operating conditions and then reduce its value in small steps until either the required response time is obtained or operation becomes unsatisfactory.

In setting up the tone decoder for maximum speed, it is best to proceed as follows:

a After the center frequency has been set, adjust C_2 to give the desired bandwidth or, if the graph of response time in cycles (Figure 4.39) suggests that worst case lock-up time will be too long, incorporate the loop gain reduction scheme as an alternate means of bandwidth reduction. (See data sheet).
b Check lock-up time by observing the waveform at pin 2 while pulsing the input signal on and off (or in and out of the band when a FM generator is used). Adjust repetition rate to reveal worst lock-up time.
c Starting with a large value of C_3 (say 10 C_2), reduce it as much as possible in steps while monitoring the output to be certain that no false outputs or missed signals occur. The full input spectrum should be used for this test. Ignore brief transients or chatter during turn-on and turn-off as they can be eliminated with the chatter prevention feedback technique described in the data sheet.
d Use the desensitizing technique, also described in the data sheet, to balance turn-on and turn-off delay.
e Apply the chatter prevention technique to clean up the output.

If this procedure results in a worst-case response time that is too slow, the following suggestions may be considered:

a Relax the bandwidth requirement.
b Operate the entire system at higher frequency when this option is available.
c Use two tone decoders operating at slightly different frequencies and OR the outputs. This will reduce the statistical occurance of the worst-case lock-up time so that excessive lock-up time occurs. For example, if the lock-up time is marginal 10% of the time with one unit, it will drop to 1% with two units.
d Control the in-band input amplitude to stabilize the bandwidth, set up two tone decoders for maximum bandwidth, and overlap the detection bands to make the desired frequency range equal to the overlap. Since both tone decoders are on only when a tone appears within the overlap range, the outputs can be ANDed to provide the desired selectivity.
e If the system design permits, send the tone to be detected continuously at a low level (say 25mV rms) to keep the loop in lock at all times. The output stage, slightly desensitized, can then be gated on as required by increasing the signal amplitude during the on time. Naturally, the signal phase should be maintained as the amplitude is changed. This scheme is extremely fast, allowing repetition rates as fast as 1/3 to 1/2 the free- running frequency when C_3 is small. This is equivalent to ASK (amplitude shift keying).

DEDICATED PLLS

Signetics makes a number of dedicated, special purpose PLLs for specific audio and communication applications. The 8X08 functions as a frequency synthesizer. This device contains a reference oscillator whose frequency is controlled by an external crystal, a digital phase detector, and programmable dividers. When used in conjunction with an external VCO, a PLL is formed that can produce or synthesize many closely spaced frequencies from the single reference crystal simply by changing the divide-by modulus of the programmable counter. The 8X08 is capable of digitally

programming 200 AM channels with 10kHz spacing and 2000 FM channels with 100kHz spacing from a single 3.6MHz reference crystal. The obvious advantage of using PLL techniques for frequency synthesis is that multiple frequencies can be generated from a single crystal that acts as the reference frequency. All of the synthesized frequencies will have the same temperature stability as that of the single crystal. Thus PLLs alleviate the need for having a separate crystal for each frequency desired, considerably reducing the size and complexity of most communication systems.

The μA758 is a dedicated audio PLL for decoding an FM multiplexed stereo signal into left and right audio channels while suppressing SCA information that may be present in the input signal. The two basic signals that differentiate a stereo multiplexed signal from an FM monaural signal are the 19kHz pilot and the 38kHz subcarrier.

Most non-PLL systems reconstruct the 38kHz subcarrier by using the 19kHz pilot. Such an approach requires frequency multipliers and selective filters in the form of tuning coils. Since maximum channel separation is directly related to proper phasing, alignment procedures were extremely critical and therefore expensive. In addition, long term stability and performance were degraded due to component aging and temperature.

Using the μA758 PLL as a multiplexer decoder eliminates these shortcomings since the phase accuracy of the 38kHz signal is limited only by the loop gain of the system and the stability of the free-running oscillator frequency. Both of these parameters are controlled easily, providing rapid and easy adjustment and alignment and excellent long term stability. The μA758 has only one control to adjust: a potentiometer to set the oscillator frequency. No external coils are required.

Internal functions of the μA758 include automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation. The μA758 operates over a wide supply voltage range, uses a low number of external components, and is suitable for all line-operated and automotive FM stereo receivers.

Signetics manufactures two dedicated PLLs for CD-4 *(Compatibility Discrete 4 Channel System)* demodulation. These are the CD4-392 and the CG477 Demodulators. CD-4 systems are compatible with existing two channel stereo systems, and CD-4 records can be reproduced through the two channel systems. The left wall of the record groove contains left-front plus left-back signals. The right groove wall contains right-front plus right-back signals. When the record is played on the two channel system, the directional detection will not be picked up and the source would become a regular stereo. On the other hand, when a regular two channel stereo record is reproduced through a CD-4 system, the record will not contain the extra modulation so the system will reproduce as a normal two channel system. This interchangeable compatibility feature is the major advantage of the CD-4 system.

When playing a CD-4 record on a CD-4 system, the four audio channels are separated and independently reproduced to prevent cross talk or interference. One major figure of merit for a CD-4 system is to have no mixing between the main (left and right) signals and the sub (front and back) signals coming from the matrix circuit.

The CD-4 system has been welcomed by musicians and music lovers. Space surrounded by four speakers has introduced a new dimension to musical reproduction and has implanted into music components a new will to create music for the new era.

The CD4-392 is a CD-4 demodulator containing both a PLL carrier recovery system and an audio processing system with performance levels consistent with audiophile standards. PLL techniques are used to demodulate wide band FM signals without critical adjustment of reactive components while maintaining low distortion. By using two units of the CD4-392, CD-4 records can be reproduced with high stability and fidelity.

The CG477 is a complete CD-4 demodulator system which demodulates discrete disc recording manufactured in this format. The monolithic IC contains a low noise preamplifier, a PLL demodulator, a complete 2-band audio expansion system, as well as the complete audio processing circuitry required for CD-4 demodulation.

INTRODUCTION

One of the quickest ways to become familiar with the many uses and operational modes of phase locked loops is to study various applications. These applications have been drawn from many diverse sources - textbooks, professional and trade journals, Signetics Application Engineers, users, students projects, and personal designs and experimentations. Every effort has been made to provide usable, workable circuits which may be copied directly or modified with the aid of the design equations to serve for imaginative applications. Designers are reminded that PLL circuits for additional applications are listed on the various data sheets included at the end of this work.

FREQUENCY SYNTHESIS

Frequency multiplication can be achieved with the PLL in two ways:

a Locking to a harmonic of the input signal.
b Insertion of a counter (digital frequency divider) in the loop.

Harmonic locking is simpler and usually can be achieved by setting the VCO free-running frequency to a multiple of the input frequency and allowing the PLL to lock. However, a limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. This limits the practical harmonic locking range to multiples of approximately less than ten. For larger multiples, the second scheme is more desirable.

A block diagram of the second scheme is shown in Figure 5.1(a). Here, the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the divided VCO frequency is locked to the input reference frequency so that the VCO is actually running at a multiple of the reference frequency. The amount of multiplication is determined by the counter. An obvious practical application of this multiplication property is the use of the PLL in wide range frequency synthesizers.

In frequency multiplication applications it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency is dc and is the error voltage which drives the VCO to keep the PLL in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal) if not well filtered, will induce incidental FM on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication it is generally necessary to filter quite heavily to remove this sum frequency component. The tradeoff, of course, is a reduced capture range and a more underdamped loop transient response.

Producing a large number of frequencies with close spacing requires a counter with a large N for the system of Figure 5.1(a). Large N values, in turn, require reference frequencies too low to be practical for commercially available crystals. To overcome this difficulty, a second counter (÷M) is inserted as a prescaler as in Figure 5.1(b) to divide down the reference frequency input. This also gives more programming flexibility since the synthesized output frequencies are functions of both M and N integers, each of which can be changed separately. As an example of fractional frequency synthesis, the two counters can be set to generate an output frequency exactly 16/3 of the input reference frequency. In this case N = 16, M = 3, and the initial f_o' is set to approximately 16/3 times the reference frequency input. The output always will be exactly 16/3 of the input frequency as long as the PLL remains in lock.

PLL frequency synthesizers based upon Figure 5.1(b) find wide applications in many types of communications systems that require precisely spaced channels having narrow bandwidths which are centered around relatively high frequencies. For example, Citizens Band (CB) transceiver applications require forty channels corresponding to forty different reference frequencies, each separated by 10kHz bandwidths and centered in the 26 - 27MHz range. Channel 4 uses 27.005MHz; Channel 5 uses 27.015MHz; Channel 6 uses 27.025MHz; and so on. These frequencies could be produced by using forty different crystals - one for each channel. However, this becomes expensive and adds unnecessary complexity to the system. Frequency mixing techniques have been employed to reduce the number of crystals needed to less than one crystal per channel. For example one common mixer design uses 14 crystals for 23 channels. As a general rule, most practical approaches that use numerous crystals and mixers to produce discrete frequencies require more than one crystal for every two channel frequencies produced. As the number of channels grows large, frequency synthesis using PLLs becomes more attractive, especially since usually only one or two crystals are needed. Frequency stability of all channels will be essentially the same as that of the crystal reference frequency. Reduced system complexity, size, weight, and power consumption are key advantages of PLL synthesizers.

FREQUENCY SYNTHESIS USING PLLs

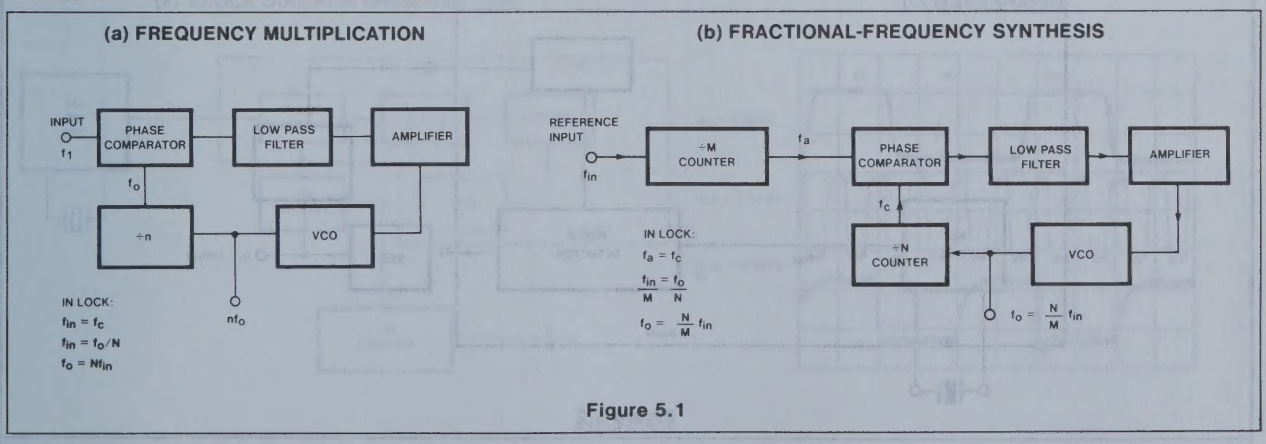


Figure 5.1

Since the function of frequency synthesizers is to generate frequencies and not to linearily decode or demodulate input signals, digital PLLs are more commonly used than analog loops. The Signetics 8X08 and SM5104 are frequency synthesizers designed for programmable digital PLL applications. Block diagrams of these devices are shown in Figure 5.2.

Analog PLLs also can be used for frequency synthesis applications. The 564 is particularly well suited for these applications because the loop is open between the VCO output and the phase comparator input. Also the phase comparator input and VCO output are compatible with TTL counters.

FREQUENCY SYNTHESIS WITH CRYSTAL CONTROL

The system shown in Figure 5.3 has been used to generate frequencies of 5.4MHz and 21.6MHz from a 3.6MHz crystal-controlled source. This reference signal input is produced by using the crystal as the frequency determining element in the VCO of a second PLL. The thermal stability of all three frequencies will be same as the stability afforded by the crystal. It may be necessary to place a small detuning capacitor in parallel with the crystal to precisely tune the PLL to the crystals resonant frequency and to prevent oscillations at harmonics of the resonant frequency. The value of this tuning capacitance must always be kept considerably less than the value required to produce an f_O' without the crystal present. Otherwise the crystal will lose control and the input reference frequency will be set by the capacitor alone.

A recommendation for improved 564 operation is to utilize a divide-by-N counter in the loop which produces "square" waves for the phase comparator that have as close to a 50% duty cycle as possible. Normally counters with even N values produce square wave outputs perfectly compatible for the phase comparator. Counters for odd N values more commonly produce unsymmetrical outputs that can be less desirable inputs to the phase comparator. An easy modification to "square up" odd divide-by-N counter outputs is to insert a single toggling flip-flop stage between the counter output and the phase comparators input. This produces an effective 2N multiplication of the input frequency within the PLL. The extra factor of two is removed by a second toggle flip-flop whose input is the output from the first flip-flop. This is the same system as was previously shown in Figure 5.3(a) where the ÷N counter becomes a ÷2N and M = 2 for the second counter.

DIGITAL PLLS USED FOR FREQUENCY SYNTHESIS

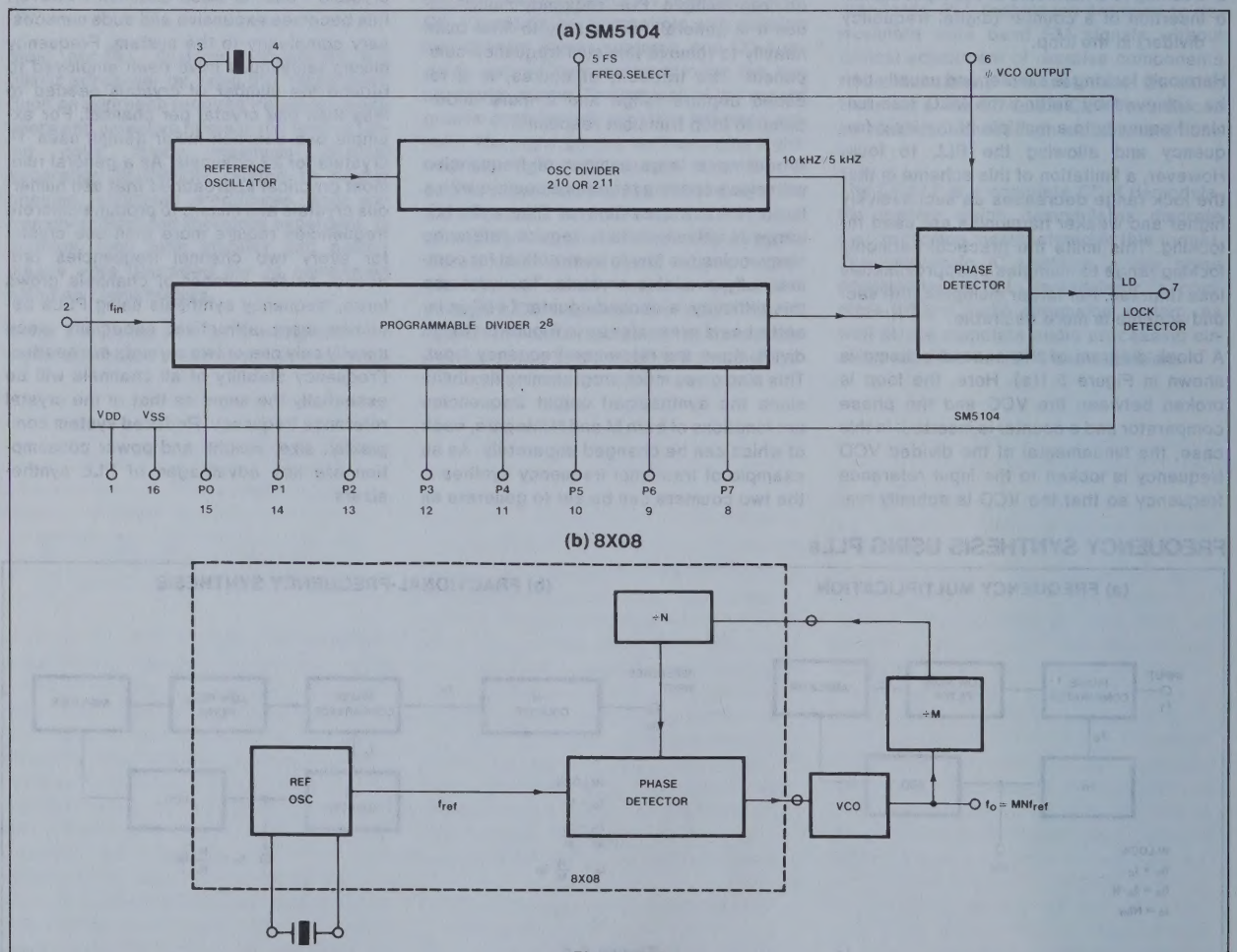


Figure 5.2

The 10kΩ bias potentiometer on the first 564 is used to adjust internal bias currents so that a stable waveshape at the crystal frequency is available as the input for the second PLL. The other 10kΩ potentiometer adjusts the loop gain to insure a large enough capture range for the reference input. Waveshapes for the synthesized frequencies referenced to the 3.6MHz input are shown in Figure 5.3(b).

FSK DEMODULATION

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

FSK Demodulation with the 560B

The 560B phase locked loop can be used as a receiving converter to demodulate FSK audio tones and to provide a shifting dc voltage to initiate mark or space frequencies. The PLL can replace the bulky audio filters and undependable relay circuits previously used for this application. Connection of the 560B PLL as a FSK demodulator is illustrated in Figure 5.4. This specific circuit was designed to match the Bell 103C and 103D Data Phones.

The system functions by locking-on and tracking the output frequency of the receiver. The input frequency shift is translated within the 560B to a dc voltage of about 60mV amplitude which appears at pin 9. This output is amplified, conditioned, and applied to a voltage comparator (μA710) which provides compatible outputs for interfacing with digital logic systems. The voltage at pin 12 should be from 30mV to 2V peak-to-peak, square or sine wave. Pin 10, the de-emphasis terminal, is used for band-shaping. The capacitor connected between this terminal and ground bypasses unwanted high frequency noise to ground.

When modifying this circuit to accommodate other systems, maintain the resistance to ground from pin 9 at approximately 15kΩ. Pins 2 and 3 are the connections for the external capacitor that determines the free-running frequency of the VCO. The 0.33μF value indicated provides a VCO frequency, f_o', of approximately 1060Hz. The value of the timing capacitor can be calculated by

$$C_o = \frac{300}{f_o'} \text{ pF} \qquad (5.1)$$

where f_o' is in MHz.

The comparator has a swing of 2V peak-to-peak, over a 0 to 600 baud input FSK rate, with less than 10% jitter at the comparator output. The circuit is operative over a temperature range of 0° to 70°C with a total drift of approximately 100mV over the temperature range.

FSK Demodulation with the 565

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 5.5. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output (pin 7).

The loop filter capacitor C_2 is chosen to set the proper overshoot on the output and a three-stage RC ladder filter is used to remove the sum frequency components. The band edge of the ladder filter is chosen to be approximately half-way between the maximum keying rate (300 baud or bits per second, or 150Hz). The free-running frequency should be adjusted (with R_1) so that the dc voltage level at the output is the same as that at pin 6 of the loop. The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6.

The input connection is typical for cases where a dc voltage is present at the source and, therefore, a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to achieve a 600Ω input impedance).

A more sophisticated approach primarily useful for narrow frequency deviations is shown in Figure 5.6. Here, a constant current is injected into pin 8 by means of transistor Q1. This has the effect of decreasing the lock range and increasing the output voltage sensitivity to the input frequency shift. The basis for this scheme is the fact that the output voltage (control voltage for the VCO) controls only the current through R_1, while the current through Q1 remains constant. Thus, if most of the capacitor charging current is due to Q1, the current variation due to R_1 will be a small percentage of the total charging current and, consequently, the total frequency deviation of the VCO will be limited to a small percentage of the center frequency. A 0.25μF loop filter capacitor gives approximately 30% overshoot on the output pulse, as seen in the accompanying photographs. Figure 5.7 shows the output of the μA710 comparator and the output of the 565 phase locked loop

FRACTIONAL FREQUENCY SYSTHESIS WITH THE 564

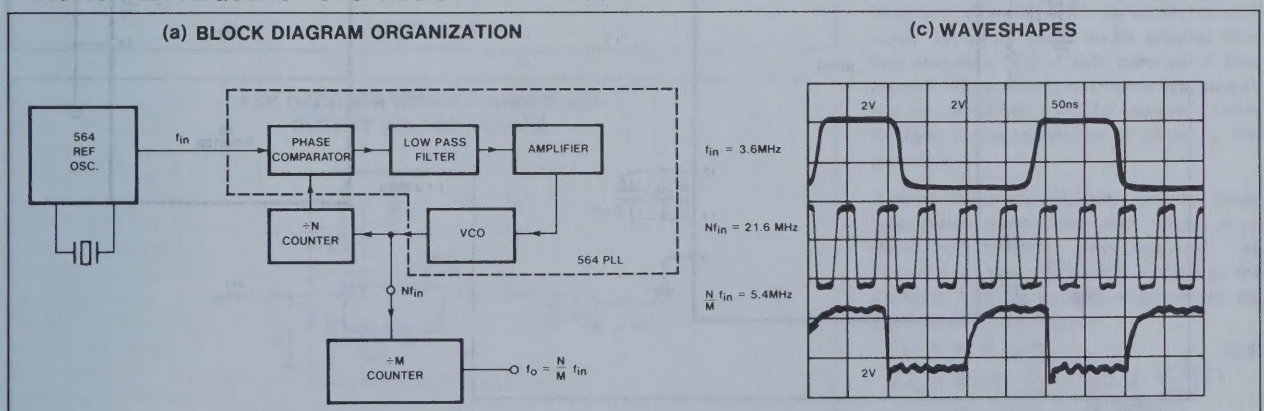


Figure 5.3

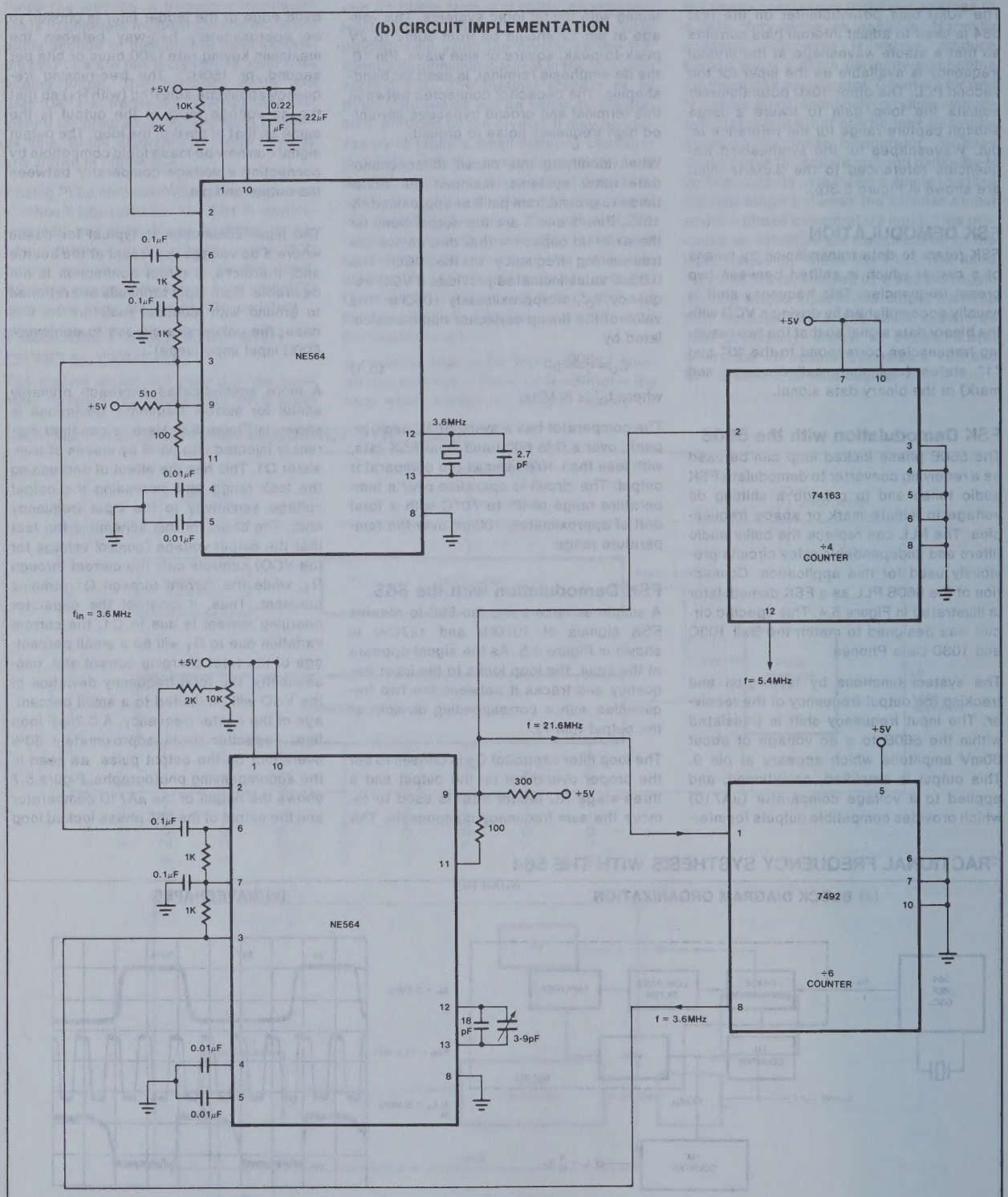


Figure 5.3 (Cont'd)

after the filter at rates of 100, 200 and 300 baud, respectively.

The PLL output is filtered with a two-stage RC ladder filter with a band edge chosen to be approximately 800Hz (approximately half-way between the maximum keying rate of 150Hz and twice the carrier frequency). The number of stages on the filter can be more or less depending on the degree of uncertainty allowable in the comparator output pulse. Two small capacitors (typically 0.001μF) are connected between pins 8 and 7 of the 565 and across the input of the comparator to avoid possible oscillation problems.

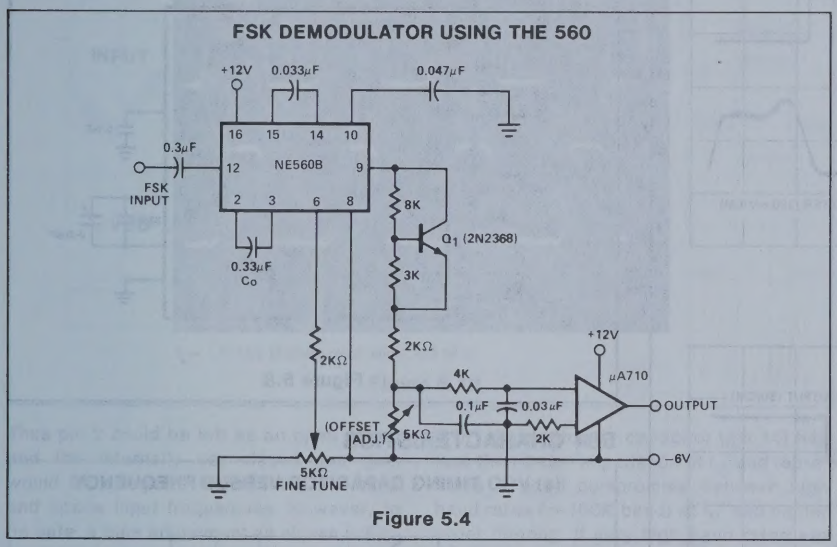


Figure 5.4

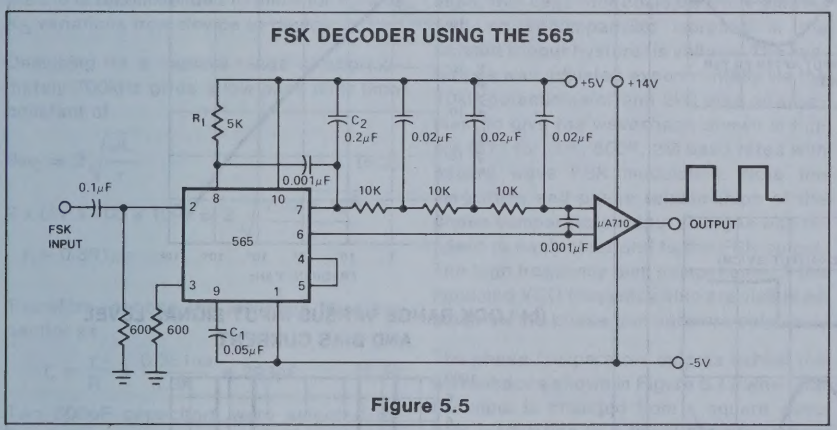


Figure 5.5

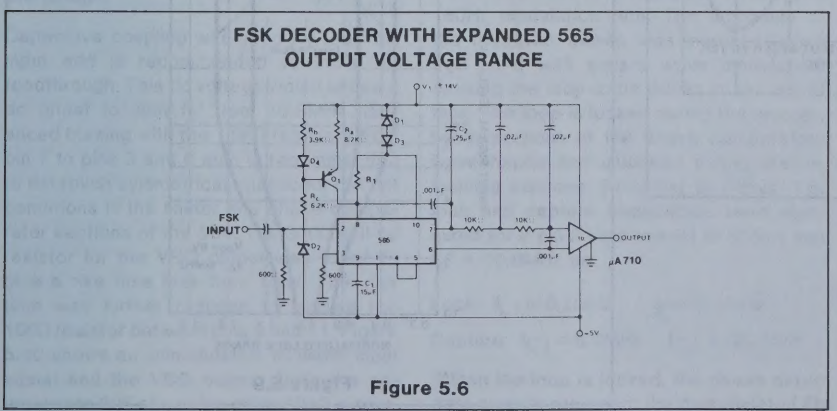


Figure 5.6

For best operation, the free-running VCO frequency should be adjusted so that the output voltage (corresponding to the input frequencies of 1070Hz and 1270Hz) swings equally to both sides of the reference voltage at pin 6. This can be easily done by adjusting the center frequency of the VCO so that the output signal of the μA710 comparator has a 50% duty cycle. It is usually necessary to decouple pin 6 with a large capacitor connected to the positive supply in order to obtain a stable reference voltage for the μA710 comparator.

FSK Demodulation with the 564

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5 volt power supply. Demodulated dc voltages associated with the mark and space frequencies are recovered with a single external capacitor in a dc retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 5.8 shows a high-frequency FSK decoder designed for input frequency deviations of ± 1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from Figure 5.9(a) to be approximately 40pF. A trimmer capacitor was added to fine tune f_o' to 10.8MHz.

Figure 5.9(b) indicates that the ± 1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_o' frequencies.

A more thorough analysis confirms these lock range conclusions and serves as a guide for designing other systems. The closed loop gain of the PLL is equal to the systems lock range and is found as the product of K_d and K_o, or

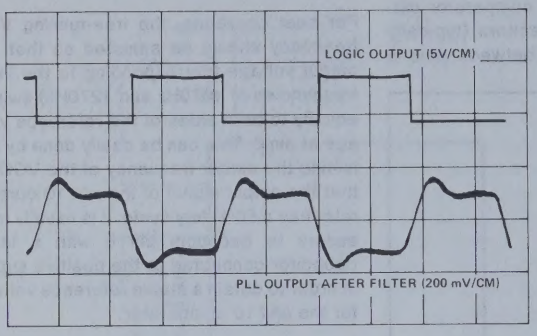
$$2\omega_L = K_V = K_d K_o \qquad (5.2)$$

$$2\omega_L = \left(0.64 \frac{\text{volt}}{\text{radian}}\right)\left(0.34 \frac{\text{radian}}{\text{volt}}\right)\left(2\pi \times 10.8 \times 10^6 \frac{\text{radian}}{\text{sec}}\right)$$

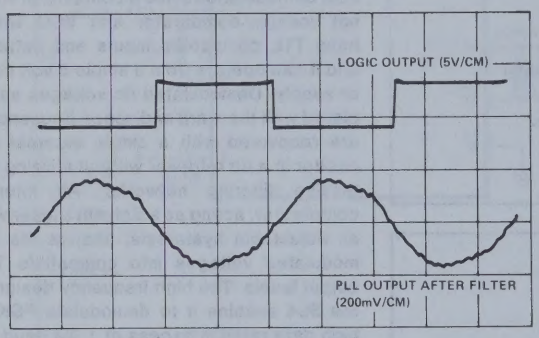
$$2\omega_L = 14.7\text{M} \frac{\text{radian}}{\text{sec}} \text{ (Lock range)}$$

FSK DECODING OUTPUT WAVESHAPES

(a) 100 BAUD



(b) 200 BAUD



(c) 300 BAUD

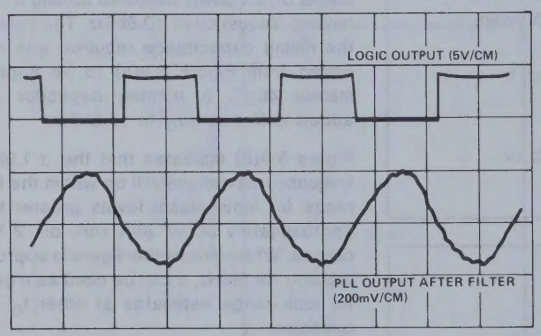


Figure 5.7

10.8 MHz FSK DECODER USING THE 564

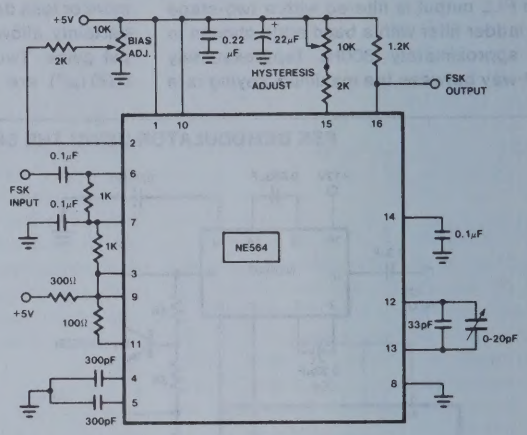
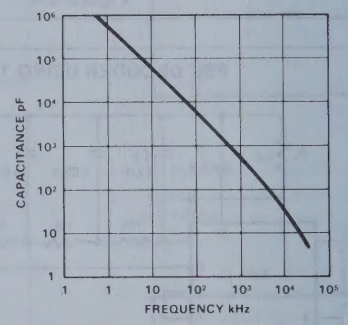


Figure 5.8

564 CHARACTERISTICS

(a) VCO TIMING CAPACITOR VERSUS FREQUENCY



(b) LOCK RANGE VERSUS INPUT SIGNAL LEVEL AND BIAS CURRENT

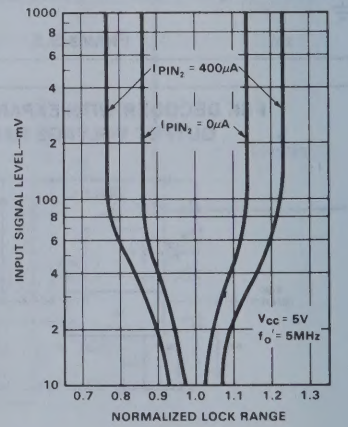
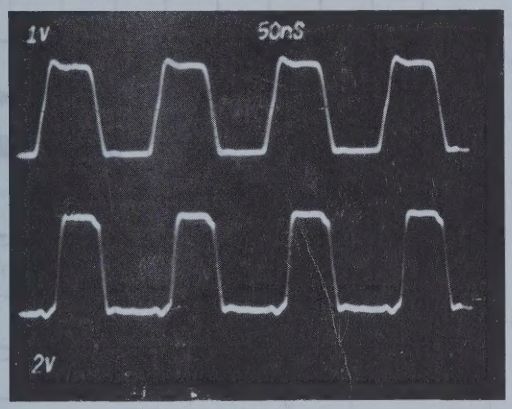


Figure 5.9

PLL INPUT AND VCO OUTPUT FOR PHASE AND FREQUENCY LOCK AT 10.8 MHz



f_L = 1.17 MHz (tracking range about 10.8 MHz)

Figure 5.10

Thus pin 2 could be left as an open circuit and the internally set closed-loop gain would be adequate for tracking the mark and space input frequencies. However, to be safe, a bias adjustment as shown in Figure 5.8 is recommended to allow for K_d and K_o variations from device to device.

Designing for a capture range of approximately 700kHz gives a low-pass filter time constant of

$$2\omega_c \simeq 2\sqrt{\frac{\omega L}{\tau}} \qquad (5.3)$$

$$2 \times (2\pi \times 700 \times 10^3) \simeq 2\sqrt{\frac{7.38 \times 10^6}{\tau}}$$

$$\tau = 0.381\mu s$$

Therefore, choose the low-pass filter capacitor as

$$C = \frac{\tau}{R} = \frac{0.381\mu s}{1.3K} = 293pF \qquad (5.4)$$

Two 300pF capacitors were selected for the design.

Capacitive coupling was used for the FSK input and is recommended to avoid dc feedthrough. This dc voltage would act as a dc offset to shift f_o' from 10.8MHz. Balanced biasing with the 1.0kΩ resistors from pin 7 to pins 3 and 6 also is recommended to establish symmetrical, quiescent current conditions in the limiter and phase comparator sections of the 564. The 300Ω pull-up resistor for the VCO output was found to give a rise time less than 10ns. This rise time was further reduced by adding the 100Ω resistor between pins 9 and 11. Figure 5.10 shows an unmodulated 10.8MHz input signal and the VCO output. Note the approximate 90° phase lag of the VCO output.

A 0.1μF dc retriever capacitor (pin 14) has less than 1 ohm impedance at f_o' and represents a good compromise between high baud rates (~100K baud) at f_o' and higher order filtering. If very high baud rates are used, this capacitor could be made smaller with an accompanying increase in the Schmitt trigger hysteresis voltage. The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 5.11 for 20K, 500K, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparators outputs.

The phase comparators outputs exhibit the waveshapes shown in Figure 5.12 when the FM input is changed from a square wave FSK modulation to a triangular sweep at a 100Hz modulation rate. The amplitude of the triangular sweep was increased from that used with square wave modulation, causing the loop to be driven in and out of lock. The loop is locked during the smooth, linear portions of the phase comparators waveshapes and unlocked during the remaining portions. Referring to Figure 1.6, lock and capture frequencies were measured for a pin 2 bias current of 375μA and f_o' = 10.8MHz as:

Lock: f_{L1} = 6.2MHz f_{L2} = 16.4MHz

Capture: f_{C1} = 9.3MHz f_{C2} = 12.2MHz

When the loop is locked, the phase detectors outputs represent the demodulated FM output. When unlocked, high frequency harmonics are present, increasing in amplitude until lock is achieved.

FM DEMODULATION

If the PLL is locked to a frequency modulated (FM) signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage, which forces the VCO to maintain lock with the input signal then becomes the demodulated FM output. The linearity of this demodulated signal depends solely on the linearity of the VCO voltage-to-frequency transfer characteristic. Since the PLL is in lock during FM demodulation, the response is linear and is readily predicted from a root locus plot. FM demodulation applications are numerous; some popular ones are FM broadcast demodulation and SCA decoding.

Broadcast FM Detection

Here the PLL functions as a complete IF strip, limiter, and FM detector, and can be used for detecting either wide or narrow band FM signals with greater linearity than can be obtained by other means. For frequencies within the range of the VCO, the PLL functions as a self contained receiver since it combines the functions of frequency selectivity and demodulation. One increasingly popular use of the PLL is in scanning receivers where a number of broadcast channels may be sequentially monitored by simply varying the VCO free-running frequency.

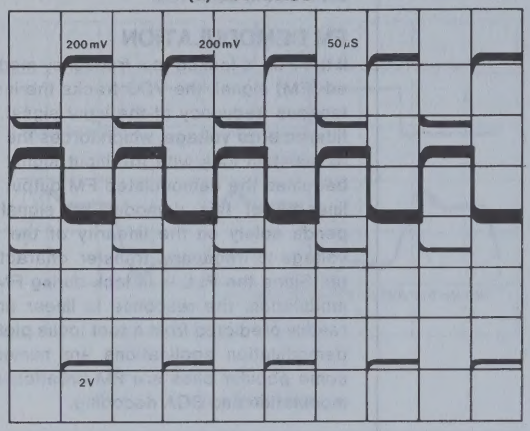
FM Demodulation Using the 560B

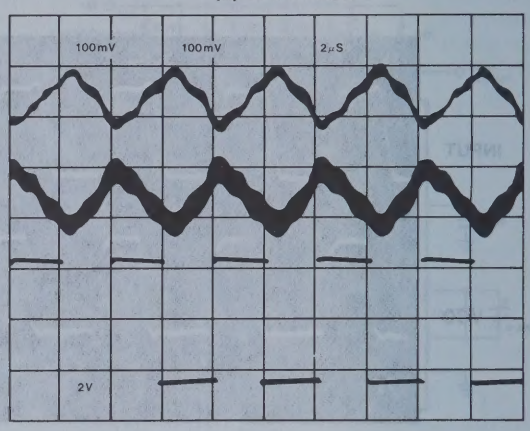
When used as a FM demodulator, the 560B PLL requires selection of external components and/or circuits to create the desired response. The areas to be considered are:

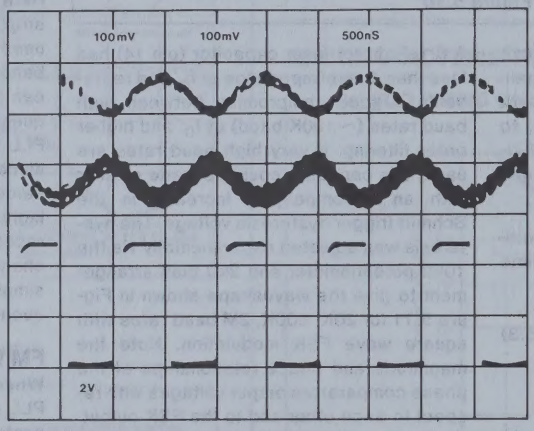
a Input Signal Conditioning
b Tuning — VCO Frequency
c Low Pass Filter Selection/Gain Adjustment
d Output Swing
e Tracking Range Adjustment
f De-emphasis Network Selection

Figure 5-13 illustrates schematically a typical FM demodulator with IF amplifier and limiter using the 560B PLL. The amplitude of the input signal has a pronounced effect on the operation. For the tracking range to be constant, the input signal level should be greater than 2mV rms. In addition, AM rejection diminishes at higher signal levels and drops to less than 20dB for signals greater than 30mV. If either tracking range or AM rejection is critical, the input signal should be conditioned to be in the 2 to 10mV range by using either a limiter or a combination limiter-amplifier. This circuit should limit at the smallest input voltage that is expected.

PHASE COMPARATOR (PINS 4 AND 5) AND FSK (PIN 16) OUTPUTS FOR DATA RATES OF







NOTE
Top trace-pin 4
Center trace-pin 5
Bottom trace-pin 16

Figure 5.11

PHASE COMPARATOR OUTPUTS SHOWING LOCK AND CAPTURE RANGES

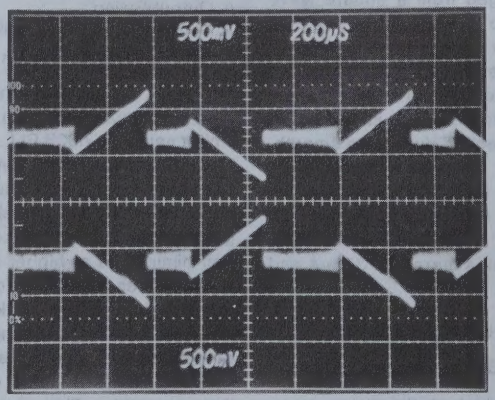


Figure 5.12

The PLL is tuned by adjusting the VCO to the center frequency of the FM signal. This is accomplished by connecting a capacitor across pins 2 and 3. The capacitor value is determined by

$$C_o \simeq \frac{300}{f_o'} \text{ pF} \quad (5.5)$$

where f_o' is the free running VCO frequency in MHz. The exact value is not important as the internal resistors are only within ± 10% of their nominal value and fine tuning is normally required. Fine tuning may be accomplished by using a trimmer capacitor in parallel with C_o or by using a potentiometer whose end terminals are connected between the power supply and ground and whose wiper is connected to pin 6 through a 200Ω current limiting resistor.

The low pass filter controls the capture range and hence the selectivity of the loop.

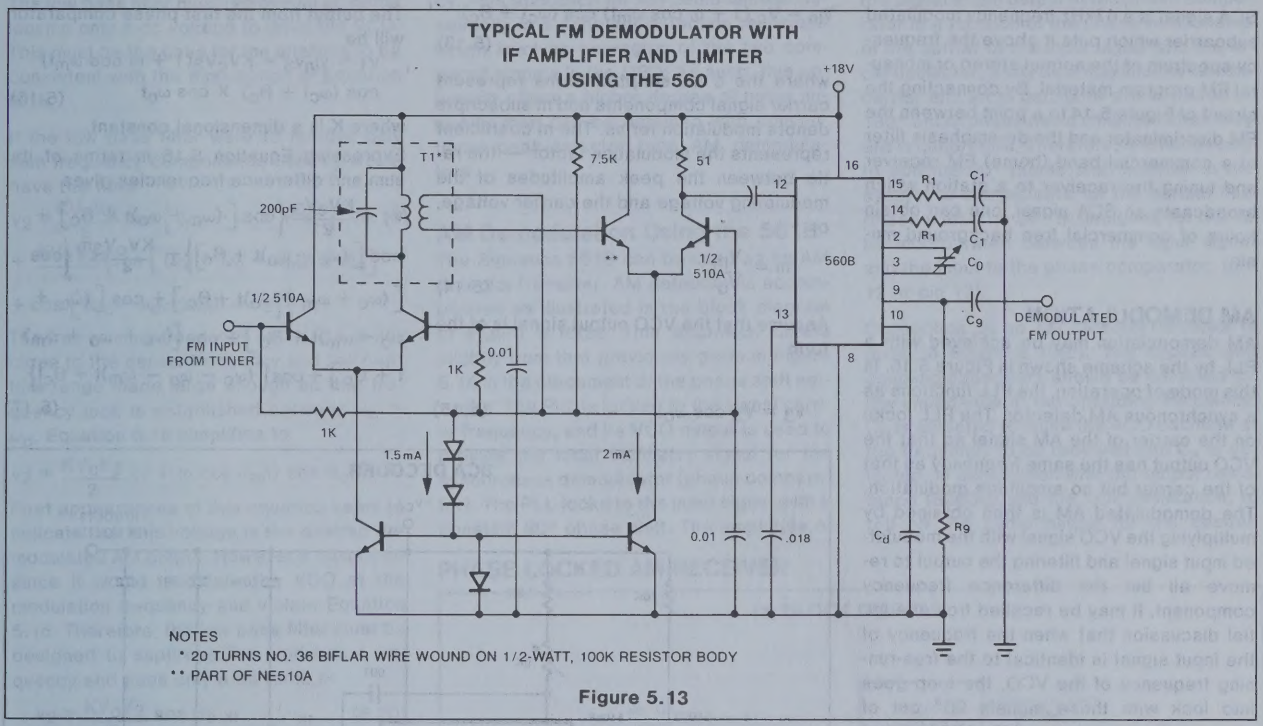


Figure 5.13

Implementation of the low pass filter can be made in either of two ways. The series combination of R_1 and C_1 connected to pins 14 and 15 as shown in Figure 5.13 uses R_1 and C_1 to set the bandwidth (in Hz) of the demodulated information according to

$$BW = \frac{1}{2\pi C_1 (R_1 + R_A)} \quad (5.6)$$

where R_A = 6kΩ and is the output resistance of the phase detector. For example, if the desired information bandwidth is 15kHz an $R_1 - C_1$ combination of 10kΩ and 700pF will produce the desired filtering.

An alternative way of implementing the low pass filter that is adequate for most applications is to connect a single capacitor, C_2, between pins 14 and 15. The capacitance value required can be approximated from

$$C_2 = \frac{1}{(2\pi)(BW)(2R_A)} = \frac{13.26}{BW}\ \mu F \quad (5.7)$$

where $2R_A$ represents the effective differential output resistance of the phase comparator. Here a single 885pF capacitor will provide the required filtering for the previous 15kHz bandwidth example.

The dc loop gain, which sets the lock range and threshold sensitivity, can be controlled by placing a resistor R_2 between pins 14 and 15. This resistor reduces the loop gain and the detection sensitivity by a factor of α where

$$\alpha = \frac{R_2}{R_2 + 2R_A} \quad (5.8)$$

Reduction of the loop gain may be desirable at high input signal levels (V_{IN} > 30mV) and at high frequencies (f_{IN} >5MHz) where excessively high loop gain may cause instability.

Simultaneously utilizing both R_2 and C_2 will cause some interactions. The α gain reduction factor remains as in Equation 5.8; however, the C_2 - BW expression of Equation 5.7 now becomes a function of R_2 according to

$$C_2 = \frac{1}{2\pi(BW)(2R_A + R_2)} \quad (5.9)$$

A combination of the series R_1 - C_1 network for bandwidth control and R_2 alone for α adjustment is recommended for independent filter and sensitivity adjustments.

The amplitude of the output voltage swing available at pin 9 is a function of the frequency deviation of the incoming signal and is approximately $0.3V_{p\text{-}p}$ for a ±1.0% deviation. For example, a standard 10.7MHz IF frequency has a deviation of ±75kHz; therefore, the percentage deviation is

$$\%\ dev. = \frac{\pm 0.075 \times 100\%}{10.7} = \pm 0.7\% \quad (5.10)$$

Therefore, the output voltage will be approximately

$$V_{OUT} = 0.3V_{p\text{-}p} \times \frac{0.7\%}{1.0\%} = 0.21V_{p\text{-}p} \quad (5.11)$$

This output level is equivalent to 74mV rms for 100% modulation. Pin 9 is an open emitter output. Therefore R_9 must be in place and can be used to set the drive current available for the next amplifier stage. The value of coupling capacitor C_9 determines the low frequency response of the demodulator.

The de-emphasis network requires an external capacitor from pin 10 to ground. This capacitor, C_d, and the internal 8kΩ resistance should produce a time constant of approximately 75μsec for standard FM broadcast demodulation. The value of this de-emphasis capacitor for this application is determined by

$$C_d = \frac{\tau}{R_{int}} = \frac{75 \times 10^{-6}}{8K} = 0.0094\mu F \quad (5.12)$$

For most applications, a 0.01μF value would be satisfactory since manufacturing tolerance of the resistor is in the order of ±10%.

SCA Demodulator Using the 565

This application involves demodulation of a frequency modulated subcarrier of the main channel. A popular example here is the use of the PLL to recover the SCA (Subsidiary Carrier Authorization or storecast music) signal from the combined signal of many commercial FM broadcast stations. The

SCA signal is a 67kHz frequency modulated subcarrier which puts it above the frequency spectrum of the normal stereo or monaural FM program material. By connecting the circuit of Figure 5.14 to a point between the FM discriminator and the de-emphasis filter of a commercial band (home) FM receiver and tuning the receiver to a station which broadcasts an SCA signal, one can obtain hours of commercial free background music.

AM DEMODULATION

AM demodulation may be achieved with a PLL by the scheme shown in Figure 5.15. In this mode of operation, the PLL functions as a synchronous AM detector. The PLL locks on the carrier of the AM signal so that the VCO output has the same frequency as that of the carrier but no amplitude modulation. The demodulated AM is then obtained by multiplying the VCO signal with the modulated input signal and filtering the output to remove all but the difference frequency component. It may be recalled from the initial discussion that when the frequency of the input signal is identical to the free-running frequency of the VCO, the loop goes into lock with these signals 90° out of phase. If the input is now shifted 90° so that it is in phase with the VCO signal and the two signals are mixed in a second phase comparator (multiplier), the average dc value (difference frequency component) of the phase comparator output will be directly proportional to the amplitude of the input signal.

To mathematically illustrate AM demodulation using a PLL in the system of Figure 5.15, consider an AM input voltage of the form

$$v_{in} = V_c (1 + m \cos \omega_m t) \cos (\omega_c t + \Theta_c) \quad (5.13)$$

where the c subscripted terms represent carrier signal components and m subscripts denote modulation terms. The m coefficient represents the modulation factor — the ratio between the peak amplitudes of the modulating voltage and the carrier voltage, or

$$m = \frac{V_m}{V_c} \quad (5.14)$$

Assume that the VCO output signal is of the form

$$v_3 = V_3 \cos \omega_o t \quad (5.15)$$

The output from the first phase comparator will be

$$v_1 = v_{in} v_3 = K V_c V_3 (1 + m \cos \omega_m t) \cos (\omega_c t + \Theta_c) \times \cos \omega_o t \quad (5.16)$$

where K is a dimensional constant.

Expressing Equation 5.16 in terms of its sum and difference frequencies gives

$$v_1 = \frac{K V_c V_3}{2} \left\{ \cos \left[(\omega_c + \omega_o)t + \Theta_c \right] + \cos \left[(\omega_c - \omega_o)t + \Theta_c \right] \right\} + \frac{K V_c V_3 m}{4} \left\{ \cos \left[(\omega_c + \omega_m + \omega_o)t + \Theta_c \right] + \cos \left[(\omega_c + \omega_o - \omega_m)t + \Theta_c \right] + \cos \left[(\omega_c - \omega_o + \omega_m)t + \Theta_c \right] + \cos \left[(\omega_c - \omega_o - \omega_m)t + \Theta_c \right] \right\} \quad (5.17)$$

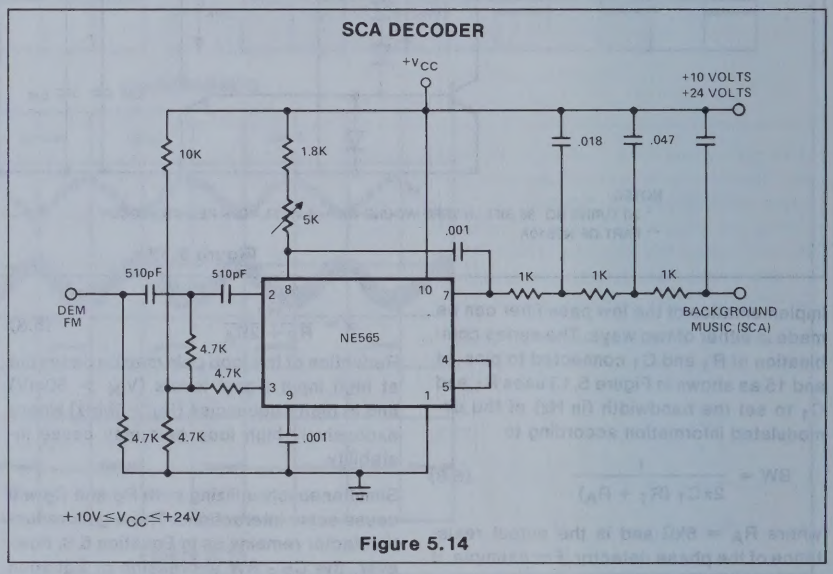


Figure 5.14

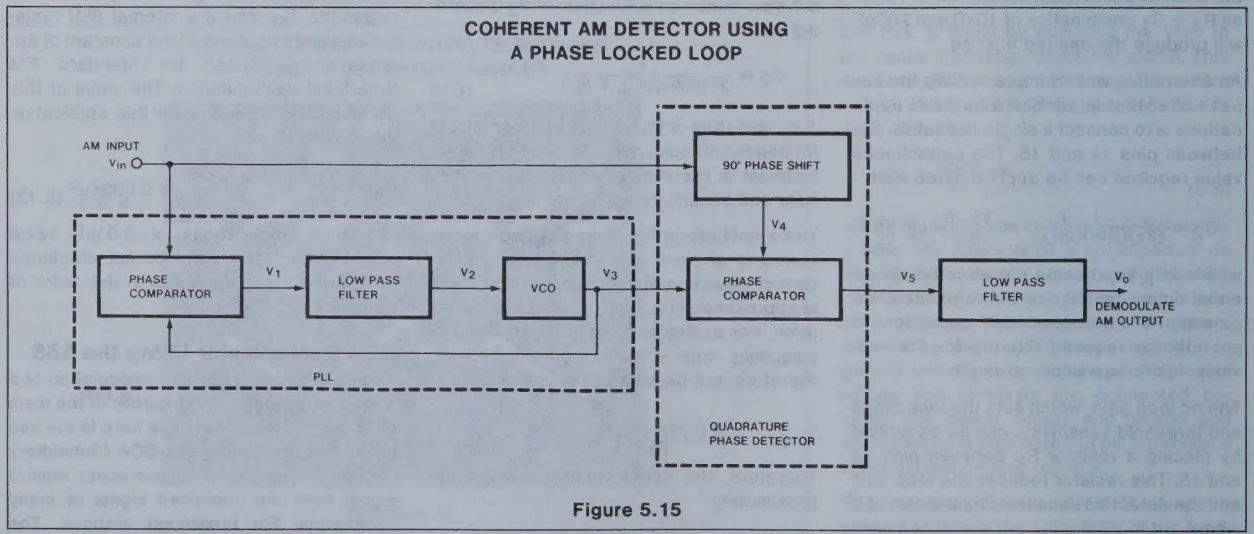


Figure 5.15

The low pass filter must remove all ac terms leaving only a dc voltage to drive the VCO. This must be the case for the analysis to be consistent with the assumption of Equation 5.15.

If the low pass filter were to remove only sum frequency components, then v_2 would have the form

$$v_2 = \frac{KV_cV_3}{2}\cos\left[(\omega_c - \omega_o)t + \Theta_c\right] \quad (5.18)$$
$$+ \frac{KV_cV_3}{4}\left\{\cos\left[(\omega_c - \omega_o + \omega_m)t + \Theta_c\right]\right.$$
$$\left. + \cos\left[(\omega_c - \omega_o - \omega_m)t + \Theta_c\right]\right\}$$

The free-running frequency of the PLL is set close to the carrier frequency and the capture range made large enough so that frequency lock is established between $\omega_c = \omega_o$. Equation 5.18 simplifies to

$$v_2 = \frac{KV_cV_3}{2}(1 + m\cos\omega_m t)\cos\Theta_c \quad (5.19)$$

First appearances of this equation seem to indicate that this voltage is the desired demodulated AM output. However it cannot be since it would modulate the VCO at the modulation frequency and violate Equation 5.15. Therefore, the low pass filter must be designed to suppress the modulation frequency and pass only a dc term, or

$$v_2 = \frac{KV_cV_3}{2}\cos\Theta_c \quad (5.20)$$

The constant phase shift network associated with the quadrature phase detector shifts the phase of v_{in} by 90° so that

$$v_4 = V_c(1 + m\cos\omega_m t)\cos \quad (5.21)$$
$$(\omega_c t + \Theta_c - 90°)$$
$$v_4 = V_c\,(1 + m\cos\omega_m t)\sin(\omega_c t + \Theta_c)$$

The second phase comparator multiplies v_3 and v_4 to give

$$v_5 = K_1\,V_3\,V_c\,(1 + m\cos\omega_m t)$$
$$\sin(\omega_c t + \Theta_c)\cos\omega_c t \quad (5.22)$$

where K_1 is a dimensional constant. Using trigonometric identities to simplify gives

$$v_5 = K_1V_3V_c\,(1 + m\cos\omega_m t)\left[\sin\right. \quad (5.23)$$
$$\left.(2\omega_c t + \Theta_c) - \tfrac{1}{2}(1 + \cos 2\omega_c t\right]$$

The second low pass filter is designed to suppress the carrier frequency harmonics and pass the modulation frequency so the demodulated output voltage appears as

$$v_o = \frac{K_1V_3V_c}{2}(1 + m\cos\omega_m t) \quad (5.24)$$

The mathematical analysis shows that the PLL low pass filter must have a very large time constant to reject the modulation frequency and keep the VCO locked to the carrier signal. Out of necessity the PLL will have a very narrow capture range, giving a high degree of selectivity centered about f_o'. Requirements for the second low pass filter are less stringent since this filter must reject only harmonics of the carrier frequency. This approach for AM demodulation essentially is a coherent detection technique which involves averaging of the two compared signals in the QPD. As such, this approach offers a higher degree of noise immunity than can be obtained with conventional peak-detector type AM demodulators.

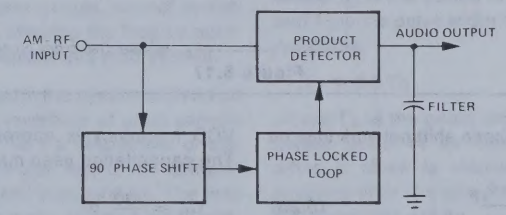
AM Demodulation Using the 561B

The Signetics 561B can be used as an AM detector/receiver. AM detection is accomplished as illustrated in the block diagram of Figure 5.16(a). This approach differs slightly from that previously given in Figure 5.15 in the placement of the phase shift networks. The PLL is locked to the signal carrier frequency, and its VCO output is used to provide the local oscillator signal for the synchronous demodulator (phase comparator). The PLL locks to the input signal with a constant 90° phase shift. The amplitude of the signal at the output of the phase comparator is a function of the phase relationship of the carrier of the input signal and the local oscillator; it will be a maximum when the carrier and local oscillator are in phase or 180° out of phase and a minimum when they are in quadrature. Therefore, it is necessary to add the 90° phase shift network in the system to compensate for the normal PLL phase shift. The 561 is designed for this to be incorporated between the input signal and the input to the phase comparator, (pin 12 or pin 13).

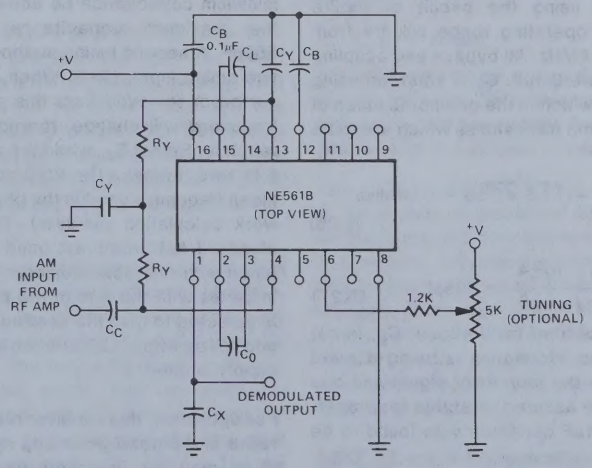
Connection as an AM detector/receiver is given in Figure 5.16(b). The bypass and coupling capacitors should be selected for low impedance at the operating frequency. C_o is selected to make the VCO oscillate at the frequency to be received and C_x is selected, in conjunction with the output resistance (8000Ω) and the load resistance, to roll off the audio output for the desired

PHASE LOCKED AM RECEIVER

(a) BLOCK DIAGRAM



(b) CIRCUIT IMPLEMENTATION USING THE 561



C_B = BYPASS CAPACITOR
C_C = COUPLING CAPACITOR

Figure 5.16

BLOCK DIAGRAM OF MISSING CLOCK REGENERATOR

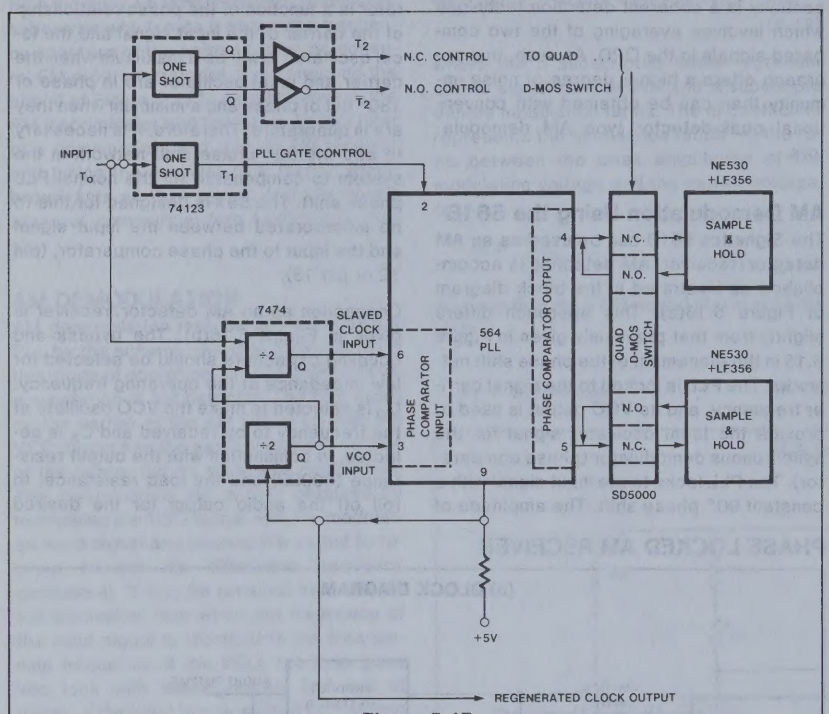


Figure 5.17

bandwidth. The phase shift network may be determined by

$$C_y = \frac{1.3 \times 10^{-4}}{f_c} F \qquad (5.25)$$

where f_c is the carrier frequency of the signal to be received and $R_y = 3000\Omega$. A receiver for standard AM reception is easily constructed using the circuit of Figure 5.16(b). Its operating range will be from 550kHz to 1.6MHz. All bypass and coupling capacitors are 0.1μF. C_y is selected using a frequency which is the geometric mean of the limits of the frequencies which are to be received.

$$f_c = \sqrt{f_{hi} f_{lo}} = \sqrt{1.6 \times 0.55} = 0.94MHz \qquad (5.26)$$

Then,

$$C_y = \frac{1.3 \times 10^{-4}}{0.94 \times 10^6} = 135pF \qquad (5.27)$$

The low pass filter for the loop, C_L, is not critical for no information is being derived directly from the loop error signal and one need only be assured of stable loop operation. A 0.01μF capacitor was found to be adequate.

Tuning may be accomplished in several ways. The simplest method uses a variable capacitor as C_o. It should be trimmed so that when set for minimum capacitance, the VCO frequency is approximately 1.6MHz. The capacitance used may be obtained by

$$C_o \approx \frac{300}{f_o} pF \qquad (5.28)$$

where f_o is in MHz.

Application of this formula shows that the minimum capacitance be about 180pF and the maximum capacitance should be 550pF. A second tuning method utilizes the fine tuning input, pin 6. When current is inserted or removed from this pin, the VCO frequency will change, thereby tuning the receiver. Select C_o, when the current at pin 6 is zero, to make the VCO operate at the mean frequency used in the phase shift network calculation (940kHz). The complete standard AM broadcast band may now be tuned with one potentiometer. The resistor in series with the arm of the potentiometer is selected to give the desired tuning range and will be about 1200Ω when an 18V power supply is used.

For operation, this receiver requires an antenna and a good grounding system. Operation may be improved by including a broadband untuned RF amplifier, but care should be used to ensure that the phase locked loop is not overdriven, e.g. input signals should be kept less than 0.5V rms.

CLOCK REGENERATION

Recovery of missing clocks on data transmission lines is a problem which has always faced designers. With the 564 phase locked loop and some peripheral control elements, a high quality clock recovery (or clock regeneration) can be designed that has the ability to deal with many consecutive missing clock pulses (8 or more) without the loss of clock integrity (frequency and phase). As such, the 564 clock recovery system is extremely desirable in PCM systems where the clock is effectively an integral portion of the data and may be buried in either a stream of zeros (0's) or ones (1's). A non-return-to-zero (NRZ) data system is a good example of this type of transmission.

Once clock information has been recovered, the data stream information can be properly converted back into its coded format and then translated. Phase error in a PCM system determines which type of clock recovery system to incorporate.

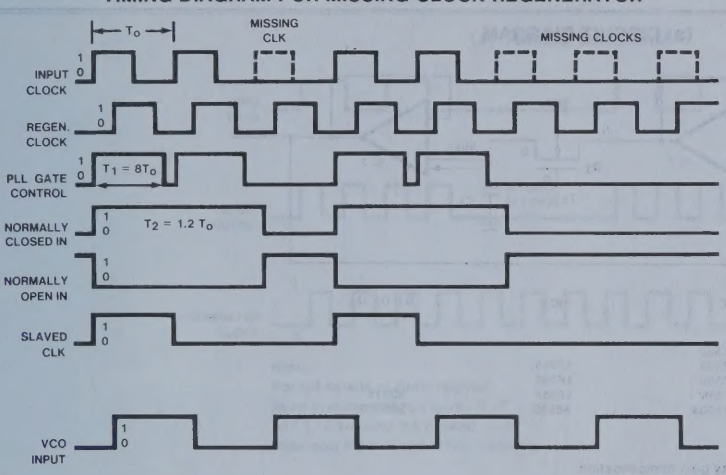
The general approach for the 564 design is one which will guarantee minimm phase shift conditions even when up to 8 (or more, depending on peripheal design) clock pulses are missing or buried in the transmitted data.

Figure 5.17 shows the block diagram of a "missing clock regenerator". This nomenclature has been selected to indicate the true nature of the system which "regenerates" the missing information with proper phase and time relationships. Figure 5.18 shows the timing diagram of the missing clock regenerator.

The heart of the system is the 564 phase locked loop. The sample and hold system consists of a 530 high-performance operational amplifier, a LF356 Bi-Fet operational amplifier, and a SD5000 D-MOS quad analog switch. In addition, two discrete D-MOS switches are used to sense missing clock pulses enabling the sample and hold sysem to maintain a fixed reference voltage until the next clock pulse appears. To generate the proper timing pulses, a dual retriggerable one-shot (74123) is incorporated. A dual edge triggered flip-flop (7474) is used to insure that all inputs to the system are 50% duty cycle.

System Operation

The 564, like all analog PLLs, operates on the principle that the frequency and phase are proportional to the differential and common mode voltages at the phase comparator outputs, pins 4 and 5. Without a sample and hold system, removing the input signal



NOTE
1. Grounding Pin 2 voltage, turns PLL phase comparator and limiter off.
2. Differential and common mode voltages at phase comparators loop filers are proportional to sample and hold droop characteristics.

Figure 5.18

causes the VCO of the PLL to oscillate at its free-running frequency, f_o'. As this happens the phase comparators output voltages change. The clock regeneration system incorporates a sample and hold system to maintain the phase comparators output voltages. These sample and hold systems (one for each output port of the phase comparator) sense the missing clock information and force the phase comparators common-mode and differential-mode voltages to remain at the exact levels they were prior to loss of clock pulses. By keeping these voltage levels fixed, the VCO frequency and phase of the 564 will remain constant with respect to the incoming clock. Also, lock-up time and phase jitter with respect to the next incoming clock signal is minimal.

Figure 5.19 shows the sample and hold circuitry and its associated timing. Essentially when all clock pulses are present, switch Q1 stays on, switch Q2 remains off, and switch Q3 is sampled at a 10% duty cycle in anticipation of a missing clock and to avoid feedback of switching glitches into the phase comparator loop filter ports of the 564 (pins 4 and 5). When a clock pulse is missing, switch Q3 stays open allowing no more charge transfer to capacitor C_1. With the Bi-Fet op amp (LF356) the output voltage droop is approximately $0.01\mu V/\mu s$. This droop rate depends on capacitor C_1 and the load on the output of the LF356. During the hold mode switch Q1 opens and switch Q2 closes, forcing the stored voltage conditions on capacitor C_1 into the phase comparator output ports. As soon as the next clock pulse occurs, normal switch conditions return allowing the loop to operate without the sample and hold system.

The errors involved in the system depend on the tracking and matching of each sample and hold circuit to its respective phase comparator output port and to the complementary sample and hold system. The first function determines the common-mode voltage levels; the latter function determines the differential-mode voltage, which is directly proportional to jitter or phase distortion.

Referring to Figure 5.17 the PLL Gate Control function (pin 2) of the 564 is pulled to ground when a clock pulse is missing. This action shuts off the input limiter and the phase comparator of the 564. (See Figure 4.16 - the current sinks of Q4 and Q15 have their bases grounded, thereby forcing the internal limiter and phase comparator currents to zero.)

Timing pulses from the incoming clock data are shown in the timing diagram of Figure 5.18. With the basic clock frequency known, the periods T_0, T_1, and T_2 can be determined. The period T_0 is that of the external system clock, and its reciprocal should be used as the 564s free-running frequency. The dual retriggerable one shot (74123) generates T_1, $\overline{T_2}$, and T_2. The duration of the first pulse is set slightly lower than the system clock period. This pulse is used to gate the 564 on and off, and also acts as the anticipate trigger for the missing clock. If a clock pulse is missing the T_1 pulse will stay low, keeping the PLL phase comparator turned off and opening switch Q3 of the sample and hold circuit (Figure 5.19 (b)). T_2 and $\overline{T_2}$ are compliments and have a pulse length slightly longer than the basic clock period. The retriggerable feature of the 74123 will always keep the outputs high and low respectively until a clock pulse is missing, at which point the outputs switch state.

Under normal conditions of no clock pulses missing, T_2 will be high keeping the switch Q1 on, and $\overline{T_2}$ will be low keeping switch Q2 off. When a clock pulse is missing, these switches will change state. Figure 5.19(a) indicates source and drain configurations for minimum pulse feed-through. (D-MOS switches have gate-to-drain capacitances an order of magnitude lower than the gate-to-source capacitance.) With respect to the normal period of the switching pulses the following conditions prevail.

For switches Q1 and Q2

$$T_2 = 1.2\ T_0 \qquad (5.29)$$

where T_0 is the period of the system clock and T_2 is the pulse width of the positive output pulse.

$$T_1 = 0.8\ T_0 \qquad (5.30)$$

where T_1 is the pulse width of the positive output pulse of its one-shot. Therefore, when a clock is missing, the maximum tracking error the sample and hold system will encounter will be

$$T_{error} = T_2 - T_1 = 0.4\ T_0 \qquad (5.31)$$

If the system frequency is 1MHz, T_0 is $1.0\mu s$ so that

$$T_{error} = 400ns \qquad (5.32)$$

The maximum droop during this period will be less than $1\mu V$. Using this number and the K_o and K_d functions of the 564 produces a phase shift of less than 1.0 degree.

The 7474 Dual-D Flip-Flop is incorporated in the system to guarantee 50% duty cycle inputs to the 564. Using 50% duty cycle signals greatly reduces the possibility of the PLL locking on a signal other than the fundamentl clock frequency. Since both the clock input signal and the VCO input to the phase comparator are divided by 2, the VCO output frequency is equal to the system clock frequency.

NRZ Clock Regeneration

A PCM signal consists of a series of binary digits, or bits, occurring at a periodic rate. The weight of each bit ("zero" or "one") is random but the duration of each bit, and

SAMPLE AND HOLD SYSTEM

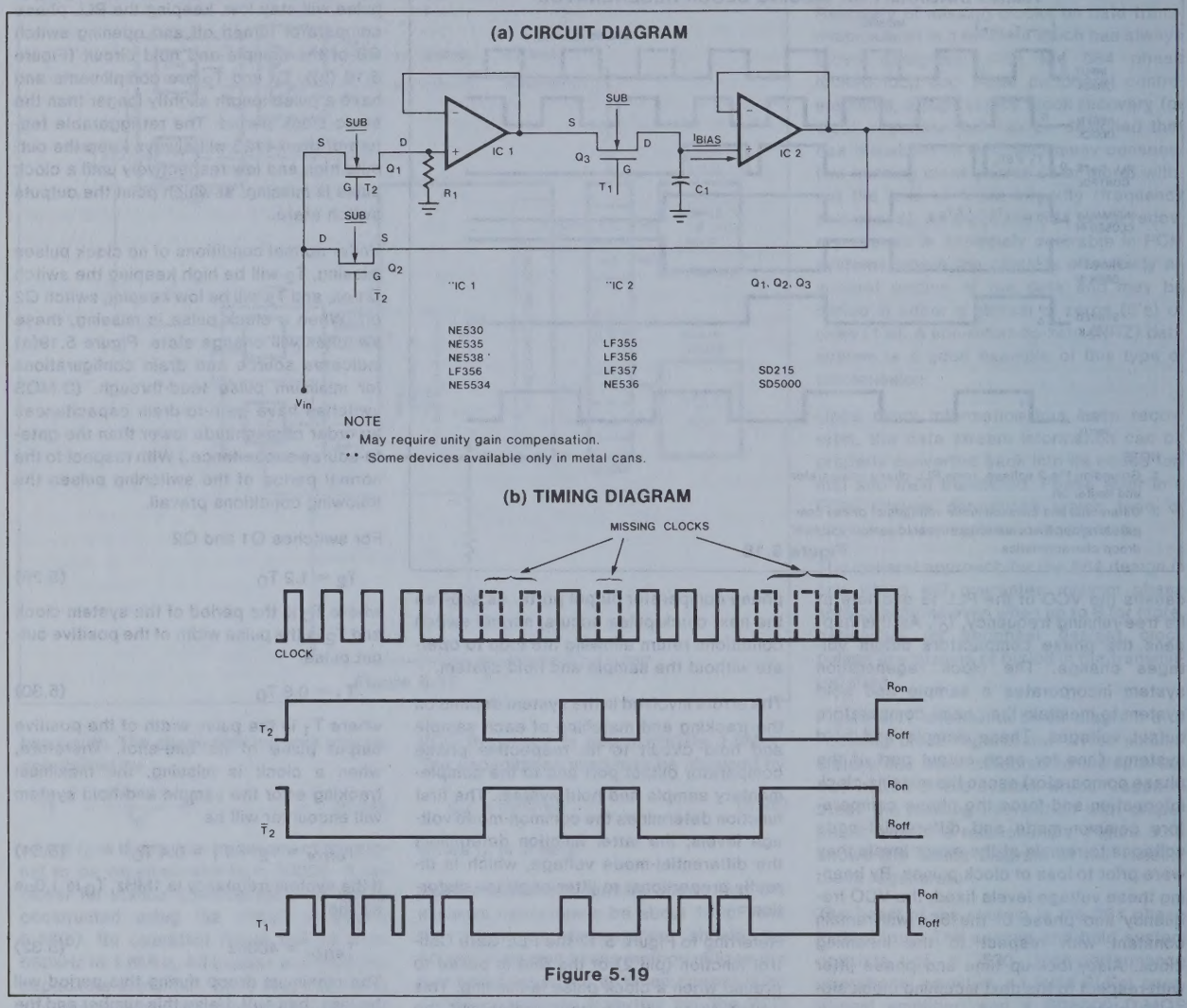


Figure 5.19

therefore the periodic "bit rate", is constant. For detection and further processing of the digits it is necessary to have a "clock" that is coherent with the bit rate. This clock must ordinarily be derived from the incoming data stream. Phaselock techniques are widely used to recover the clock from the data (11).

Some form of Nonreturn-to-Zero (NRZ) modulation is almost always used to maximize data rate in a given transmission bandwidth. In a truly random NRZ bit stream, there are no discrete frequency components present. Specifically, there is no component at the bit rate. In fact, the continuous spectrum of an NRZ wave has a null at the bit frequency.

An NRZ signal may be regarded as lacking a "carrier" which must be reconstructed from information contained within the signal. It is impossible to recover the clock merely by applying the input signal to the phase lock loop; there is nothing on which the loop can lock.

Timing information in a PCM signal is carried in the data transitions; th time of a transition marks one boundary of an individual bit. Transitions can have either positive or negative direction, but both polarities have the same meaning for time recovery. If a series of unidirectional pulses is generated to mark transition times, there will be a discrete component of the bit frequency in the pulse train and a loop can be locked to it.

NRZ systems operate with transition occurring only when clocks are present. If data does not change as many as 8 clock pulses can be missing. By incrporating the Signetics 8T20 Bi-Directional One Shot as shown in Figure 5.20, the NRZ data stream can be incorporated in a "missing clock format" and fed into the missing clock generator network as indicated.

All PCM recovery systems must have the following two properties in common:

1 A method of locating the data transitions. This is normally performed by some kind of linear differentiating or differencing operation.

2 A form of rectification that converts the transition information to a usable form. This operation is necessarily a second-order (or higher even-order) nonlinearity.

NRZ CLOCK REGENERATOR

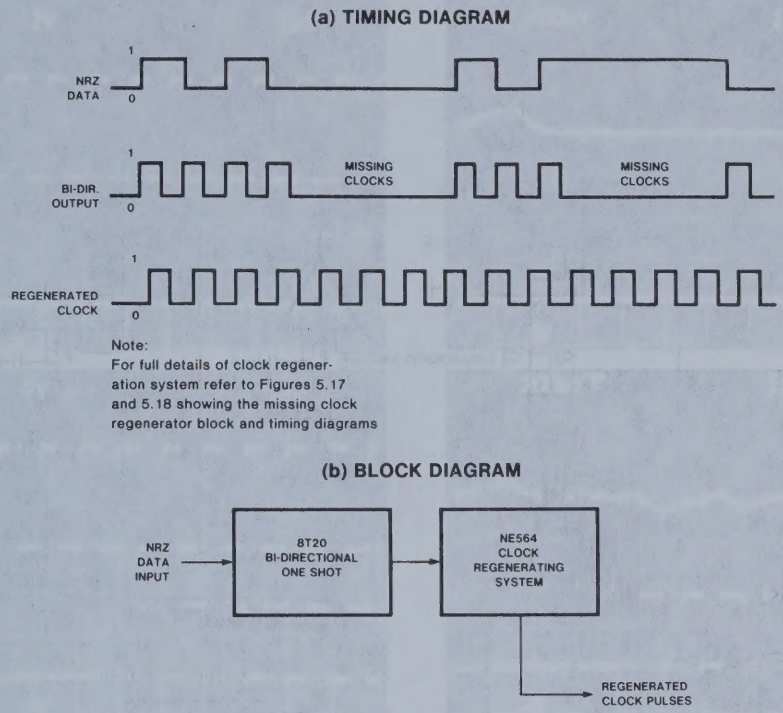


Figure 5.20

The circuit diagram for an NRZ system using the 564 is shown in Figure 5.21. Experimental waveshapes obtained with this system operating at a 1.0MHz data rate are shown in Figure 5.22. The 564 remained in lock for up to 15 missing clock pulses. The waveshapes show system operation for 4 and 8 missing clock pulses.

TONE DECODER APPLICATIONS (567)

The 567 is a special purpose PLL intended solely for use as a tone decoder. It contains a complete PLL including VCO, phase comparator, and amplifier as well as a quadrature phase detector or multiplier. If the signal amplitude at the lock frequency is above a minimal value, the driver amplifier turns on, driving a load with as much as 200mA. Thus the 567 gives an output whenever an inband tone is present. The 567 is optimized for both free-running frequency and bandwidth stability.

Dual Tone Decoder

Two 567 tone decoders connected as shown in Figure 5.23(a) permit decoding of simultaneous or sequential tones. Both units must be on before an output is given. R_1C_1 and $R_1'C_1'$ are chosen respectively for tones 1 and 2. If sequential tones (tone 1 followed by tone 2) are to be decoded, then C_3 is made very large to delay turn off of unit 1 until unit 2 has turned on and the NOR gate is activated. Note that the wrong sequence (tone 2 followed by tone 1) will not provide an output since unit 2 will turn off before unit 1 comes on. Figure 5.23(b) shows a circuit variation which eliminates the NOR gate. The output is taken from unit 2, but the unit 2 output stage is biased off by R_{L1} and D_1 until activated by tone 1. A further variation is given in Figure 5.23(c). Here, unit 2 is turned on by the unit 1 output when tone 1 appears, reducing the standby power to half. Thus, when unit 2 is on, tone 1 is or was present. If tone 2 is now present, unit 2 comes on also and an output is given. Since a transient output pulse may appear during unit 1 turn on, even if tone 2 is not present, the load must be slow in response to avoid a false output due to tone 1 alone.

High-Speed, Narrow-Band Tone Decoder

The circuit of Figure 5.23(a) may be used to obtain a fast, narrow-band tone decoder. The detection bandwidth is achieved by overlapping the detection bands of the two tone decoders. Thus, only a tone within the overlap portion will result in an output. The input amplitude should be greater than 70mV rms at all times to prevent detection band shrinkage and C_2 should be between $130/f_o$ and $1300/f_o\mu F$ where f_o is the nominal detection frequency. The small value of C_2 allows operation at the maximum speed so that worst-case output delay is only about 14 cycles.

Touch-Tone® Decoder

Touch-Tone® decoding is of great interest since all sorts of remote control applications are possible if you make use of the encoder (the pus-button dial) that will ultimately be part of every phone. A low cost decoder can be made as shown in Figure 5.24. Seven 567 tone decoders, their inputs connected in common to a phone line or acoustical coupler, drive three integrated NOR gate packages. Each tone decoder is tuned, by means of R_1 and C_1, to one of the seven tones. The R_2 resistor reduces the bandwidth to about 8% at 100mV and 5% at 50mV rms. Capacitor C_4 decouples the seven units. The seven R_2 resistors and capacitor C_4 can be eliminated at the expense of a somewhat slower response at

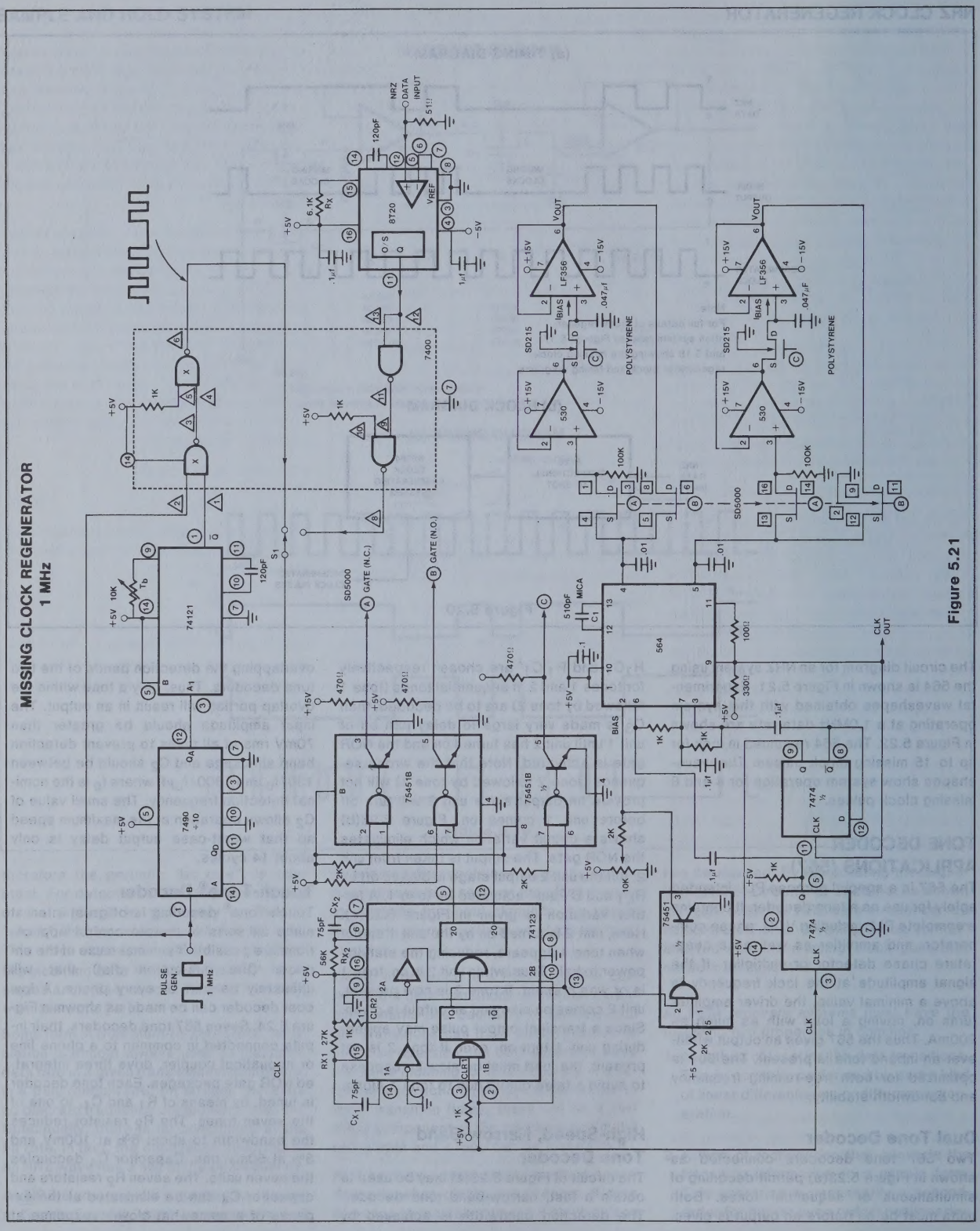

MISSING CLOCK REGENERATOR
1 MHz
NRZ DATA INPUT
8T20
VREF
7400
74121
7490
÷10
75451B
74123
564
LF356
530
SD215
SD5000
POLYSTYRENE
VOUT
IBIAS
GATE (N.C.)
GATE (N.O.)
PULSE GEN.
1 MHz
CLK
CLK OUT
BIAS
MICA
510pF
100Ω
330Ω
470Ω
100K
10K
2K
1K
56K
27K
75pF
120pF
.047μF
.1μF
1μF
+5V
−5V
+15V
−15V

Figure 5.21

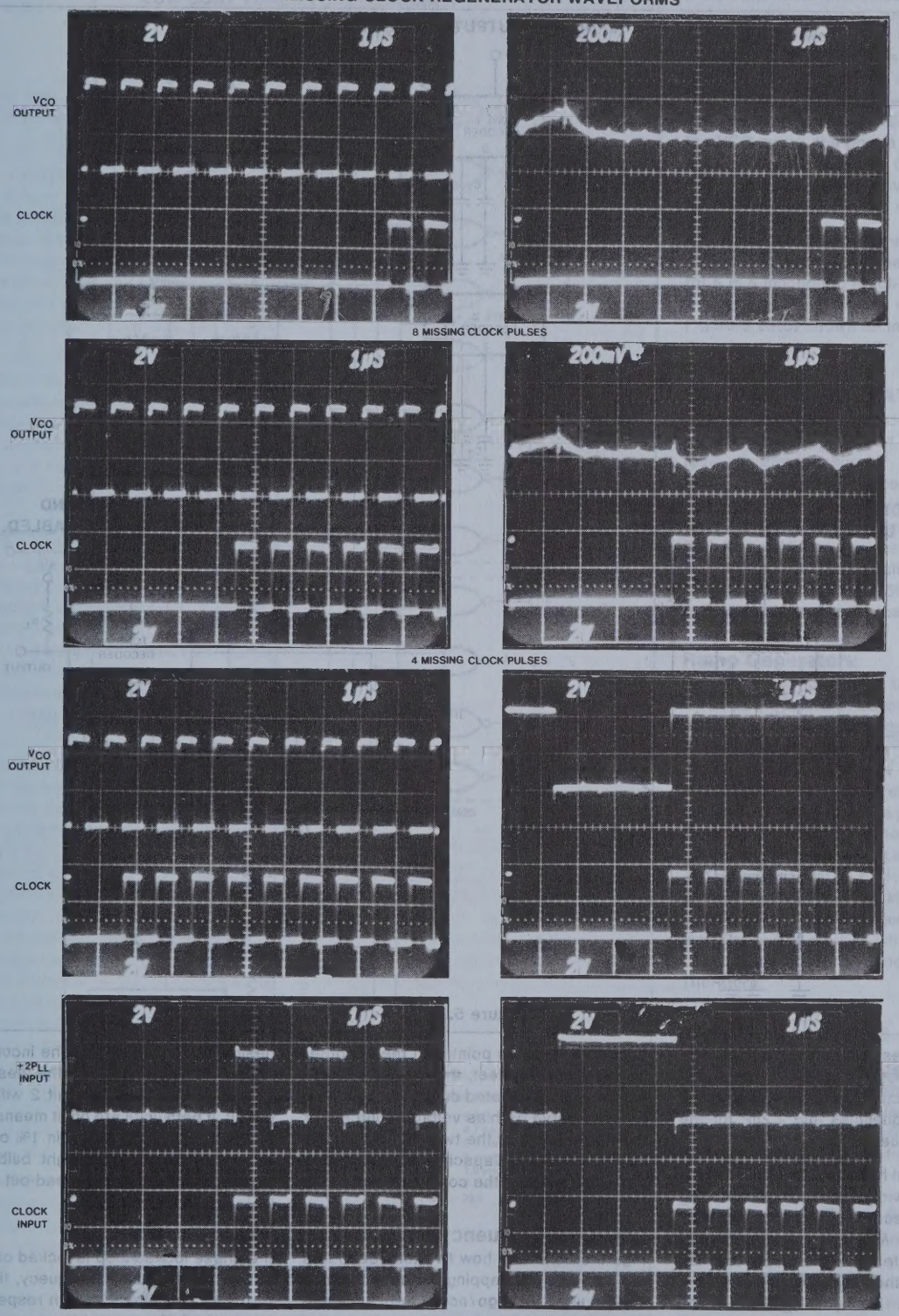
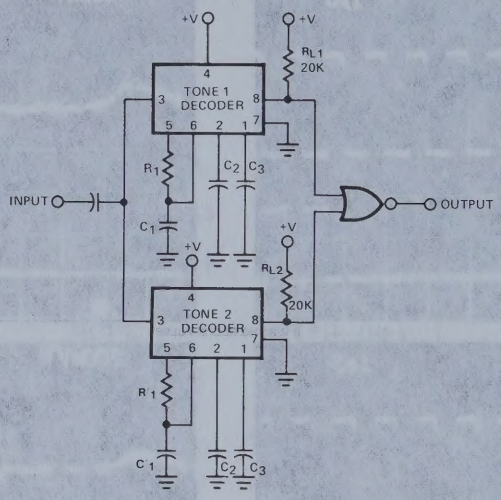

MISSING CLOCK REGENERATOR WAVEFORMS
2V
1μS
200mV
VCO OUTPUT
CLOCK
PIN 4 DC VOLTAGE
CLOCK INPUT
8 MISSING CLOCK PULSES
4 MISSING CLOCK PULSES
N.C. SWITCH CONTROL
+2PLL INPUT
NC SWITCH CONTROL

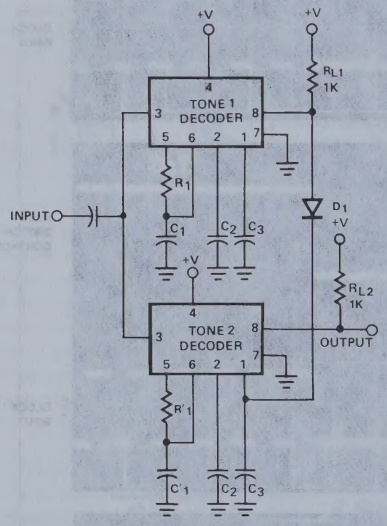
Figure 5.22

DETECTION OF TWO SIMULTANEOUS OR SEQUENTIAL TONES

(a) NORING OUTPUTS TOGETHER



(B) DISABLING THE SECOND DECODER UNTIL ENABLED BY THE FIRST



(C) BLOCKING POWER TO THE SECOND DECODER (PIN 7) UNTIL THE FIRST IS ENABLED.

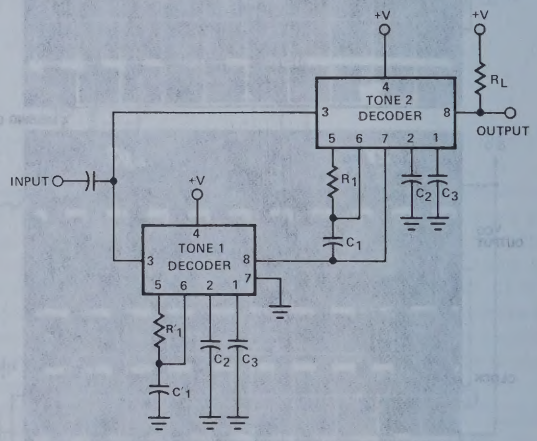


Figure 5.23

low input volages (50 to 100mV rms). The bandwidth can be controlled in the normal manner by selecting C_2 to be 4.7μF for the three lower frequencies and 2.2μF for the four higher frequencies.

The only unusual feature of this circuit is the means of bandwidth reduction using the R_2 resistors. As shown in the 567 data sheet under *Alternate Method of Bandwidth Reduction,* an external resistor R_A can be used to reduce the loop gain and, therefore, the bandwidth. Resistor R_2 serves the same function as R_A except that instead of going to a voltage divider for dc bias, it goes to a common point with the six other R_2 resistors. In effect, the five 567s which are not being activated during the decoding process serve as bias voltage sources for the R_2 resistors of the two 567s which are being activated. Capacitor C_4 decouples the ac currents at the common point.

Low-Cost Frequency Indicator

Figure 5.25 shows how two tone decoders set up with overlapping detection bands can be used for a go/no-go frequency meter. Unit 1 is set 6% above the desired sensing frequency and unit 2 is set 6% below the desired frequecy. Now, if the incoming frequency is within 13% of the desired frequency, either unit 1 or unit 2 will give an output. If both units are on, it means that the incoming frequency is within 1% of the desired frequency. Three light bulbs and a transistor allow low cost read-out.

Phase Modulator

If a phase locked loop is locked onto a signal at the free-running frequecy, the phase of the VCO will be 90° with respect to the input signal. If a current is injected into the VCO terminal (the low pass filter output),

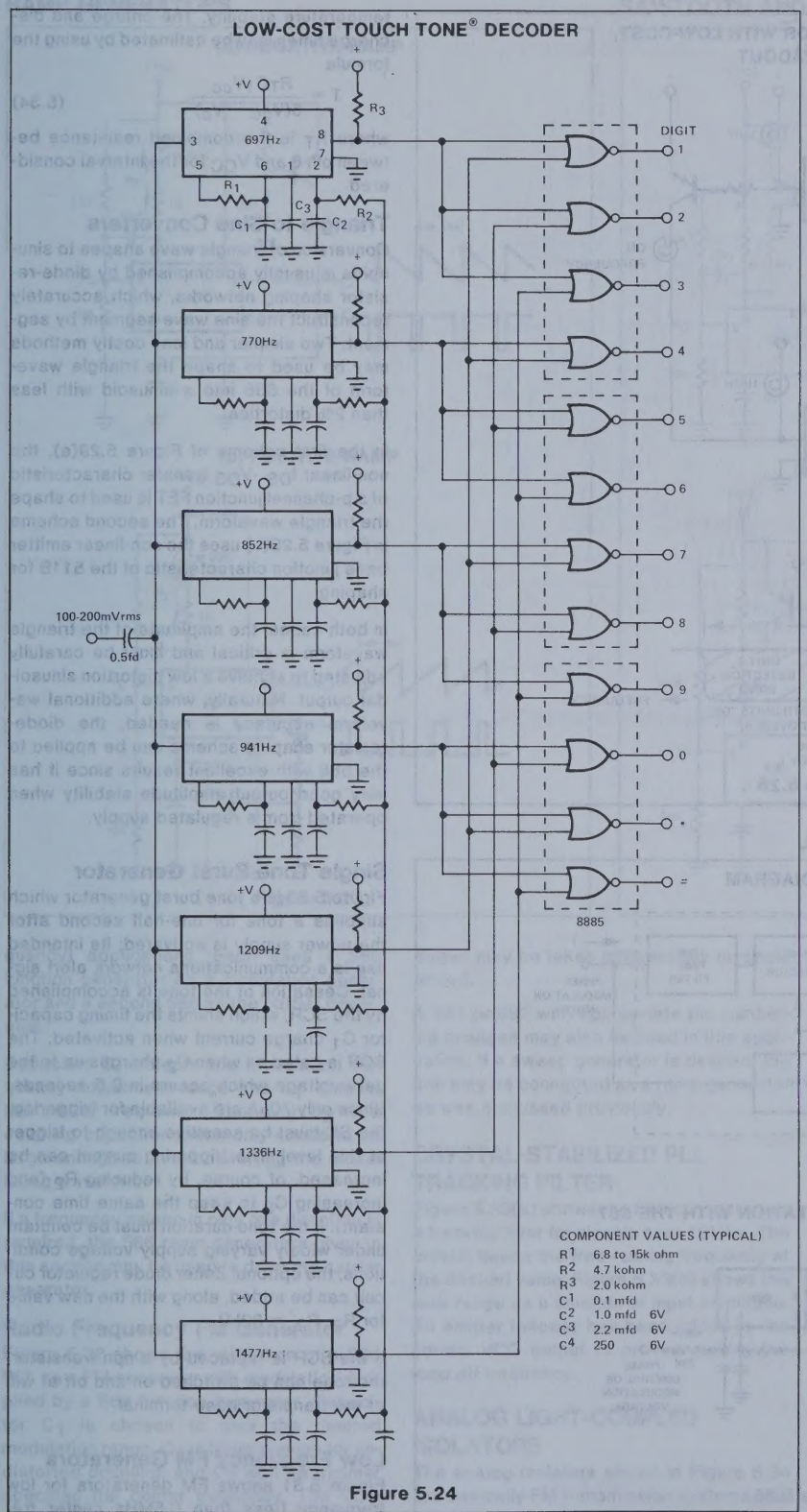


Figure 5.24

the phase will shift sufficiently to develop an opposing average current out of the phase comparator so that the VCO voltage is constant and lock is maintained. When the input signal amplitude is low enough so that the loop frequency swing is limited by the phase comparator output rather than the VCO swing, the phase can be modulated over the full range of 0 to 180°. If the input signal is a square wave, the phase will be a linear function of the injected current.

A block diagram of the phase modulator is given in Figure 5.26(a). The conversion factor K is a function of which loop is used, as well as the input square wave amplitude. Figure 5.26(b) shows an implementation of this circuit using the 567.

WAVEFORM GENERATORS

The oscillator portion of many of the PLLs can be used as a precision, voltage-controllable waveform generator. Specifically, the 566 Function Generator contains the oscillator of the 565 PLL. Most of the applications which follow are designs using the 566. Many of these designs can be modified slightly to utilize the oscillator section of the 560, 561, 562, and 564 if higher frequency performance is desired.

Ramp Generators

Figure 5.27 shows how the 566 can be wired as a positive or negative ramp generator. In the positive ramp generator, the external transistor driven by the pin 3 output rapidly discharges C_1 at the end of the charging period so that charging can resume instantaneously. The pnp transistor of the negative ramp generator likewise rapidly charges the timing capacitor C_1 at the end of the discharge period. Because the circuits are reset so quickly, the temperature stability of the ramp generator is excellent. The period τ is $\frac{1}{2} f_o$ where f_o is the 566 free-running frequency in normal operation. Therefore,

$$T = \frac{1}{2f_o} = \frac{R_T C_1 V_{CC}}{5(V_{CC} - V_C)} \qquad (5.33)$$

where V_C is the bias voltage at pin 5 and R_T is the total resistance between pin 6 and V_{CC}. Note that a short pulse is available at pin 3. (Placing collector resistance in series with the external transistor collector will lengthen the pulse.)

Sawtooth and Pulse Generator

Figure 5.28 shows how the pin 3 output of the 566 can be used to provide different charge and discharge currents for C_1 so that a sawtooth output is available at pin 4 and a pulse at pin 3. The pnp transistor should be well saturated to preserve good

FREQUENCY DETECTOR WITH LOW-COST, LAMP READOUT

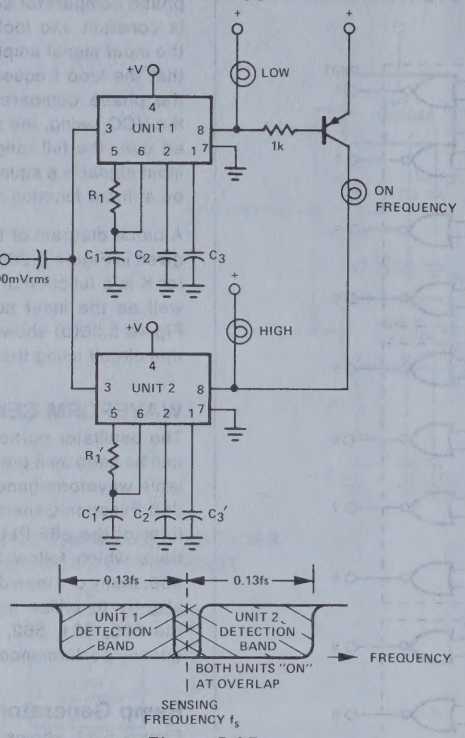
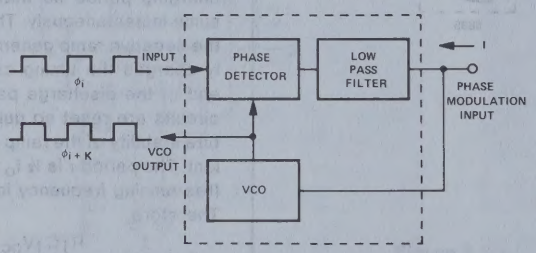


Figure 5.25

PHASE MODULATION USING THE PLL

(a) BLOCK DIAGRAM



(b) CIRCUIT IMPLEMENTATION WITH THE 567

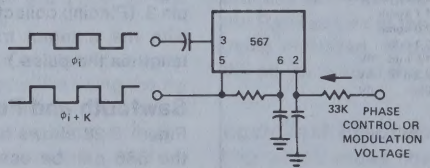


Figure 5.26

temperature stability. The charge and discharge times may be estimated by using the formula

$$T = \frac{R_T C_1 V_{CC}}{5(V_{CC} - V_C)} \qquad (5.34)$$

where R_T is the combined resistance between pin 6 and V_{CC} for the interval considered.

Triangle to Sine Converters

Conversion of triangle wave shapes to sinusoids is usually accomplished by diode-resistor shaping networks, which accurately reconstruct the sine wave segment by segment. Two simpler and less costly methods may be used to shape the triangle waveform of the 566 into a sinusoid with less than 2% distortion.

In the first scheme of Figure 5.29(a), the non-linear I_{DS} -V_{DS} transfer characteristic of a p-channel junction FET is used to shape the triangle waveform. The second scheme in Figure 5.29(b) uses the non-linear emitter base junction characteristic of the 511B for shaping.

In both cases, the amplitude of the triangle waveform is critical and must be carefully adjusted to achieve a low distortion sinusoidal output. Naturally, where additional waveform accuracy is needed, the diode-resistor shaping scheme can be applied to the 566 with excellent results since it has very good output amplitude stability when operated from a regulated supply.

Single Tone Burst Generator

Figure 5.30 is a tone burst generator which supplies a tone for one-half second after the power supply is activated; its intended use is a communications network alert signal. Cessation of the tone is accomplished by the SCR, which shunts the timing capacitor C_1 charge current when activated. The SCR is gated on when C_2 charges up to the gate voltage which occurs in 0.5 seconds. Since only 70μA are available for triggering, the SC must be sensitive enough to trigger at this level. The triggering current can be increased, of course, by reducing R_2 (and increasing C_2 to keep the same time constant). If the tone duration must be constant under widely varying supply voltage conditions, the optional Zener diode regulator circuit can be added, along with the new value for R_2, $R_2' = 82k\Omega$.

If the SCR is replaced by a npn transistor, the tone can be switched on and off at will at the transistor base terminal.

Low Frequency FM Generators

Figure 5.31 shows FM generators for low frequency (less than 0.5MHz center fre-

RAMP GENERATORS

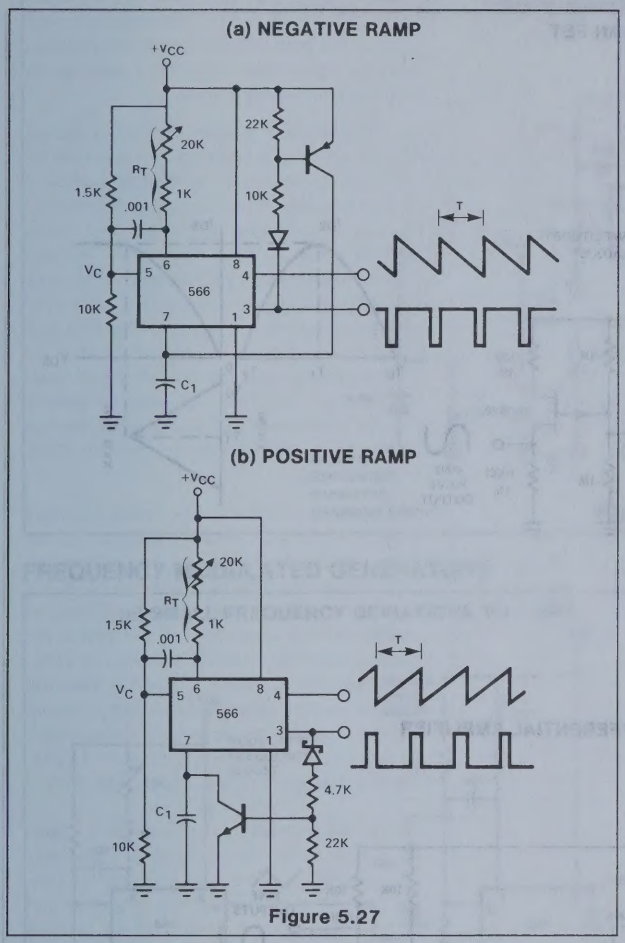


Figure 5.27

SAWTOOTH AND PULSE GENERATORS

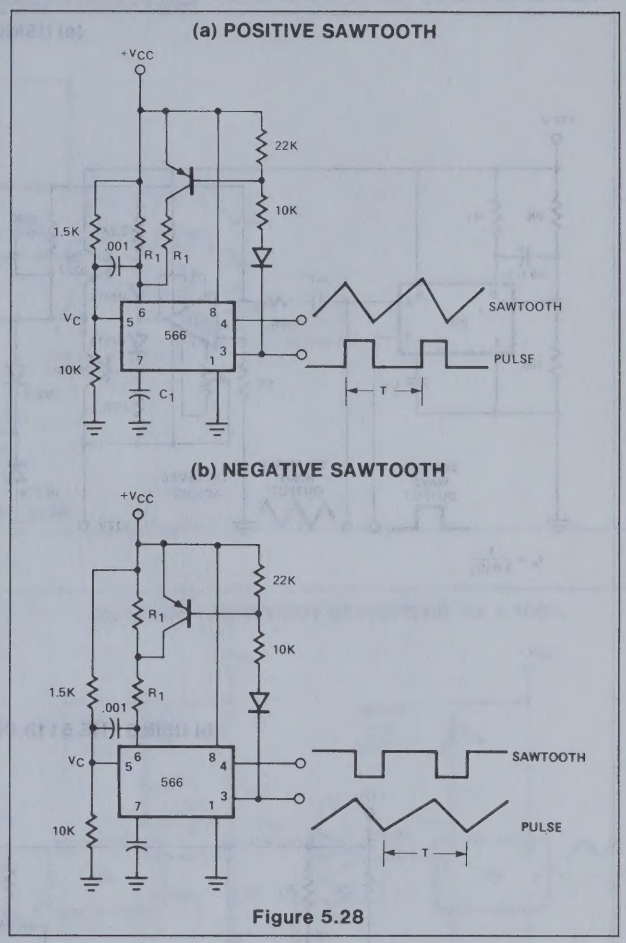


Figure 5.28

quency) applications. Each uses a 566 function generator as a modulation generator and a second 566 as the carrier generator.

Capacitor C_1 selects the modulation frequency adjustment range and C_1' selects the center frequency. Capacitor C_2 is a coupling capacitor which only needs to be large enough to avoid distorting the modulating waveform.

If a frequency sweep in only one direction is required, the 566 ramp generators given in this section may be used to drive the carrier generator.

Radio Frequency FM Generator

Figure 5.32 shows the utilization of a 560 PLL as a FM generator with modulation supplied by a 566 function generator. Capacitor C_1 is chosen to give the desired modulation range, C_2 is large enough for undistorted coupling, and C_3 with its trimmer specifies the center frequency. The VCO output may be taken differentially or single ended.

A 561 or 562 with appropriate pin numbering changes may also be used in this application. If a sweep generator is desired, the 566 may be connected as a ramp generator as was discussed previously.

CRYSTAL-STABILIZED PLL TRACKING FILTER

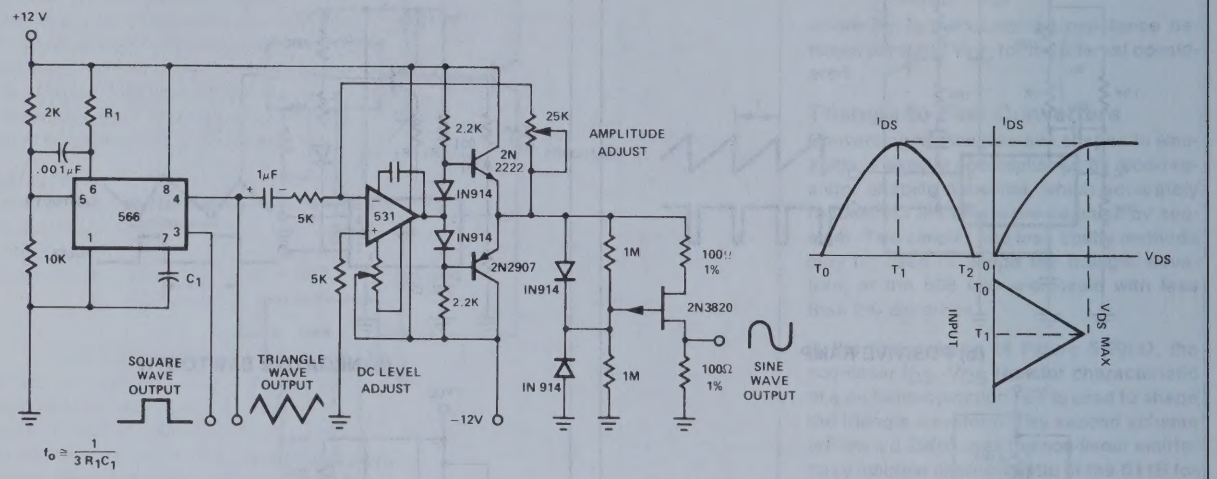
Figure 5.33(a) shows the 560 connected as a tracking filter for signals near 10MHz. The crystal keeps the free-running frequency at the desired value. Figure 5.33(b) shows the lock range as a function of input amplitude. An emitter follower has been added to the normal VCO output to prevent pulling the loop off frequency.

ANALOG LIGHT-COUPLED ISOLATORS

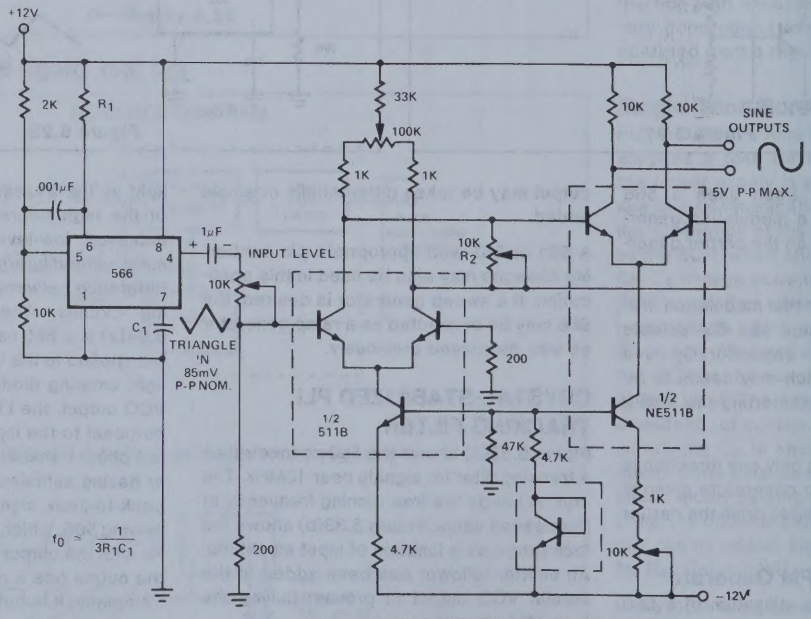
The analog isolators shown in Figure 5.34 are basically FM transmission systems with light as the transmission medium. Because of the high degree of electrical isolation achieved, low-level signals may be transmittd without interference by great potential difference between the sending and receiving circuits. The transmitter in Figure 5.34(a) is a 565 used as a VCO with the input applied to the VCO terminal 7. Since the light emitting diode is driven from the 565 VCO output, the LED flashes at a rate proportional to the input voltage. The receiver is a photo transistor which drives an amplifier having sufficient gain to apply a 200mV peak-to-peak signal to the input of the receiving 565, which then acts as a FM detector with the output appearing at pin 7. Since the output has a ripple at twice the carrier frequency, it is best to keep the carrier frequency as high as possible (typically 100 times the highest modulation frequency). Beause of the excellent temperature stability of the 565, drift is minimal even when dc levels are being transmitted. If operation to dc is not required, the output of the receiver

TRIANGLE-TO-SINE CONVERTERS

(a) USING AN FET



(b) USING THE 511B DIFFERENTIAL AMPLIFIER



R_1, R_2, AND INPUT LEVEL MAY BE ADJUSTED TO GIVE LESS THAN 2% T.H.D. AT OUTPUT USING HEWLETT-PACKARD 333A DIST. ANALYZER.

Figure 5.29

SINGLE-BURST TONE GENERATOR

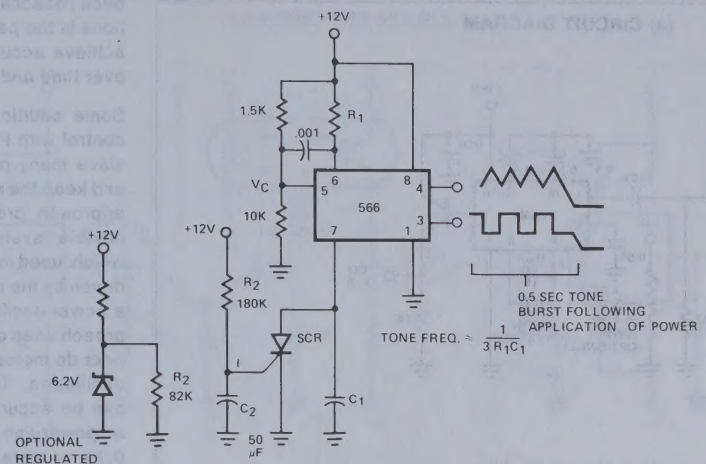


Figure 5.30

FREQUENCY MODULATED GENERATORS

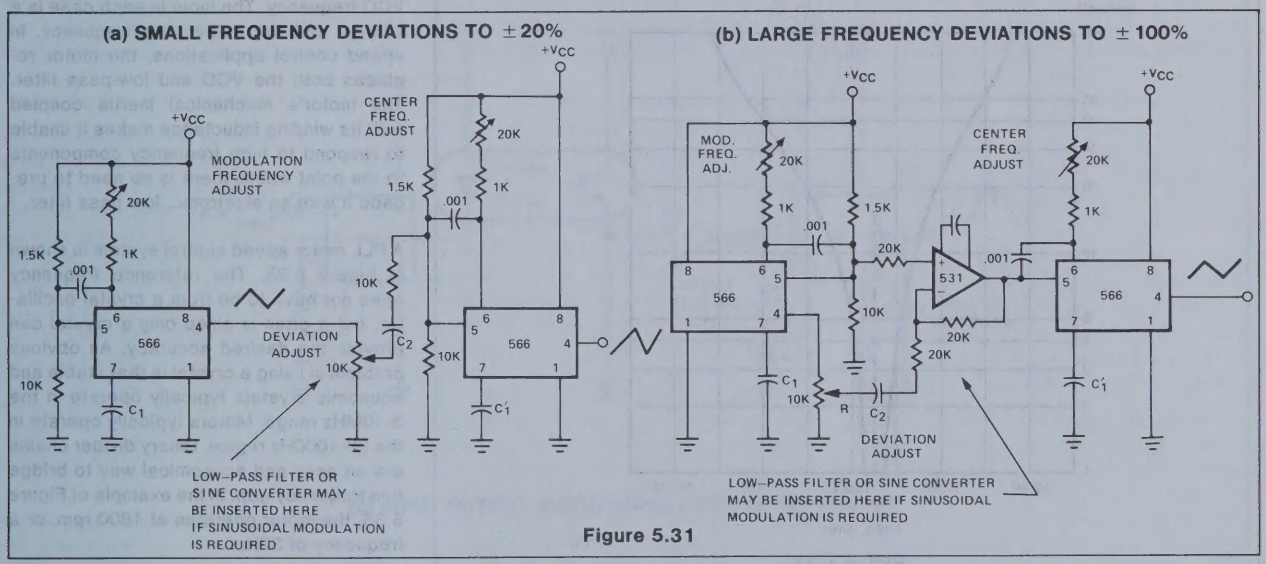


Figure 5.31

RF-FM GENERATOR

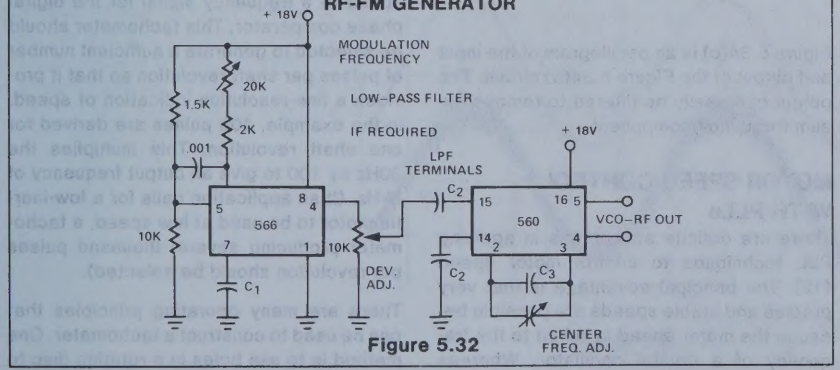
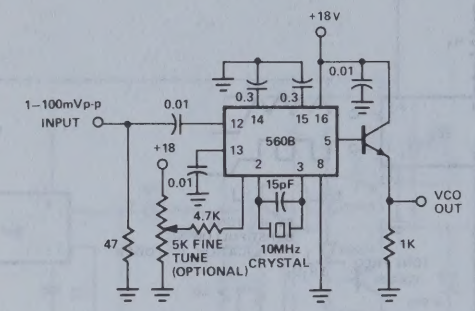


Figure 5.32

CRYSTAL-STABILIZED TRACKING FILTER

(a) CIRCUIT DIAGRAM



(b) LOCK RANGE VERSUS INPUT AMPLITUDE

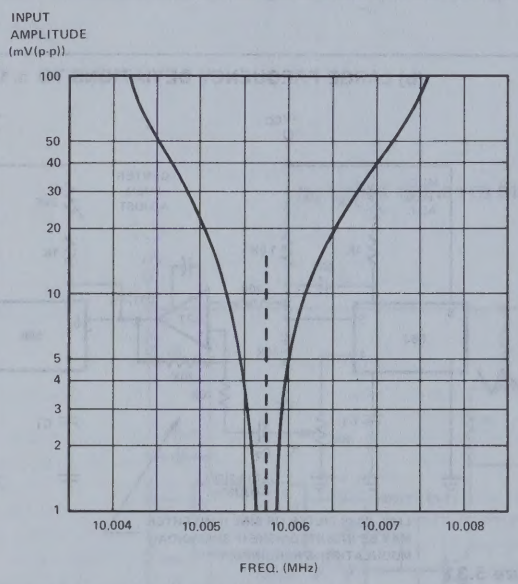


Figure 5.33

can be capacitively coupled to the next stage. Also, a 566 can be used as the transmitter.

Figure 5.34(b) shows that the 567 may be used in the same manner when operation from 5V supplies is required. Here, the output stage of the 567 is used to drive the LED directly. When the free-running frequency of the receiving 567 is the same as that of the transmitting 567, the non-linearity of the two controlled oscillator transfer functions cancel so that highly linear information transfer results.

Figure 5.34(c) is an oscillogram of the input and output of the Figure 5.34(a) circuit. The output can easily be filtered to remove the sum frequency component.

MOTOR SPEED CONTROL WITH PLLs

There are definite advantages in applying PLL techniques to control motor speed (12). The principal advantage is that very precise and stable speeds are possible because the motor speed is linked to the frequency of a crystal oscillator. Whereas speed controls of 1.0% to 0.1% may have been reasonably tight in industrial applications in the past, it is now quite practical to achieve accuracies of 0.002% maintained over time and temperature.

Some additional reasons for using speed control with PLLs are that it is possible to slave many motors to a master oscillator and keep the motors synchronized. The PLL approach produces a smaller and more flexible system than the older method which used many synchronous ac motors driven by the same power-line frequency (or a power oscillator or inverter). The PLL approach uses ordinary inexpensive and compact dc motors and low-power, signal-level oscillators. The PLL oscillator frequency can be accurate to 0.0015% whereas the ac power-line 60Hz frequency may be off by 0.1% or more.

The transfer function of a dc motor is similar to that of the VCO where the motor speed (the rate of shaft rotation) is analogus to VCO frequency. The input in each case is a voltage and the output is a frequency. In speed control applications, the motor replaces both the VCO and low-pass filter. The motor's mechanical inertia coupled with its winding inductance makes it unable to respond to high frequency components to the point where there is no need to precede it with an electronic, low pass filter.

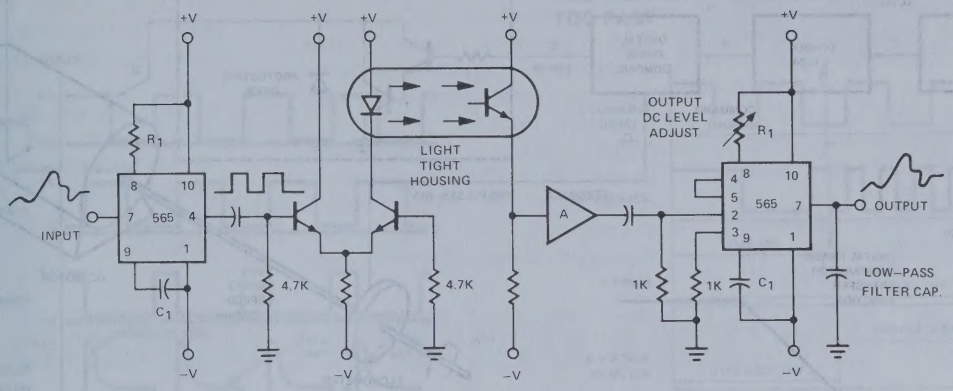
A PLL motor speed control system is shown in Figure 5.35. The reference frequency does not have to be from a crystal oscillator, but it often is since only a crystal can provide the desired accuracy. An obvious problem in using a crystal is that stable and economic crystals typically operate in the 3-10MHz range. Motors typically operate in the 30-1000Hz region. Binary divider chains are an easy and economical way to bridge this frequency gap. In the example of Figure 5.35, the motor operates at 1800 rpm, or a frequency of 30Hz.

A tachometer is used to translate the shaft speed to a frequency signal for the digital phase comparator. This tachometer should be selected to generate a sufficient number of pulses per shaft revolution so that it provides a fine-resolution indication of speed. In the example, 100 pulses are derived for one shaft revolution. This multiplies the 30Hz by 100 to give an output frequency of 3kHz. (If an application calls for a low-inertia motor to be used at low speed, a tachometer producing several thousand pulses per revolution should be selected).

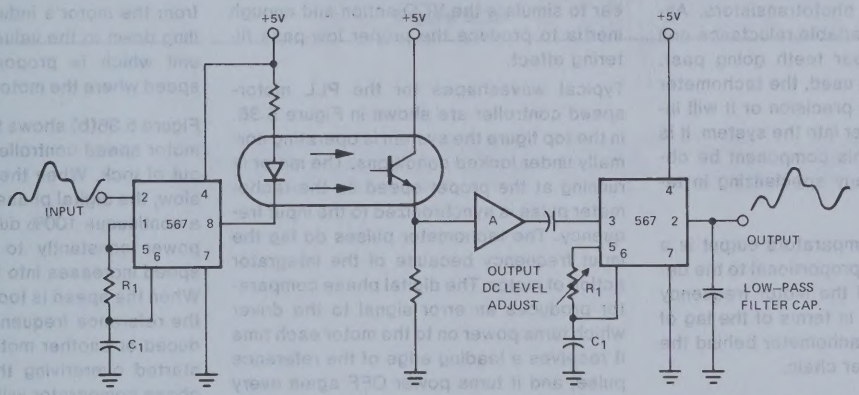
There are many operating principles that can be used to construct a tachometer. One method is to use holes in a rotating disc to

LIGHT-COUPLED ANALOG ISOLATORS

(a) USING THE 565 PLL



(b) CIRCUIT USING THE 567 PLL



(c) INPUT-OUTPUT WAVESHAPES FOR THE 565 CIRCUIT

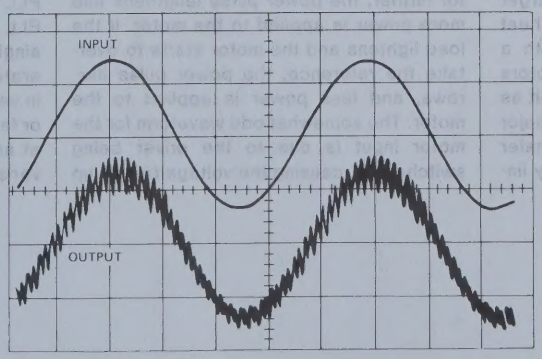


Figure 5.34

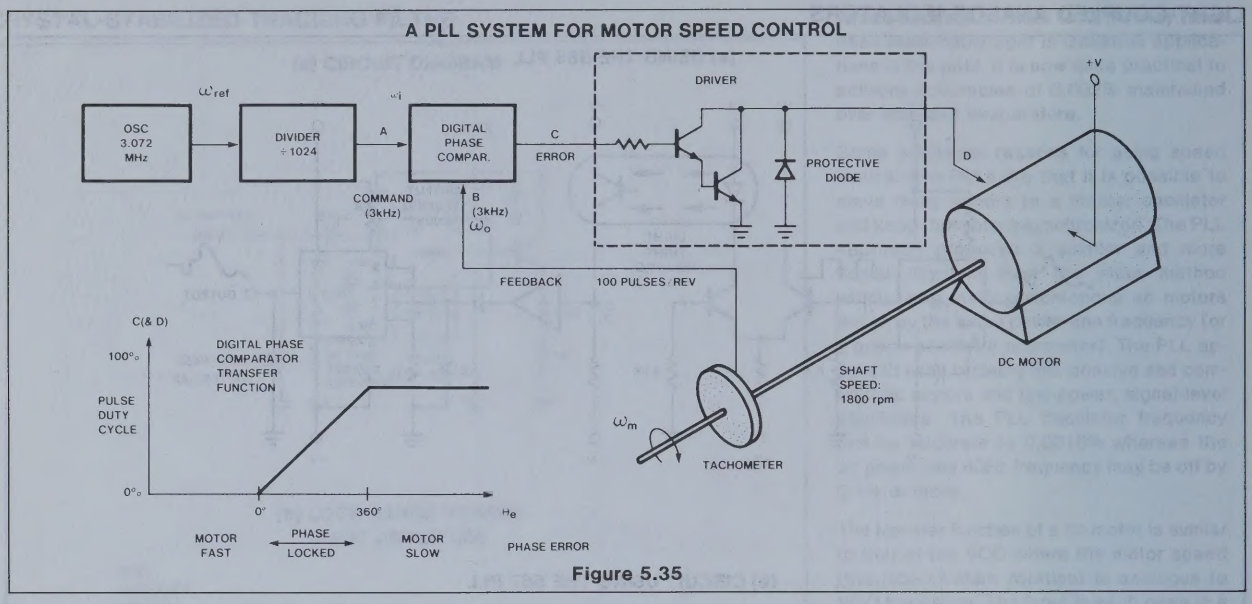


Figure 5.35

gate light pulses to phototransistors. Another way is to use variable reluctance coil pickups to sense gear teeth going past. Whatever principle is used, the tachometer should be made with precision or it will introduce noise and jitter into the system. It is recommended that this component be obtained from a company specializing in tachometers.

The digital phase comparators output is a pulse whose width is proportional to the degree of phase lag of the motor frequency behind the reference in terms of the lag of the pulses from the tachometer behind the pulses from the divider chain.

For small dc motors operating in the one-ampere range, a simple Darlington driver can be used. The driver should be protected against the motors inductive kick upon turn-off by a power diode as shown. For larger dc motors, proportionately larger drivers should be used with adequate heat sinking. There is no reason why, with a proper driver, that very large dc motors could not be used with this same circuit as for small miniature dc motors. The major considerations are that motor's transfer characteristic should be approximately linear to simulate the VCO action and enough inertia to produce the proper low-pass filtering effect.

Typical waveshapes for the PLL motor-speed controller are shown in Figure 5.36. In the top figure the system is operating normally under locked conditions. The motor is running at the proper speed so the tachometer pulse is synchronized to the input frequency. The tachometer pulses do lag the input frequency because of the integrator action of motor. The digital phase comparator produces an error signal to the driver which turns power on to the motor each time it receives a leading edge of the reference pulse, and it turns power OFF again every time it receives a tachometer pulse. This action makes the power-ON duty cycle proportional to the phase lag between the input and tachometer pulses. If the load on the motor increases and tries to retard the motor further, the power pulse lengthens and more power is applied to the motor. If the load lightens and the motor starts to overtake the reference, the power pulse narrows, and less power is applied to the motor. The somewhat odd waveform for the motor input is due to the driver being switched off, causing the voltage to kick up from the motor's inductance and then settling down to the value of the motor's back emf which is proportional to the motor speed where the motor acts as a generator.

Figure 5.36(b) shows the waveforms for the motor speed controller when the system is out of lock. When the motor is running too slow, the digital phase comparator puts out a continuous 100% duty cycle, applying full power constantly to the motor until the speed increases into the linear lock range. When the speed is too fast (as it might be if the reference frequency were suddenly reduced or another motor on the same shaft started overdriving the motor) the digital phase comparator will put a continuous 0% duty cycle which will completely remove power from the motor until it falls back into the lock range.

Like every electronic-system concept, the PLL has infinite variations.For example, the PLL speed control does not have to be a single speed system. It can be made to operate at several fixed speeds by switching in various binary dividers in either the input or feedback loop. It can be made to operate at an infinite number of speeds by using a variable reference oscillator.

WAVEFORMS FOR THE PLL MOTOR SPEED CONTROLLER

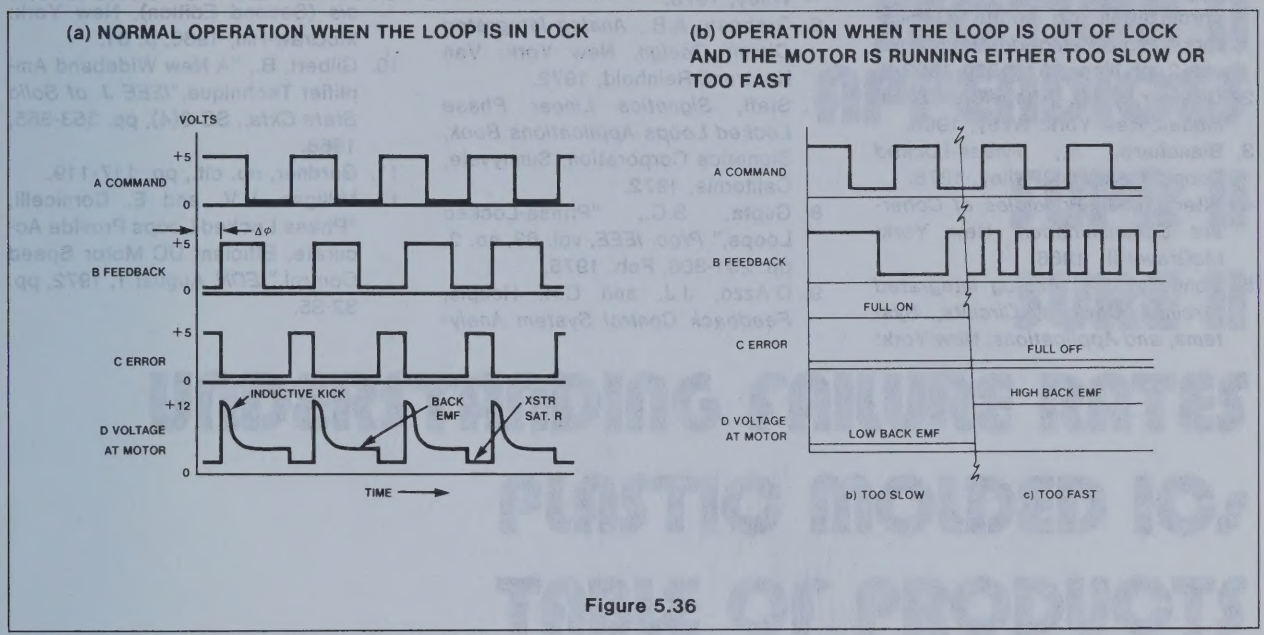


Figure 5.36

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SECTION II
APPENDICES

SUPR II

SURE II

UNDERSTANDING FAILURE RATES

PLASTIC MOLDED ICs

TABLE OF PRODUCTS AND ORDERING INFORMATION

APPENDICES

APPENDICES

INCHES			DECIMAL EQUIVALENT	MILLIMETER EQUIVALENT
1/64			.0156	0.397
	1/32		.0313	0.794
3/64			.0469	1.191
		1/16	.0625	1.588
5/64			.0781	1.985
	3/32		.0938	2.381
7/64			.1094	2.778
		1/8	.1250	3.175
9/64			.1406	3.572
	5/32		.1563	3.969
11/64			.1719	4.366
		3/16	.1875	4.762
13/64			.2031	5.159
	7/32		.2188	5.556
15/64			.2344	5.953
		1/4	.2500	6.350
17/64			.2656	6.747
	9/32		.2813	7.144
19/64			.2969	7.541
		5/16	.3125	7.937
21/64			.3281	8.334
	11/32		.3438	8.731
23/64			.3594	9.128
		3/8	.3750	9.525
25/64			.3906	9.922
	13/32		.4063	10.319
27/64			.4219	10.716
		7/16	.4375	11.112
29/64			.4531	11.509
	15/32		.4688	11.906
31/64			.4844	12.303
		1/2	.5000	12.700
33/64			.5156	13.097
	17/32		.5313	13.494
35/64			.5469	13.891
		9/16	.5625	14.287
37/64			.5781	14.684
	19/32		.5938	15.081
39/64			.6094	15.478
		5/8	.6250	15.875
41/64			.6406	16.272
	21/32		.6563	16.669
43/64			.6719	17.067
		11/16	.6875	17.463
45/64			.7031	17.860
	23/32		.7188	18.238
47/64			.7344	18.635
		3/4	.7500	19.049
49/64			.7656	19.446
	25/32		.7813	19.842
51/64			.7969	20.239
		13/16	.8125	20.636
53/64			.8281	21.033
	27/32		.8438	21.430
55/64			.8594	21.827
		7/8	.8750	22.224
57/64			.8906	22.621
	29/32		.9063	23.018
59/64			.9219	23.415
		15/16	.9375	23.812
61/64			.9531	24.209
	31/32		.9688	24.606
63/64			.9844	25.004
		1.0	1.0000	25.400

MATHEMATICAL CONSTANTS

$\pi = 3.14$

$2\pi = 6.28$

$(2\pi)^2 = 39.5$

$4\pi = 12.6$

$\pi^2 = 9.87$

$\frac{\pi}{2} = 1.57$

$\frac{1}{\pi} = 0.318$

$\frac{1}{2\pi} = 0.159$

$\frac{1}{\pi^2} = 0.101$

$\frac{1}{\sqrt{\pi}} = 0.564$

$\sqrt{\pi} = 1.77$

$\sqrt{\frac{\pi}{2}} = 1.25$

$\sqrt{2} = 1.41$

$\sqrt{3} = 1.73$

$\frac{1}{\sqrt{2}} = 0.707$

$\frac{1}{\sqrt{3}} = 0.577$

$\log \pi = 0.497$

$\log \frac{\pi}{2} = 0.196$

$\log \pi^2 = 0.994$

$\log \sqrt{\pi} = 0.248$

TEMPERATURE CONVERSION TABLE

°C	°F	°C	°F	°C	°F	°C	°F
−100	−148	+ 60	+140	+220	+428	+380	+716
− 95	−139	+ 65	+149	+225	+437	+385	+725
− 90	−130	+ 70	+158	+230	+446	+390	+734
− 85	−121	+ 75	+167	+235	+455	+395	+743
− 80	−112	+ 80	+176	+240	+464	+400	+752
− 75	−103	+ 85	+185	+245	+473	+405	+761
− 70	− 94	+ 90	+194	+250	+482	+410	+770
− 65	− 85	+ 95	+203	+255	+491	+415	+779
− 60	− 76	+100	+212	+260	+500	+420	+788
− 55	− 67	+105	+221	+265	+509	+425	+797
− 50	− 58	+110	+230	+270	+518	+430	+806
− 45	− 49	+115	+239	+275	+527	+435	+815
− 40	− 40	+120	+248	+280	+536	+440	+824
− 35	− 31	+125	+257	+285	+545	+445	+833
− 30	− 22	+130	+266	+290	+554	+450	+842
− 25	− 13	+135	+275	+295	+563	+455	+851
− 20	− 4	+140	+284	+300	+572	+460	+860
− 15	+ 5	+145	+293	+305	+581	+465	+869
− 10	+ 14	+150	+302	+310	+590	+470	+878
− 5	+ 23	+155	+311	+315	+599	+475	+887
0	+ 32	+160	+320	+320	+608	+480	+896
+ 5	+ 41	+165	+329	+325	+617	+485	+905
+ 10	+ 50	+170	+338	+330	+626	+490	+914
+ 15	+ 59	+175	+347	+335	+635	+495	+923
+ 20	+ 68	+180	+356	+340	+644	+500	+932
+ 25	+ 77	+185	+365	+345	+653	+505	+941
+ 30	+ 86	+190	+374	+350	+662	+510	+950
+ 35	+ 95	+195	+383	+355	+671	+515	+959
+ 40	+104	+200	+392	+360	+680	+520	+968
+ 45	+113	+205	+401	+365	+689	+525	+977
+ 50	+122	+210	+410	+370	+698	+530	+986
+ 55	+131	+215	+419	+375	+707	+535	+995

REACTANCE CHART

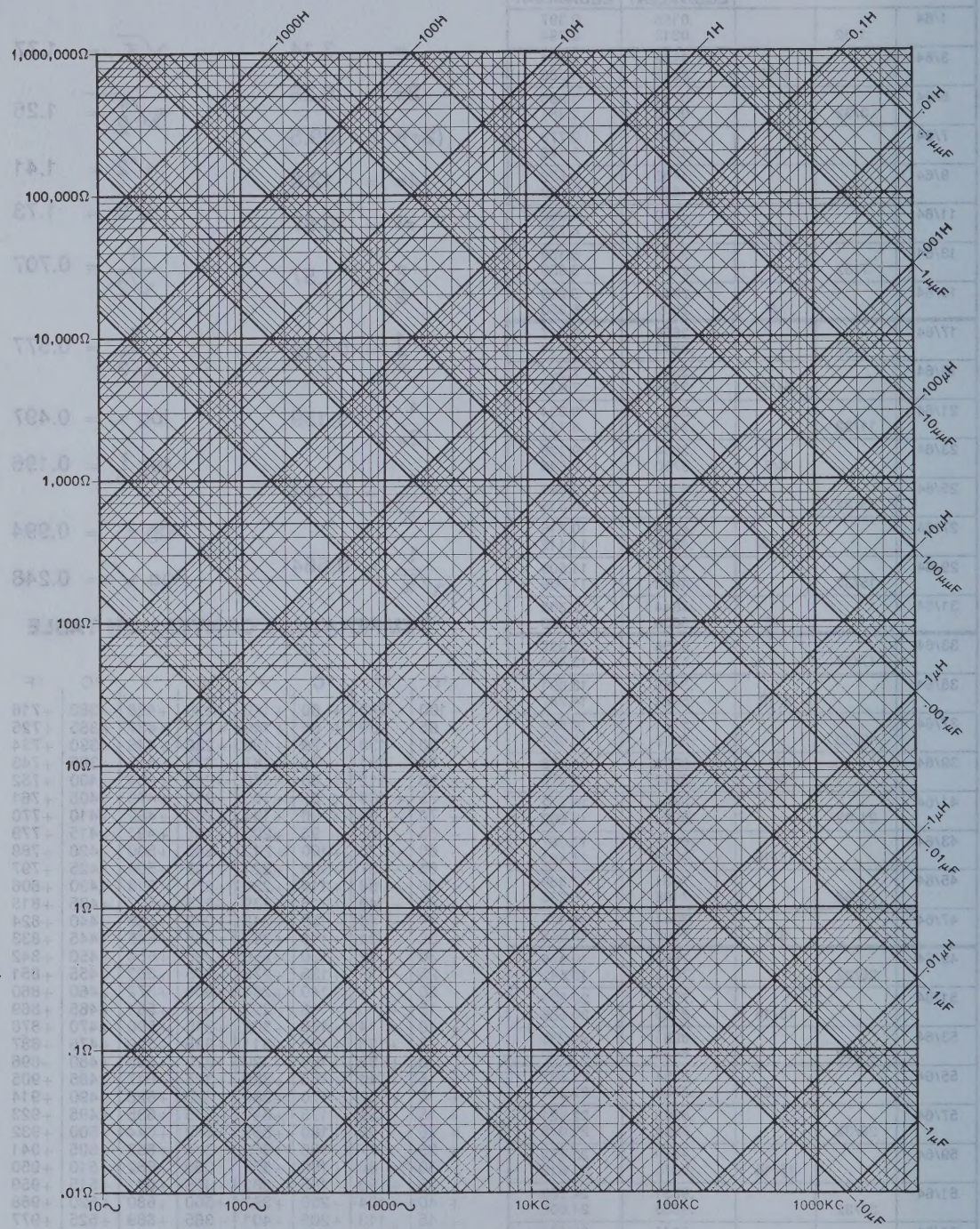


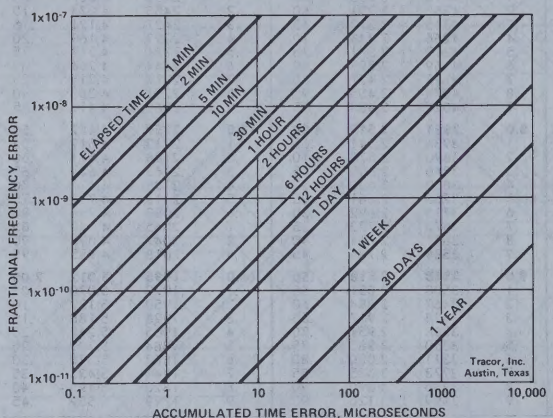
TABLE OF DECIBELS

DECIBEL (Voltage)	LOSS	GAIN	DECIBEL (Power)
.0	1.0000	1.000	.0
.1	.9886	1.012	.05
.2	.9772	1.023	.10
.3	.9661	1.035	.15
.4	.9550	1.047	.20
.5	.9441	1.059	.25
.6	.9333	1.072	.30
.7	.9226	1.084	.35
.8	.9120	1.096	.40
.9	.9016	1.109	.45
1.0	**.8913**	**1.122**	**.50**
.1	.8810	1.135	.55
.2	.8710	1.148	.60
.3	.8610	1.161	.65
.4	.8511	1.175	.70
.5	.8414	1.189	.75
.6	.8318	1.202	.80
.7	.8222	1.216	.85
.8	.8128	1.230	.90
.9	.8035	1.245	.95
2.0	**.7943**	**1.259**	**1.00**
.1	.7852	1.274	.05
.2	.7762	1.288	.10
.3	.7674	1.303	.15
.4	.7586	1.318	.20
.5	.7499	1.334	.25
.6	.7413	1.349	.30
.7	.7328	1.365	.35
.8	.7244	1.380	.40
.9	.7161	1.396	.45
3.0	**.7079**	**1.413**	**.50**
.1	.6998	1.429	.55
.2	.6918	1.445	.60
.3	.6839	1.462	.65
.4	.6761	1.479	.70
.5	.6683	1.496	.75
.6	.6607	1.514	.80
.7	.6531	1.531	.85
.8	.6457	1.549	.90
.9	.6383	1.567	.95
4.0	**.6310**	**1.585**	**2.00**
.1	.6237	1.603	.05
.2	.6166	1.622	.10
.3	.6095	1.641	.15
.4	.6026	1.660	.20
.5	.5957	1.679	.25
.6	.5888	1.698	.30
.7	.5821	1.718	.35
.8	.5754	1.738	.40
.9	.5689	1.758	.45
5.0	**.5623**	**1.778**	**.50**
.1	.5559	1.799	.55
.2	.5495	1.820	.60
.3	.5433	1.841	.65
.4	.5370	1.862	.70
.5	.5309	1.884	.75
.6	.5248	1.905	.80
.7	.5188	1.928	.85
.8	.5129	1.950	.90
.9	.5070	1.972	.95
6.0	**.5012**	**1.995**	**3.00**
.1	.4955	2.018	.05
.2	.4898	2.042	.10
.3	.4842	2.065	.15
.4	.4786	2.089	.20
.5	.4732	2.113	.25
.6	.4677	2.138	.30
.7	.4624	2.163	.35
.8	.4571	2.188	.40
.9	.4519	2.213	.45
7.0	**.4467**	**2.239**	**.50**
.1	.4416	2.265	.55
.2	.4365	2.291	.60
.3	.4315	2.317	.65
.4	.4266	2.344	.70
.5	.4217	2.371	.75
.6	.4169	2.399	.80
.7	.4121	2.427	.85
.8	.4074	2.455	.90
.9	.4027	2.483	.95
8.0	**.3981**	**2.512**	**4.00**
.1	.3936	2.541	.05
.2	.3890	2.570	.10
.3	.3846	2.600	.15
.4	.3802	2.630	.20
.5	.3758	2.661	.25
.6	.3715	2.692	.30
.7	.3673	2.723	.35
.8	.3631	2.754	.40
.9	.3589	2.786	.45
9.0	**.3548**	**2.818**	**.50**
.1	.3508	2.851	.55
.2	.3467	2.884	.60
.3	.3428	2.917	.65
.4	.3388	2.951	.70
.5	.3350	2.985	.75
.6	.3311	3.020	.80
.7	.3273	3.055	.85
.8	.3236	3.090	.90
.9	.3199	3.126	.95
10.0	**.3162**	**3.162**	**5.00**
.1	.3126	3.199	.05
.2	.3090	3.236	.10
.3	.3055	3.273	.15
.4	.3020	3.311	.20
.5	.2985	3.350	.25
.6	.2951	3.388	.30
.7	.2917	3.428	.35
.8	.2884	3.467	.40
.9	.2851	3.508	.45
11.0	**.2818**	**3.548**	**.50**
.1	.2786	3.589	.55
.2	.2754	3.631	.60
.3	.2723	3.673	.65
.4	.2692	3.715	.70
.5	.2661	3.758	.75
.6	.2630	3.802	.80
.7	.2600	3.846	.85
.8	.2570	3.890	.90
.9	.2541	3.936	.95
12.0	**.2512**	**3.981**	**6.00**
.1	.2483	4.027	.05
.2	.2455	4.074	.10
.3	.2427	4.121	.15
.4	.2399	4.169	.20
.5	.2371	4.217	.25
.6	.2344	4.266	.30
.7	.2317	4.315	.35
.8	.2291	4.365	.40
.9	.2265	4.416	.45
13.0	**.2239**	**4.467**	**.50**
.1	.2213	4.519	.55
.2	.2188	4.571	.60
.3	.2163	4.624	.65
.4	.2138	4.677	.70
.5	.2113	4.732	.75
.6	.2089	4.786	.80
.7	.2065	4.842	.85
.8	.2042	4.898	.90
.9	.2018	4.955	.95
14.0	**.1995**	**5.012**	**7.00**
.1	.1972	5.070	.05
.2	.1950	5.129	.10
.3	.1928	5.188	.15
.4	.1905	5.248	.20
.5	.1884	5.309	.25
.6	.1862	5.370	.30
.7	.1841	5.433	.35
.8	.1820	5.495	.40
.9	.1799	5.559	.45
15.0	**.1778**	**5.623**	**.50**
.1	.1758	5.689	.55
.2	.1738	5.754	.60
.3	.1718	5.821	.65
.4	.1698	5.888	.70
.5	.1679	5.957	.75
.6	.1660	6.026	.80
.7	.1641	6.095	.85
.8	.1622	6.166	.90
.9	.1603	6.237	.95
16.0	**.1585**	**6.310**	**8.00**
.1	.1567	6.383	.05
.2	.1549	6.457	.10
.3	.1531	6.531	.15
.4	.1514	6.607	.20
.5	.1496	6.683	.25
.6	.1479	6.761	.30
.7	.1462	6.839	.35
.8	.1445	6.918	.40
.9	.1429	6.998	.45
17.0	**.1413**	**7.079**	**.50**
.1	.1396	7.161	.55
.2	.1380	7.244	.60
.3	.1365	7.328	.65
.4	.1349	7.413	.70
.5	.1334	7.499	.75
.6	.1318	7.586	.80
.7	.1303	7.674	.85
.8	.1288	7.762	.90
.9	.1274	7.852	.95
18.0	**.1259**	**7.943**	**9.00**
.1	.1245	8.035	.05
.2	.1230	8.128	.10
.3	.1216	8.222	.15
.4	.1202	8.318	.20
.5	.1189	8.414	.25
.6	.1175	8.511	.30
.7	.1161	8.610	.35
.8	.1148	8.710	.40
.9	.1135	8.811	.45
19.0	**.1122**	**8.913**	**.50**
.1	.1109	9.016	.55
.2	.1096	9.120	.60
.3	.1084	9.226	.65
.4	.1072	9.333	.70
.5	.1059	9.441	.75
.6	.1047	9.550	.80
.7	.1035	9.661	.85
.8	.1023	9.772	.90
.9	.1012	9.886	.95

DECIBEL (Voltage)	LOSS	GAIN	DECIBEL (Power)
20.0	**.1000**	**10.00**	**10.00**
	Use the same numbers as 0-20 dB, but shift point one step to the left. Thus since 10dB = .3162 30dB = .03162	Use the same numbers as 0-20 dB, but shift point one step to the right. Thus since 10dB = 3.162 30dB = 31.62	This column repeats every 10dB instead of every 20dB
40.0	**.01**	**100**	**20.00**
	Use the same numbers as 0-20 dB, but shift point two steps to the left. Thus since 10dB = .3162 50dB = .003162	Use the same numbers as 0-20 dB, but shift point two steps to the right. Thus since 10dB = 3.162 50db = 316.2	This column repeats every 10dB instead of every 20dB

DECIBEL (Voltage)	LOSS	GAIN	DECIBEL (Power)
60.0	**.001**	**1,000**	**30.00**
	Use the same numbers as 0-20dB, but shift point three steps to the left. Thus since 10dB = .3162 70dB = .0003162	Use the same numbers as 0-20 dB, but shift point three steps to the right. Thus since 10dB = 3.162 70dB = 3162.	This column repeats every 10dB instead of every 20dB
80.0	**.0001**	**10,000**	**40.00**
	Use the same numbers as 0-20 dB, but shift point four steps to the left. Thus since 10dB = .3162 90dB = .00003162	Use the same numbers as 0-20dB, but shift point four steps to the right. Thus since 10dB = 3.162 90dB = 31620.	This column repeats every 10dB instead of every 20dB.
100.0	**.00001**	**100,000**	**50.00**

FREQUENCY CONVERSION FACTORS



Frequency Conversion Factors

1 min=60 sec=6×10^7 μsec
1 hr.=3600 sec=3.6×10^9 μsec
1 day=8.64×10^4 sec=8.64×10^{10} μsec
1 microsecond/min=1.667×10^{-8}
1 microsecond/hr.=2.78×10^{-10}
1 microsecond/day=1.16×10^{-11}
Fractional frequency error, $\frac{\Delta f}{f}$ =

$$\frac{\text{difference in microseconds}}{\text{elapsed time in seconds}} \times 10^{-6}$$

SUPR II

SUPR II

QUALITY AND RELIABILITY

Quality and reliability are two important measures of a product's merit. Quality is a measure of an integrated circuit's conformance to agreed-upon criteria at a given time, while Reliability is a measure of the circuit's ability to continue to conform over a period of time. The Signetics SUPR II Program has been designed to upgrade the basic product quality through the use of more rigorous screening criteria at the critical process steps. These additional screens constitute the Level A portion of the Program. A burn-in option is available for those users requiring enhanced reliability performance, and this option is designated as Level B.

Quality

The quality of an integrated circuit is appraised by the user based on the ability of the circuit to meet the specified electrical criteria and external visual appearance. The SUPR II Program focuses on supplying to the user a product that has a high probability of meeting the user's needs through the sampling plans defined in MIL-STD-105D and the quality levels (AQL's) stated in Table II. Many of the inspection methods at critical process steps are now based on MIL-STD-883 criteria in order to build, rather than test, quality into the product.

Reliability

System performance over a period of time is the user's measure of an integrated circuit's reliability. The SUPR II Program improves system reliability by building quality into the product via additional manufacturing inspections and the offering of a burn-in screen. In addition to the SUPR II Program, Signetics performs periodic reliability testing via the SURE II/883A Program to assure continuing uniformity and long-term reliability of all product lines. This data base is available upon request as is the ten-year reliability summary, Signetics Product Reliability Report, R-363.

How Do Integrated Circuit Failures Occur?

Results from the Signetics Failure Analysis Lab over a three-year period on product returned from board checkout, system checkout, field usage and accelerated life testing are graphically presented in Figure 11-1. Under typical system operating conditions, random manufacturing defects, as outlined in Table 11-1, are the primary cause of true device failure. Also shown in Table 1 are the process controls that have been added via the SUPR II Program to minimize these defects prior to shipment to the customer. The device failure models are categorized as:

Half of the devices analyzed were found to be electrically good. They are attributed to being "false pulls" that occur during normal troubleshooting at the board and system levels.

Devices damaged by electrical over-stress account for 25% of the failures. Typical causes for electrical over-stress are incorrect board insertion, board shorts between device pins, power supply transients, and poor handling techniques.

The remaining 25% were verified to be true failures which occurred as a result of an in-process manufacturing defect or test escape.

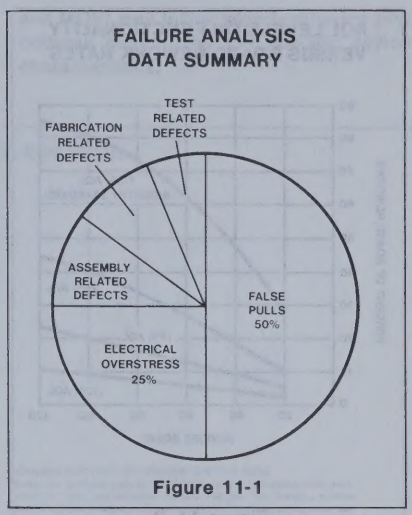


Figure 11-1

SIGNETICS SUPR II LEVEL A

Improved Quality Benefits

From the user's point of view, improved integrated circuit quality from the supplier means a lower cost of ownership. This cost saving can be effected through the reduction or elimination of involved incoming inspection testing, reduced PC board rework, simplified system checkout, reduced in-line inventories, and less complicated part tracking by Purchasing Management.

The SUPR II Program is Corporate in scope and covers Logic (Standard TTL, Schottky TTL, Low Power Schottky TTL, ECL, 8T Interface), Analog (Industrial, Consumer, Interface), Bipolar Memories (RAM's, ROM's, PROM's), and MOS Memories (RAM's, ROM's, Shift Registers), All package options are also available.

The SUPR II flow is detailed in Figure 11-5, including the test methods and Quality acceptance levels (Table 11-2 provides the electrical/mechanical finished product AQL's). Highlights of the flow are visual inspections, thermal shock preconditioning, hermeticity, and burn-in, all based on MIL-STD-883 criteria.

A good example of the savings which can be achieved by purchasing tighter inspection levels is given in Figure 11-2. Here we are comparing the various levels of inspection (AQL's) available for device functionality and its impact on the number of PC boards which must be reworked during system manufacturing. Using the standard commercial AQL in functionality of 1.0%, at 120 integrated circuit packages per board, typically more than 90% of boards will require rework. At 0.15% AQL, rework is reduced to 25%, and at 0.1%, typically only 12% rework is required.

SIGNETICS SUPR II LEVEL B

Infant Mortality Failures

Failure rates are most severe during the first few months of operating life. This is known as the "infant mortality" phase. A system

FAILURE MECHANISMS	CAUSES	SUPR II CONTROL
Die Fabrication Related	Metalization Oxide Defects Mechanical Scratches Contamination	SEM Monitor Visual Stabilization Bake Burn-In
Assembly Related	Bonding, Wire, Package and Seal Defects	Preseal Visual Thermal Shock Stabilization Bake Hermeticity Hot-Rail Testing
Test Related	Test Escapes	Tightened AQL Guarantees High Temperature Testing

Table 11-1

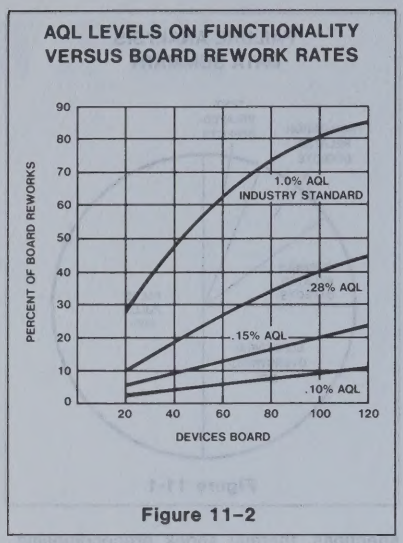


Figure 11–2

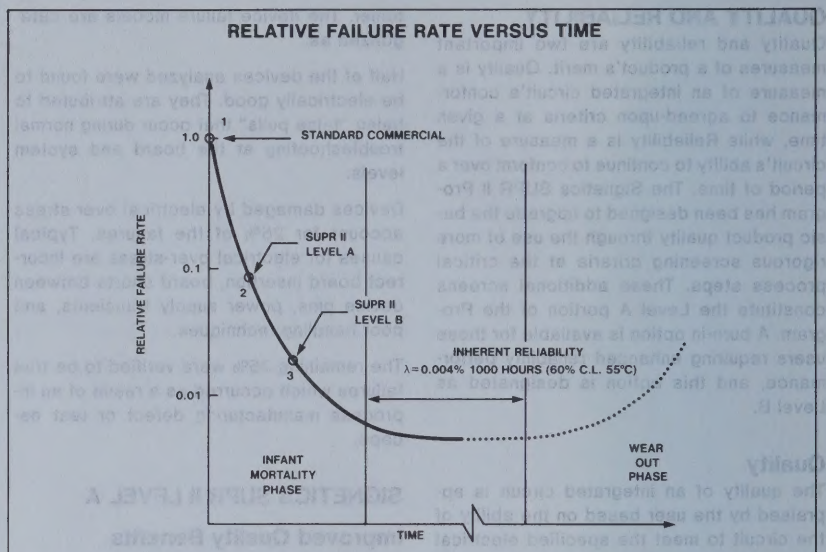


Figure 11-3

manufacturer has various options to solve problems arising from infant failures. He can ship his system to the end customer and repair field failures as they occur. He can operate the system in-house for this period and repair failures. Or he can purchase devices which have already been preconditioned to eliminate the early failures. Each customer must choose the most cost-effective method for his particular business. A considerable number of the reliabilty defects which cause early failures are eliminated by the manufacturing control and preconditioning steps of SUPR II Level A processing. More persistent defects can be removed by the use of "burn-in" techniques. The "burn-in" processing of SUPR II Level B effectively allows the system manufacturer to ship his equipment at Point 3 on the failure rate curve in Figure 11-3.

Burn-In Conditions

MIL-STD-883A, Method 1015 describes a number of different conditions for integrated

		ANALOG		BIPOLAR MEMORY		LOGIC		MOS/LSI	
		Plastic	Ceramic Metal Can	Plastic	Ceramic Metal Can	Plastic	Ceramic Metal Can	Plastic	Ceramic Metal Can
HOT OPENS	100°C	0.15%	-	0.15%	-	0.15%	-	0.15%	-
FUNCTIONALITY (NOTE 1)	25°C	0.15	0.15	0.25	0.25	0.10	0.10	0.25	0.25
	HIGH TEMPERATURE	0.25	0.25	-	-	0.10	0.10	0.25	0.25
D.C. PARAMETRIC	25°C	0.25	0.25	0.65	0.65	0.65	0.65	0.65	0.65
	OVER TEMPERATURE	0.65	0.65	0.65	0.65	0.65	0.65	0.65	0.65
A.C. PARAMETRIC	25°C	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
MECHANICAL	MAJOR	0.25	0.25	0.25	0.25	0.25	0.25	0.25	0.25
SEAL TEST (CERAMIC METAL CAN ONLY)	MINOR	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
	FINE LEAK 1×10^{-7} cc/s	N/A	1.0	N/A	1.0	N/A	1.0	N/A	1.0
	GROSS LEAK 1×10^{-5} cc/s	N/A	0.65	N/A	0.65	N/A	0.65	N/A	0.65

NOTE

1. To insure AQL levels tighter than 0.65% on D.C. parameters usually requires continual correlation of test equipment between customer and vendor to avoid test interpretation problems. If the objective is to reduce system rework costs, functional operation of a device (does it switch or toggle in the system) is often more critical than the absolute value of a parameter. For this reason SUPR II focuses attention on tightened AQL's on functionality.

For analog devices, D. C. parameters, such as input current and offset voltages, tend to be more critical to system operation than for logic devices. A 0.25% AQL is therefore offered on analog D.C. parameters, with the realization that careful attention must be paid to establishing correlation at the customer's incoming inspection.

Table 11-2 SUPRA II AQL GUARANTEE

circuit burn-in. For SUPR II Level B, Signetics has selected Condition F. This is the accelerated burn-in method derived from MIL-STD-883A, utilizing a high temperature reversed bias condition. This bias scheme is preferred for infant mortality screening, while operating conditions are generally utilized for internal reliability programs oriented toward generating MTBF data for the system designer.

Integrated Burn-In Flow

Signetics SUPR II Level B burn-in is performed to provide reliability assurance equivalent to a 168-hour/125°C screen. This process has been integrated into the standard manufacturing flow to provide the customer with the most cost effective screen and significantly reduced delivery times.

BURN-IN FLOW

ASSEMBLY

The flow from SEM control through package seal is common to Levels A and B.

⇩

TEST

The pre-burn-in electrical screen is designed to remove assembly rejects and increase equipment efficiency.

⇩

BURN-IN

The 24-hour/155°C accelerated burn-in is well controlled to provide maximum screening effectiveness without damaging good devices.

⇩

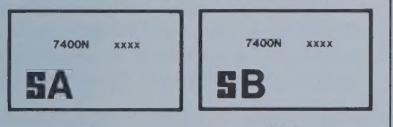
TEST

The post-burn-in electrical is a 100% production DC/function electrical test.

Figure 11-4

Marking Format

Product processed to the SUPR II manufacturing flow can be identified by an SA for Level A, and an SB for the Level B burn-in option.



SUPR II LEVEL A

SUPR II LEVEL B

NOTE
Marking for Level A in process of being implemented.

Figure 11-5 shows the generalized process flow for all Signetics integrated circuits purchased to the SUPR II program. Each product group (Analog, Bipolar Memory, Logic, and MOS) may follow slightly different procedures dictated by the specific device characteristics.

SUPR II PROCESS FLOW

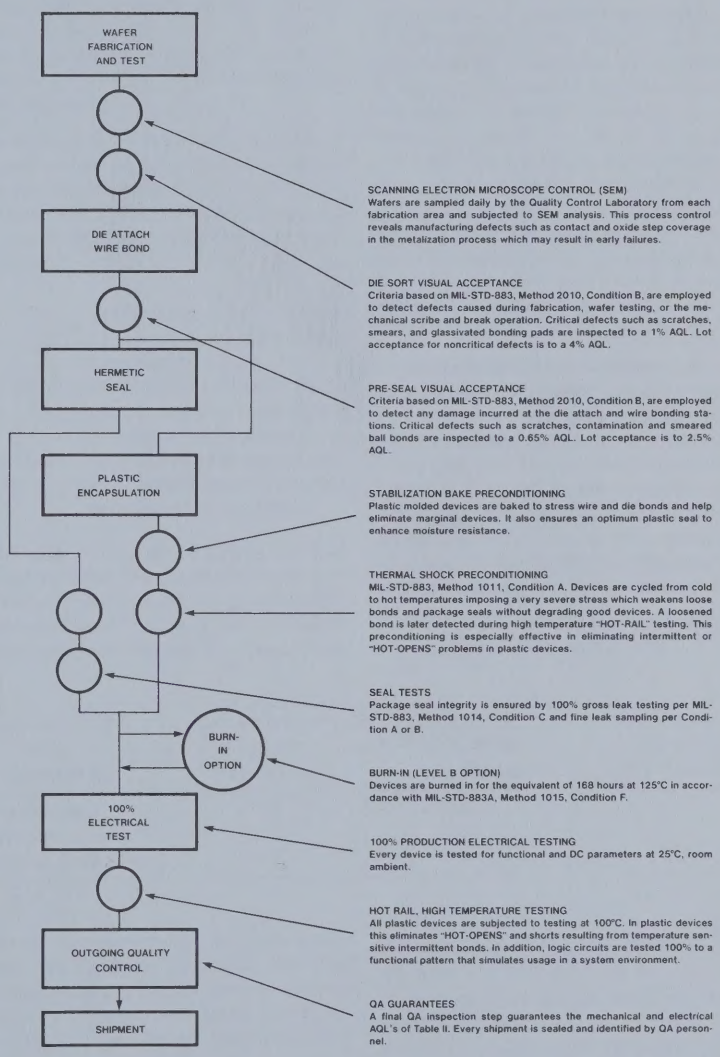
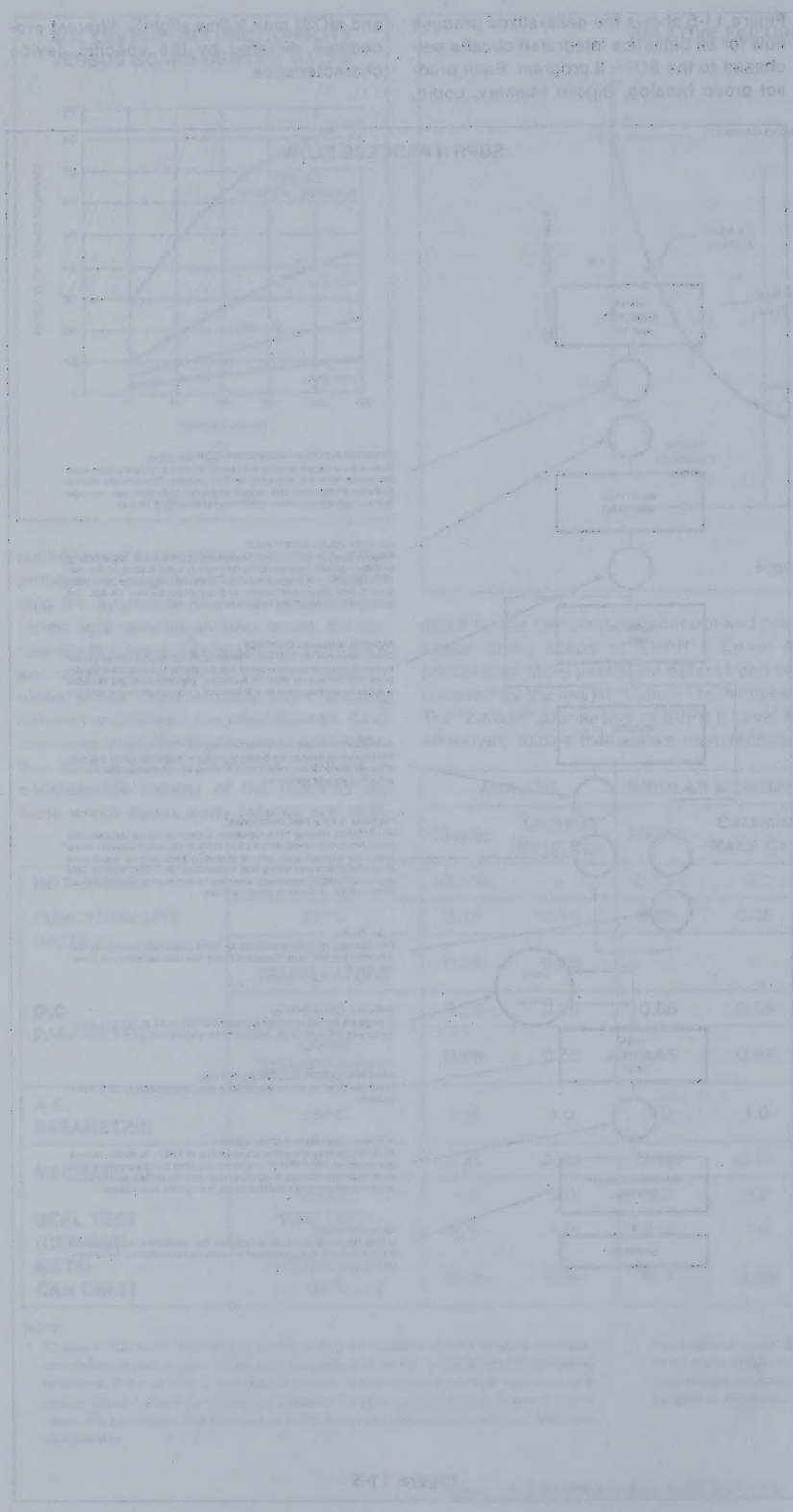

WAFER FABRICATION AND TEST
DIE ATTACH WIRE BOND
HERMETIC SEAL
PLASTIC ENCAPSULATION
BURN-IN OPTION
100% ELECTRICAL TEST
OUTGOING QUALITY CONTROL
SHIPMENT
SCANNING ELECTRON MICROSCOPE CONTROL (SEM)
Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.
DIE SORT VISUAL ACCEPTANCE
Criteria based on MIL-STD-883, Method 2010, Condition B, are employed to detect defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Critical defects such as scratches, smears, and glassivated bonding pads are inspected to a 1% AQL. Lot acceptance for noncritical defects is to a 4% AQL.
PRE-SEAL VISUAL ACCEPTANCE
Criteria based on MIL-STD-883, Method 2010, Condition B, are employed to detect any damage incurred at the die attach and wire bonding stations. Critical defects such as scratches, contamination and smeared ball bonds are inspected to a 0.65% AQL. Lot acceptance is to 2.5% AQL.
STABILIZATION BAKE PRECONDITIONING
Plastic molded devices are baked to stress wire and die bonds and help eliminate marginal devices. It also ensures an optimum plastic seal to enhance moisture resistance.
THERMAL SHOCK PRECONDITIONING
MIL-STD-883, Method 1011, Condition A. Devices are cycled from cold to hot temperatures imposing a very severe stress which weakens loose bonds and package seals without degrading good devices. A loosened bond is later detected during high temperature "HOT-RAIL" testing. This preconditioning is especially effective in eliminating intermittent or "HOT-OPENS" problems in plastic devices.
SEAL TESTS
Package seal integrity is ensured by 100% gross leak testing per MIL-STD-883, Method 1014, Condition C and fine leak sampling per Condition A or B.
BURN-IN (LEVEL B OPTION)
Devices are burned in for the equivalent of 168 hours at 125°C in accordance with MIL-STD-883A, Method 1015, Condition F.
100% PRODUCTION ELECTRICAL TESTING
Every device is tested for functional and DC parameters at 25°C, room ambient.
HOT RAIL, HIGH TEMPERATURE TESTING
All plastic devices are subjected to testing at 100°C. In plastic devices this eliminates "HOT-OPENS" and shorts resulting from temperature sensitive intermittent bonds. In addition, logic circuits are tested 100% to a functional pattern that simulates usage in a system environment.
QA GUARANTEES
A final QA inspection step guarantees the mechanical and electrical AQL's of Table II. Every shipment is sealed and identified by QA personnel.

Figure 11-5



SURE II

SIGNETICS SURE II/883B RELIABILITY PROGRAM

Definition

Signetics is recognized as a manufacturer of reliable integrated circuits. Signetics realized long ago the need for a comprehensive reliability program to provide timely data representative of the entire Signetics product line. Thus the establishment of a Systematic and Uniform Reliability Evaluation program, known as SURE, which provides this data in a manner unique to the industry. Furthermore, this program is provided at no cost to customers.

The SURE Program is a Signetics in-house Qualification Test Program which has been in existence since 1963. The SURE Program is designed to monitor the continuing uniformity of all Signetics products and to demonstrate via periodic qualifications that Signetics products meet or exceed the stringent long-term reliability requirements of their intended applications.

The SURE Program is reviewed and modified annually to incorporate appropriate changes in military microelectronic test programs, products and demonstrated product capabilities, and market requirements. The 1978 SURE II/883B Reliability Program contains minor changes to the 1975 SURE II/883A Program, most significant of which is the inclusion of recent changes in military microelectronic test programs (i.e., inclusion of MIL-STD-883B, Method 5005.4 and MIL-M-38510D). The SURE II/883B Program continues to incorporate additional environmental tests to fulfill the need for special reliability assurance of plastic products.

Concept of SURE II Program

Signetics at the present time has approximately 2,500 unique products. The cost to qualify each of these products even once per year via some life testing and some environmental testing would be excessive. Fortunately for the customer and for Signetics, there is no need, technically or otherwise, to pursue this brute-force approach.

Signetics continues to maintain that the way to assure product reliability from both a technical and a cost-effective point of view is to differentiate between assembly/package-related failure mechanisms, and die process-related failure mechanisms. This approach is used in the Signetics SURE II Program with the following definitions:

- Die Process Family. For any die process family, individual device types (regardless of circuit complexity) are fabricated with similar wafer processing. This premise recognizes that circuit layout of a product will have little impact on reliability because established design rules apply to all products fabricated by the same process.
- Package/Assembly Family. For any package/assembly family, packages of like construction are assembled with identical materials, manufacturing operations, and controls.

The general "die process" and "package/assembly" approach to reliability is similar in concept to that now used in the Military Standards for microelectronic testing and reliability.

The number of families can and will change from year to year as new fab processes and packages are introduced and old ones become obsolete. The current Die Process and Package families are defined in the following tables:

Table 12-6	1978 SURE II Die Process Qualification Program Definitions and Schedule.
Table 12-7	1978 SURE II Plastic Package Qualification Program Definitions and Schedule.
Table 12-8	1978 SURE II Hermetic Package Qualification Program Definitions and Schedule.

A Functional Family listing (Table 12-9) is included to show the interrelationships of Die Process Families with the general product categories of Signetics Data Manuals. Note that products within a Functional Family may be manufactured via processes from several Die Process Families. Since all Signetics products, i.e. die, are qualified by the quarterly die process tests, the Functional Families may be not tested in every quarter.

Maintenance of SURE II

Within Signetics, reporting directly to the Corporate Reliability and Quality Assurance Manager, is the Reliability Engineering organization. This group assesses product failure rates/reliability, helps to set guidelines for quality control requirements, provides technical support to customer inquiries, and has the responsibility for formulating, implementing, and maintaining the SURE II program.

At the start of each year, Reliability Engineering contacts all the wafer fab processing groups at Signetics and identifies all standard processes. Out of these discussions the Die Process Families are created. Similar discussions with the packaging groups lead to establishment of the Package Families. Finally, the product groups and Reliability Engineering select candidate devices to represent the families and a schedule for SURE II qualification start dates is created. The criteria in preparing the schedule are that a representative device from each Die Process Family be evaluated once every 90 days (or four times a year), that a representative device from each Package Family be evaluated once semiannually, and that the representative devices be changed routinely to cover the range of products within each family.

Once this schedule is established, the evaluations begin. Reliability Engineering samples units that have gone through the standard process flow and are located in Finished Goods, the last inventory at Signetics prior to shipment to the market. The samples are pulled randomly from Finished Goods just as for any customer. In essence, Reliability Engineering acts as if it were a customer buying Signetics product.

During a year of SURE II qualification testing, the following relationship exists:

SIGNETICS SURE II PROGRAM FOR	QUANTITY OF DEVICES PER QUAL	DEVICES OBTAINED PER TABLE	DEVICES TESTED PER TABLE
Die processes	110	6	2
Plastic packages	272	7	4
Hermetic packages	81	8	3

Analysis of SURE II Process Flow Tables 12-2, 12-3, 12-4

Inspection of Table 12-2, Table 12-3 and Table 12-4 shows that the Signetics SURE II/883B Qualification Program includes Class B requirements of MIL-STD-883B, Method 5005.4 and MIL-M-38510D. Signetics has decided to continue to augment the standard high-temperature operating life test with a 150°C ambient high temperature storage sub group. This provides a common denominator ($T_J = T_A = 150°C$) for evaluating/qualifying all die process families and assures that many products do in fact see a stress at their maximum rated

junction temperature (T_J) values. The die process qualification life tests include 168-hour and 1168-hour time points to allow analysis of 168-hour screening effectiveness. For plastic package qualifications, 200 cycles of −65°C to +150°C thermal shock, 1000 cycles of −55°C to +125°C temperature cycle, 96 hours of 30 PSIA pressure cooker, and 2000 hours of temperature-humidity stress with bias continue to be meaningful measures of reliability.

The primary purpose of the thermal shock and temperature cycle tests is to demonstrate bond wire integrity. The pressure cooker test is an accelerated test that may or may not relate to reality. However, Signetics believes that products which pass this test do demonstrate significant improvement in performance on this test over plastic products that were available in the marketplace several years ago. The temperature-humidity test of 85°C and 85% R.H. with bias applied is an accelerated test that appears to have significance in demonstrating long term reliability under realistic application conditions (e.g. 25°C ambient temperature and 5% to 55% relative humidities).

Acceptance Criteria

The acceptance criteria for die process qualifications are indicated in Table 12-2. Table 12-2 refers to Table 12-5, the Signetics SURE II Criteria for Die Process Families. All die process qualifications involve post stress electrical testing to DC min/max limits, functionality, and the stringent drift criteria indicated. Functionality and DC parameters with drift criteria applied are ample indicators of product stability without the necessity of performing all the Group A subgroups (Table 12-1). From a device physics point of view, the foregoing statement reflects the knowledge that unstable surface fields and conductor resistance changes will produce a significant drift in key reliability parameters such as threshold voltages, offset voltages, supply currents, input currents and input/output voltage levels before an appreciable effect is observed in the AC characteristics. Permanent failure mechanisms such as metal migration or oxide pinhole problems are detected by the functionality and DC parametric tests. From a practical point of view, reliability evaluations are significantly more cost-effective when using functionality, DC parametric, and the drift of key parameters as criteria for reliability assurance. Signetics has found that many customers specify performance of all DC static parameters to data sheet limits, and others may

MIL-STD-883B GROUP A SUBGROUP	TEST DESCRIPTION
A1	Static tests at 25°C
A2	Static tests at maximum rated operating temperature
A3	Static tests at minimum rated operating temperature
A4	Dynamic tests at 25°C *
A5	Dynamic tests at maximum rated operating temperature *
A6	Dynamic tests at minimum rated operating temperature *
A7	Functional tests at 25°C
A8	Functional tests at maximum and minimum rated operating temperatures
A9	Switching tests at 25°C
A10	Switching tests at maximum rated operating temperature
A11	Switching tests at minimum rated operating temperature

NOTE
* Applicable only to Signetics Analog Products

Table 12-1 MIL-STD-883B GROUP A ELECTRICAL TESTS

MIL-STD-883B GROUP C SUBGROUP[4]	TEST DESCRIPTION	MIL-STD-883B METHOD	CONDITIONS	LTPD
-	Pre-Test electrical parameters	-	Subgroup A1 & A4 or A7 as applicable. Refer to Table 1.	Note 1.
-	High temperature storage	1008.1	Test Condition C. T_A = 150°C. t = 168, 1,168 hours.	10
	End-Point electrical parameters	Note 2	Subgroups A1 & A4 or A7 as applicable. Refer to Table 5.	
C1	High temperature operating life	1005.2	T_A = +125°C or +85°C as applicable. t = 168, 1,168 hrs.	10
	End-Point electrical parameters	Note 2	Subgroups A1 & A4 or A7 as applicable. Refer to Table 5.	

NOTES
1. Samples are randomly selected from finished goods, having no reliability prescreen other than standard assembly flow screens. Pre-test electrical (and/or seal, as applicable) performance is expected to be within an AQL of 1%.
2. Only electrically and/or hermetically acceptable parts (as applicable) are to be subjected to this test subgroup. The LTPD acceptance criteria are applicable to the combined 168-hour and 1168-hour results, instead of the results of the 1000-hour period from 168 hours to 1168 hours which is used in MIL-STD-883B.
3. All test equipment calibrated to meet requirements of MIL-C-45662A and MIL-I-45208.
4. The MIL-STD-883B Group D package related tests include the C2 subgroup stresses.

Table 12-2 SIGNETICS SURE II PROGRAM FOR DIE PROCESSES (REFERENCING MIL-STD-883B, GROUP C)

specify drift criteria for specific input/output measurements, while few if any require switching characteristics or tests at minimum and maximum rated operating temperature as life test electrical end-point criteria.

Signetics does test AC switching parameters as well as high and low temperature static parameters on each manufacturing lot and provides positive early feedback to Production Processing via quality assurance inspections. For the more complex MOS and Bipolar Memory circuits, however, the 25°C test programs used for SURE II qualification do include test exercises which ensure switching characteristic limits in addition to the functional performance of the devices. The post-life end-points also include dynamic parameters for Analog devices.

All products/process families meeting the LTPD's and electrical test criteria indicated are automatically qualified for that quarter. Any rejects obtained from qualification testing are submitted for failure analysis. Appropriate corrective action is initiated based upon failure modes and mechanisms identified during failure analysis.

The acceptance criteria for the SURE II Program for hermetic packages and the SURE II Program for plastic packages is indicated in Tables 12-3 and 12-4. Again, failure analysis is performed on every reject.

MIL-STD-883B GROUP B & D SUBGROUP	TEST DESCRIPTION	MIL-STD-883B METHOD	CONDITIONS	LTPD
B2	Resistance to solvents	2015.1		3 devices/0 rej.
	Internal visual and mechanical	2014	No photograph	1 device/0 rej.
	bond strength	2011.2	Test condition D (10 devices min.)	15
B3	High temperature storage	1008.1	Condition B, 160 hours min.	Note 1
	Solderability	2003.2	Solder temperature 260°C ± 10°C	15
D1	Physical dimensions	2016	Attributes data per appropriate Signetics package outline.	15
	Internal water vapor content	1018	5,000 PPM max at 100°C	3 devices/0 rej.
D2	Lead integrity	2004.2	Test condition B2. Note 2	15
	Seal	1014.2		
	a. Fine		Test condition A or B	
	b. Gross	Note 3	Test condition C	
D3	Thermal shock	1011.2	Test condition C, 15 cycles, −65°C to +150°C (Note 4)	15
	Temperature cycle	1010.2	Test condition C, 100 cycles, −65°C to +150°C (Note 4)	
	Moisture resistance	1004.2	10 cycles, no bias.	
	Seal	1014.2		
	a. Fine		Test condition A or B	
	b. Gross		Test condition C	
	Visual examination	Note 5		
	End-point electrical parameters	Note 3	Subgroups A1 & A4 or A7 as applicable. Refer to Table 1.	
D4	Mechanical shock	2002.2	Test condition B	15
	Variable frequency vibration	2007.1	Test condition A	
	Constant acceleration	2001.2	Test condition E, Y1 axis only	
	Seal	1014.2		
	a. Fine		Test condition A or B	
	b. Gross		Test condition C	
	Visual examination	Note 5		
	End-point electrical parameters	Note 3	Subgroups A1 & A4 or A7 as applicable. Refer to Table 1.	
D5	Salt atmosphere	1009.2	Test condition A	15
	Seal	1014.2		
	a. Fine		Test condition A or B	
	b. Gross		Test condition C	
	Visual examination	1009.2 Note 3		

NOTES

1. Preconditioning of the solderability sample satisfies the time/temperature requirement of Class B screening (burn-in). The LTPD for the solderability test applies to the number of leads inspected from a minimum of three devices.
2. For DIP's, 15 devices, all leads on each device. For FlatPacs, 15 devices, 3 leads on each device.
3. Only electrically and/or hermetically acceptable parts (as applicable) are to be subjected to this test subgroup.
4. Test Condition B for FM and FN packages.
5. Visual examination shall be in accordance with Method 1010.2 or 1011.2 at a magnification of 5X to 10X.
6. All test equipment calibrated to meet requirements of MIL-C-45662A and MIL-I-45208.

Table 12-3 SIGNETICS SURE II PROGRAM FOR HERMETIC PACKAGES (PER MIL-STD-883B, GROUP B & D)

MIL-STD-883B GROUP B & D SUBGROUP	TEST DESCRIPTION	MIL-STD-883B METHOD	CONDITIONS	LTPD/MAX. ACC.
B2	Resistance to solvents Internal visual and mechanical	2015.1 2014	 No photograph	3 devices/0 rej. 1 device/0 rej.
B3	High temperature storage Solderability	1008.1 2003.2	Condition B, 160 hours min. Solder temperature 260°C ± 10°C	Note 1 15
D1	Physical dimensions	2016	Attributes data per appropriate Signetics package outline.	15
D2	Lead integrity	2004.2	Test condition B2. Note 2.	15
D3	Thermal shock, extended End point electrical parameters	1011.2 Note 5	200 Cycles, Test Condition C, −65°C to +150°C (Note 3) Subgroup A7 & Thermal Scan (Note 4)	5
D3	Temperature cycle, extended End-point electrical parameters	1010.2 Note 5	Test condition B, 1000 cycles, −55°C to +125°C (Note 6) Subgroup A7 & Thermal Scan (Note 4)	5
D3	Moisture resistance End-point electrical parameters	1004.2 Note 5	10 cycles, no bias Subgroup A1 & A4 or A7 as applicable. Refer to Table 1.	15
D4	Mechanical shock Variable frequency Vibration Constant acceleration End-point electrical parameters	2002.2 2007.1 2001.2 Note 5	Test condition B Test condition A Test condition E Subgroup A1 & A4 or A7 as applicable. Refer to Table 1.	15
D5	Salt atmosphere, Note 7 End-point electrical parameters Visual examination	1009.2 Note 5 1009.2	Test condition A Subgroup A1 & A4 or A7 as applicable. Refer to Table 1.	15
-	Pressure cooker End-point electrical parameters	- Note 5	96 hours, 30 PSIA (Note 8) Subgroup A1, A4 or A7 as applicable. Refer to Table 1.	10
-	Biased temperature-humidity End-point electrical parameters	- Note 5	85°C/85% R.H. with 5V min. bias, t = 2000 hours (Note 9) Subgroup A1, A4 or A7 as applicable. Refer to Table 1.	 10/2

NOTES
1. Preconditioning of the solderability sample satisfies the time/temperature requirement of Class B screening. The LTPD for the solderability test applies to the number of leads inspected from a minimum of three devices.
2. For DIP's, 15 devices, all leads on each device. For FlatPacs, 15 devices, three leads on each device.
3. 100 cycles for Silicone DIP and power flange mounted Families IV and V.
4. Refer to Table 11-1 for Subgroup A7 definition. Thermal scan refers to a test that monitors bond continuity continuously over the temperature range of 25°C to 125°C.
5. Only electrically acceptable parts are to be subjected to this test subgroup.
6. 500 cycles for Silicone DIP and power flange mounted Families IV and V.
7. Not applicable for Silicone DIP and power flange mounted Families IV and V.
8. 24 hours 30 PSI for Silicone DIP and power flange mounted Families IV and V.
9. 1000 hours for Silicone DIP and power flange mounted Families IV and V.
10. All test equipment calibrated to meet requirements of MIL-C-45662A and MIL-I-45208.

Table 12-4 SIGNETICS SURE II PROGRAM FOR PLASTIC PACKAGES (REFERENCE MIL-STD-883B, GROUP B & D.)

PARAMETER	DELTA LIMIT
TTL, SCHOTTKY, LOW POWER SCHOTTKY, AND IIL[1, 2]	
"1" Input current	5X initial value or 25% of limit.[3]
"0" Input current	±20% of initial value or ±5μA[3]
"1" Output voltage	±20% of initial value
"0" Output voltage	±100 mV
I_{OH} Output leakage current[4]	±10% of limit
I_{CC} Supply current	±20% of limit
ECL (EMITTER COUPLED LOGIC)[1, 2]	
"1" Input current	±20% of initial value of ±35μA[3]
"0" Input current	±20% of initial value or ±15μA[3]
"1" Output voltage	±20% of initial value
"0" Output voltage	±20% of initial value
I_{EE} Supply current	±20% of limit
NMOS[1, 2]	
Leakage currents[4]	±10% of limit
I_{sink}[4]	±20% of initial value
I_{source}[4]	±20% of initial value
Access time[4]	±20% of initial value
All supply currents	±20% of limit
DMOS (DOUBLE DIFFUSED MOS)[1]	
V_T	±30% of initial value or ±200 mV[3]
$R_{ds\ (on)}$	±20% of limit

NOTES
1. All products are tested to subgroups A1, A4 or A7, as applicable. Refer to Table 12-1. The detailed tests, conditions and limits applicable to each product are listed in the Signetics Data Manual Electrical Characteristics Table. All parameters must meet the min./max. limits as well as the delta limits shown.
2. All Programmable Read Only Memories (PROM's) are programmed to a pseudorandom pattern prior to stress and the programming verified after stress.
3. Whichever is greater.
4. As applicable by product type.

Table 12-5A SURE II DIE PROCESS ACCEPTANCE CRITERIA

What Does SURE II Do For You?

- SURE II provides fingertip data that demonstrates the reliability of Signetics products. Data summaries from each SURE II qualification test are available for customer inquiries. Semiannual comprehensive summaries are also available for customer inquiries.**
- SURE II allows the customer to qualify Signetics products based upon testing at Signetics. This is a cost effective approach, as it allows many customers to use the same qualification results, thereby saving money industry-wide.
- SURE II provides assurance that all Signetics Fab processes meet established reliability standards on a continuous basis.
- SURE II provides assurance that all Signetics packages meet established reliability standard on a continuous basis.
- SURE II provides basic attributes data which is quoted in Product Reliability reports and is used in failure calculations.
- SURE II provides variables data on key drift parameters (as well as additional parameters) for all storage and operating life tests. This data is available for inspection at Signetics and can be obtained for a nominal fee.

**To obtain a copy, contact the QRA Department, Signetics Corp., 811 E. Arques, P.O. Box 9052, Sunnyvale, CA 94086 (408) 739-7700

PARAMETER	ANALOG PRODUCTS DELTA LIMITS[1]									
	Operational/ Differential Amplifiers	Sense Amplifier	Video & RF/IF Amplifier	Voltage Comparators	Communications & Function Gen Circuits[3]	Timers	Voltage Regulators	Phase Locked Loops	Interface Circuits[3]	Gas Tube Decoder/ Drivers
Power Supply or Quiescent current	±20% of limit	±20% of limit	±20% of limit	±20% of limit	±20% of limit	±20% of limit	±20% of limit	±20% of limit	±20% of limit	±20% of limit
V_{OS} Input offset voltage[4]	±1 mV			±1 mV						
I_{OS} Input offset current[4]	±20% of limit			±20% of limit						
I_{BIAS} Input bias current		±30% of limit								
V_T Input threshold voltage		±1 mV								
Voltage gain			±20% of initial value	±20% of initial value						
Output voltage						±0.20 V	±20% of initial value			
Trigger voltage						±0.10 V				
Initial accuracy						±1% (absolute value)				
Center frequency of oscillation								±10% of initial value		
"1" Input current		5X initial value or 25% of limit[5]							5X initial value or 25% of limit[5]	5X initial value or 25% of limit[5]
"0" Input current		±20% of initial value or ±5 μA[5]							±20% of initial value or ±5 μA[5]	±20% of initial value or ±5 μA[5]
"1" Output voltage		±20% of initial value							±20% of initial value	
"0" Output voltage		±100 mV							±100 mV	
Output breakdown voltage										±20% of initial value
I_{OH} Output leakage current										±300 nA

NOTES
1. All products are tested to subgroups A1, and to either A4 or A7 as applicable. Refer to Table 1. The detailed tests, conditions, and limits applicable to each product are listed in the Signetics Data Manual ELECTRICAL CHARACTERISTICS table. All parameters must meet the min/max limits as well as the data limits shown.
2. Radios, receivers, modulators, demodulators, detectors.
3. MOS clock drivers, line drivers, line receivers.
4. As applicable, by product type.
5. Whichever is greater.

Table 12-5B SURE II DIE PROCESS ACCEPTANCE CRITERIA

PROCESS FAMILY	DESCRIPTION	PROCESS CODE	FUNCTIONAL FAMILY[1]	CANDIDATE DEVICE	QUARTER START[2] 1	2	3	4
I TTL DTL	Gold doped slow Speed-High/Low Voltage	A	1	7440, 7447A, 7490, 7492	7440		7492	
		A	8	8T04, 8T06, 8T16		8T04		
		A1	1	7426, 7446				
		B1	8	8T18, 8T80, 8T90				8T18
		B1	12	μA710				
II TTL	Gold doped fast speed Low voltage	C1	1	7437, 7485, 7496, 74H30 8201, 8242	7496	7485		7437
		C1	8	8T14, 8T363				
		C2	1	74109, 74181, 74H04 74H103, 8225, 8260			74109	
		C2	8	8T10, 8T34				
		C5	1	7406, 74145				
		CA	1	74107, 74152, 8270, 8271				
		D	1	74147, 74148				
III Schottky	Standard aluminum Schottky	E4	5	82S290, 82S291				
		P2S	15	8X300				
		R2	5	82S215, 82S280	82S280			
	Single level metal (SLM) or dual level metal (DLM)	X2	2	74S114, 74S135		74S114		
		X2	4	82S12, 82S112				
		X2	12	NE521, NE522				NE521
		X6	12	NE527, NE529			NE527	
		X7	2	74S174, 74S175, 82S30				
IV Schottky PROM's	Standard aluminum Schottky (DLM) plus Ni-Cr Fuses	D5	5	82S190, 82S191				
		R5	5	82S101, 82S130, 82S140, 82S181, 82S185	82S181	82S185	82S140	82S130
V Schottky	Silicide Schottky (SLM) or (DLM)	R4	4	74S89, 74S189, 82S25				82S25
		S4	4	74S201, 82S09, 82S16		82S09		
		X3	2	74S140, 82S34, 82S62	74S140			
		X3	8	8T100, 8T111				
		X3	15	N3001, N3002			N3002	
		X4	2	74S112, 74S181				
		X4	8	8T31				
		Z3	5	8228				
VI Schottky (LS)	Silicide Schottky Ion implantation (SLM) or (DLM)	V3	2	74LS74, 74LS138 74LS193, 74LS241	74LS74	74LS241	74LS138	74LS193
		V3	8	8T28				
VIII ECL	Aluminum ECL (SLM) or (DLM)	RTC	3	10102, 10118, 10180			10118	10180
				10104, 10113, 10130	10113	10130		
IX Schottky	Silicide Schottky, washed emitter (DLM)	A4	4	82S10,82S11	82S10	82S11	82S10	82S11
X Schottky (I^2L)	Silicide Schottky, integrated injection (SLM) or (DLM)	I1	15	8X01	8X01	8X01	8X01	8X01
		I2	15	8X03, 8X04, 8X06, 8X07				
XI Linear	High voltage process	JX	10	LF356		LF356		
		M	10	LM101, μA709, SE531				
		M	11	NE550				
		M	12	LM111, LM339, MC3302	LM339			
		M	13	NE540				
		M3	9	NE584, NE585				
		MC	12	NE5018				NE5018
		ME	9	DM8880				
		MX	10	LM207, MC1558, μA747				
		MX	11	μA723				
		MX	12	LM319				
		PX	10	MC1456, NE536		MC1456		
		R	10	LM208A				
		RX	10	NE535, NE5535			NE5535	

Table 12-6 1978 SURE II DIE PROCESS QUALIFICATION PROGRAM DEFINITIONS AND SCHEDULE

PROCESS FAMILY	DESCRIPTION	PROCESS CODE	FUNCTIONAL FAMILY[1]	CANDIDATE DEVICE	QUARTER START[2] 1	2	3	4
XII Linear	Medium voltage process	E	9	MC1488				
		E	13	MC1496, NE565, NE645	NE565		NE645	
		E2X	11	78L05C, NE5554		NE5554		
		EX	10	LM324, NE532				
		EX	13	NE545				
		LX	13	NE542				
		Q	11	7905C, 79M05C				
		Q2	11	LM309				
		QX	11	7805C, 78M05C				7805C
		X	13	TCA440N				
XIII Linear	Low voltage process	B	12	μA711				
		B2	2	75324, 75451, DM8820		75451		
		G	9	75361				
		H	9	7520, 7524, MC1489				
		H	12	NE526				
		H	13	NE501, NE515				
		K	13	NE592, TBA1440, μA733				
		L	13	NE510, NE546, NE556, TBA120U	TBA120U			
		L5	13	NE570			NE570	
		W	13	NE543				
		W1	9	NE582				
		W2	13	NE544				NE544
XIV DMOS	Double diffused MOS, N-Channel, ion implanted	L2A	14	SD200, SD305, SD5000, SD5301	SD5000	SD5301		SD305
		L2B	14	SD202, SD306, SD307			SD306	
XVI NMOS	N-Channel enchancement MOS	NA	7	2101, 2102, 2111, 2112	2102		2112	
		NB	7	2607, 2608, 2609, 2606		2609		2609
		NH	7	4027	4027	4027	4027	4027
XVII NMOS	N-Channel depletion MOS	ND	7	2102A, 2600, 2616, 2617	2102A	2600	2102A	2616
NMOS	N-Channel double-poly MOS	NE	7	2708	2708		2708	2708
XIX NMOS	N-Channel, depletion MOS MPU	NG	15	2650A	2650A		2650A	

NOTES
1. See Table 12-9 for a listing of devices by Functional Family.
2. SURE II Die Process Sample Sizes are >55 each for HTSL and HTOL.

Table 12-6 (Cont'd) **1978 SURE II DIE PROCESS QUALIFICATION PROGRAM DEFINITIONS AND SCHEDULE**

FAMILY	DESCRIPTION	PACKAGES IN FAMILY (CODE DESIGNATION)			QUARTER START	
					1	3
I	Plastic DIP (Epoxy)	NE-8-Lead NH-14-Lead NJ-16-Lead	NK-18-Lead NL-20-Lead NM-22-Lead	NN-24-Lead NQ-28-Lead	NJ (82S16)	NN (74150)
II	Plastic power DIP (Epoxy)	NHA-14-Lead NJA-16-Lead NKA-18-Lead	NLA-20-Lead NNA-24-Lead NQA-28-Lead	PH-12-Lead & Batwing PHA-12-Lead & Batwing	NJA (82S131)	PHA (NE541)
III	Plastic power SIL or DIP lead mounted (Epoxy)	S-3-Lead (TO-92)			S (78L05)	S (78L05)
IV	Plastic DIP (Silicone)	NEB-8-Lead NHB-14-Lead	NJB-16-Lead NKB-18-Lead	NMB-22-Lead NNB-24-Lead	NJB (2102)	NJB (2102A)
V	Plastic power-flange mounted (Silicone)	U-3-Lead (TO-220)			U (79M05)	U (7805)

Table 12-7 1978 SURE II PLASTIC PACKAGE QUALIFICATION PROGRAM DEFINITIONS AND SCHEDULE

FAMILY	DESCRIPTION	PACKAGES IN FAMILY (CODE DESIGNATION)			QUARTER START	
					1	3
I	FlatPac, laminated ceramic body and lid, glass seal	QFA-10-Lead QHA-14-Lead	QJA-16-Lead QNA-24-Lead		QJA (54157)	QNA (54150)
II	FlatPac, beryllia body and lid, glass seal	RJA-16-Lead RKA-18-Lead	RNA-24-Lead RQA-28-Lead	RWA-40 Lead	RJA (82S11)	RNA (82S181)
III	FlatPac, ceramic CerPac	WF-10-Lead WH-14-Lead	WJ-16-Lead WN-24-Lead		WJ[1]	WN[1]
IV	DIP, ceramic CerDip	FE, SSI-8-Lead FH, SSI-14-Lead FH, MSI-14-Lead FJ, SSI-16-Lead	FJ, MSI-16-Lead FJ, LSI-16-Lead FK, LSI-18-Lead	FL, LSI-20-Lead FM, LSI-22-Lead FN, LSI-24-Lead	FJ,[1] SSI	FJ, SSI (82S10)
V	DIP, ceramic body and lid, glass seal, side brazed leads	IEA-8-Lead IHA-14-Lead IJA-16-Lead	IKA-18-Lead IMA-22-Lead INA-24-Lead	IQA-28-Lead IWA-40-Lead IZA-50-Lead	INC (82S214)	IKA (82S136)
VI	Solid header with mounting holes	DA-2-Lead (TO-3)			DA (LM309)	DA (7805)
VII	Metal can (Header)	DB-3-Lead (TO-39) DC-4-Lead (TO-72) DE-4-Lead (TO-72)	K-10-Lead (TO-100) L-10-Lead (TO-100) T-8-Lead (TO-99)		T (μA709)	K (LM119)

NOTE
1. JAN test data will be used to verify compliance with SURE II qualification criteria.

Table 12-8 1978 SURE II HERMETIC PACKAGE QUALIFICATION PROGRAM DEFINITIONS AND SCHEDULE

FUNCTIONAL FAMILY	DESCRIPTION	DIE PROCESS		CANDIDATE DEVICES	QUARTER START			
		CODE	FAMILY		1	2	3	4
Logic 1	Standard TTL	A	I	7440, 7447A, 7490, 7492	7440		7492	
		A1	I	7426,7446				
		C1	II	7437, 7485, 7496	7496	7485		7437
		C2	II	74109, 74181			74109	
		C5	II	7406, 74145				
		CA	II	74107, 74152				
		D	II	74147, 74148				
	High-Speed Standard TTL	C1	II	74H30				
		C2	II	74H04, 74H103				
	Standard TTL MSI	C1	II	8201, 8242				
		C2	II	8225, 8260				
		CA	II	8270, 8271				
Logic 2	Schottky TTL MSI	X3	V	82S34, 82S62				
		X7	III	82S30				
	Schottky TTL	X2	III	74S114, 74S135		74S114		
		X3	V	74S140	74S140			
		X4	V	74S112, 74S181				
		X7	III	74S174, 74S175				
	Low Power Schottky TTL	V3	VI	74LS74, 74LS138, 74LS193, 74LS241	74LS74	74LS241	74LS138	74LS193
Logic 3	Aluminum ECL	RTC	VIII	10102, 10118, 10180			10118	10180
				10104, 10113, 10130	10113	10130		
Memory 4	Schottky RAM	A4	IX	82S10, 82S11	82S10	82S11	82S10	82S11
		R4	V	74S89, 74S189, 82S25				82S25
		S4	V	74S201, 82S09, 82S16		82S09		
		X2	III	82X12, 82S112				
Memory 5	Schottky ROM	E4	III	82S290, 82S291				
		R2	III	82S215, 82S280	82S280			
		Z3	V	8228				
	Schottky PROM	D5	IV	82S190, 82S191				
		R5	IV	82S101, 82S130, 82S140, 82S181, 82S181	82S181	82S185	82S140	82S130
Memory 7	NMOS Enhancement	NA	XVI	2101, 2102, 2111, 2112	2102		2112	
		NB	XVI	2607, 2608, 2609, 2606		2609		2609
		NH	XVI	4027	4027	4027	4027	4027
	NMOS Depletion	ND	XVII	2102A, 2600, 2616, 2617	2102A	2600	2102A	2616
	NMOS EPROM	NE	XVIII	2708	2708		2708	
Interface 8	Logic Interface	A	I	8T04, 8T06, 8T16		8T04		
		B1	I	8T18, 8T80, 8T90				8T18
		C1	II	8T14, 8T363				
		C2	II	8T10, 8T34				
		V3	VI	8T28				
		X3	V	8T100, 8T111				
		X4	V	8T31				

NOTES

1. The Functional Family definitions are derived from the Signetics Data Manual and follow the Data Manual organization to assist the user in identifying the Die Process Family that is qualifying the product of interest.
2. The Functional Family Qualification Schedule is derived for the Die Process Family Qualification Schedule. A Die Process Family Quarterly Test can qualify products in more than one Functional Family, since a Die Process Family can contain products from several Functional Families.

Table 12-9 1978 SURE II FUNCTIONAL FAMILY QUALIFICATION SCHEDULE

FUNCTIONAL FAMILY	DESCRIPTION	DIE PROCESS		CANDIDATE DEVICES	QUARTER START			
		CODE	FAMILY		1	2	3	4
Interface 9	Analog Interface	B2	XIII	75324, 75451, DM8820		75451		
		E	XII	MC1488				
		G	XIII	75361				
		H	XIII	7520, 7524, MC1489				
		M3	XI	NE584, NE585				
		ME	XI	DM8880				
		W1	XIII	NE582				
Analog 10	Operational Amplifiers	EX	XII	LM324, NE532				
		JX	XI	LF356		LF356		
		M	XI	LM101, SE531, μA709				
		MX	XI	LM207, MC1558, μA747				
		PX	XI	MC1456, NE536		MC1456		
		R	XI	LM208A				
		RX	XI	NE535, NE5535			NE5535	
Analog 11	Operational Amplifiers	E2X	XII	78L05C, NE5554		NE5554		
		M	XI	NE550				
		M	XI	μA723				
		Q	XII	7905C, 79M05C				
		Q2	XII	LM309				
		QX	XII	7805C, 78M05C				7805C
Analog 12	Comparators and Converters	B	XIII	μA711				
		B1	I	μA710				
		H	XIII	NE526				
		M	XI	LM111, LM339, MC3302	LM339			
		MC	XI	NE5018				NE5018
		MX	XI	LM319				
		X2	III	NE521, NE522				NE521
		X6	III	NE527, NE529			NE527	
Analog 13	Consumer Circuits	E	XII	NE645			NE645	
		EX	XII	NE545				
		L	XIII	NE546, TBA120U	TBA120U			
		L5	XIII	NE570			NE570	
		LX	XII	NE542				
		M	XI	NE540				
		W	XIII	NE543				
		W2	XIII	NE544				NE544
	Timers	L	XIII	NE556, NE555, NE5556				
	Differential Amplifiers	H	XII	NE515				
		L	XIII	NE510, NE511				
	Video Amplifiers	H	XIII	NE501				
		K	XII	NE592, μA733				
	Phase Locked Loops	E	XII	MC1496, NE565	NE565			
		K	XIII	TBA1440				
		L	XIII	NE567, PA239				
		X	XII	TCA440N				
Analog 14	Double Diffused MOS (DMOS)	L2A	XIV	SD200, SD305, SD5001, SD5301	SD5001	SD5301		SD305
		L2B	XIV	SD202, SD306, SD307			SD306	
Microprocessor 15	IIL, MOS, and Schottky LSI	I1	X	8X01	8X01	8X01	8X01	8X01
		I2	X	8X03, 8X04, 8X06, 8X07				
		NG	XIX	2650A	2650A		2650A	
		P2S	III	8X300				
		X3	V	N3001, N3002			N3002	

NOTES

1. The Functional Family definitions are derived from the Signetics Data Manual and follow the Data Manual organization to assist the user in identifying the Die Process Family that is qualifying the product of interest.
2. The Functional Family Qualification Schedule is derived for the Die Process Family Qualification Schedule. A Die Process Family Quarterly Test can qualify products in more than one Functional Family, since a Die Process Family can contain products from several Functional Families.

Table 12-9 (Cont'd) **1978 SURE II FUNCTIONAL FAMILY QUALIFICATION SCHEDULE**

UNDERSTANDING FAILURE RATES

UNDERSTANDING FAILURE RATES

UNDERSTANDING FAILURE RATES

This section is designed to acquaint the I.C. user with some of the more commonly accepted "scientific approaches" used by an I.C. Reliability Analyst to determine whether the raw data has a probable bearing on the longevity of the I.C. in its intended system environment. The methods presented do not imply that there are not other (or better) approaches available. This section contains general information intended to stimulate one's imagination and acquaint the reader with the large degree of error that is possbile in any assessment or prediction of I.C. reliability (one must know the future to be 100% correct in predicting).

The Classical "Bathtub Curve"

Figure 13-1 suggests that a given product operating in a real-life application has "infant mortality" failure mechanisms which initially inflate the failure rate (up to t_1) such that once these mechanisms result in failure, the remaining devices will demonstrate a failure rate which is constant with time (t_1 to t_2) until some future time (years) when product wearout begins and ultimately ends the product's useful life (curve a). If this model is correct, then one approach would be to use accelerated screens to eliminate the "infant mortality" in a time less than t_1 so that once the region of random failures is reached the accelerated screens could be stopped and the surviving devices inserted in a system at the constant hazard failure rate level of curve a. Curve b suggests what would happen if the accelerated screens, especially a high-temperature operating life stress (e.g., burn-in) were allowed to continue indefinitely. The ratio of the failure rates for the constant hazard segment of curve a to that of curve b is what is usually considered to be the "acceleration factor" associated with accelerated life tests.

In regard to the bathtub curve model, two statements are necessary for proper perspective:

It has not yet been satisfactorily demonstrated with any certainty or repeatability that a bathtub curve actually exists (much less its shape) for a given product-application combination. Part of the reason for this could be that semiconductors appear to outlive people. Enough literature exists, however, to support the statement that for certain unique lots of devices, appropriate screens do, in fact, have a positive impact on subsequent failure rates.

Signetics Reliability Engineering has found that the "typical" unscreened Signetics product does not exhibit a "bathtub curve" when placed on accelerated storage or operating life tests at $T_A \geq 85°C$ for many thousands of hours. Typical Signetics products do not demonstrate a disproportionate number of early life test failures as compared to the total quantity of failures experienced during the course of an accelerated life test. Any observed decrease in the failure rate at early timepoints is more likely to be associated with the effect of an increase in the quantity of device hours rather than a decrease in the quantity of failures per unit time. When one considers the many manufacturing factors that can have an impact on the failure rate at any given time, it should not be surprising to see increasing, decreasing or constant (could be zero) "speeds of failure."

FAILURE RATES VS. TIME "BATHUB CURVE"

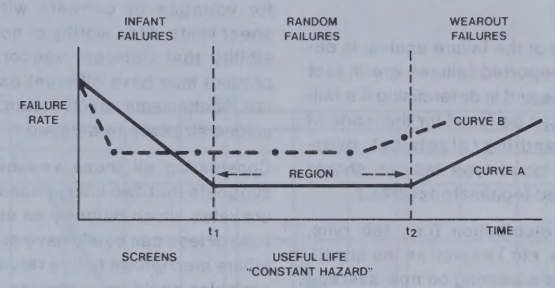


Figure 13-1

The Failure Rate Equation

Signetics uses the term "failure rate" primarily to refer to the performance of products which are life tested under steady state temperature conditions and in a relatively dry environment. It is essential that other variables (thermo-mechanical, humidity, etc.) be controlled as much as is possible so as to not have a significant influence on these assessed failure rate values. The environmental impact would need to be considered separately and factored into the real life application failure rate prediction. Section 3 of this report covers the present Signetics dry environment assessed failure rate values in detail. The failure rate equation that is used by Signetics to assess failure rates is defined as follows:

$$\lambda = \frac{F}{NtA} \times 10^5 \text{ where:}$$

λ = assessed failure rate in % per 1000 hours at temperature T_1. (This value can be multiplied by 10^4 to obtain FIT's which are "failure units," i.e., one failure per 10^9 hours or multiplied by 10 to obtain failures per million hours.)

F = The quantity of failures occurring at a temperature T_2 in a time interval t.

N = The quantity of acceptable devices at zero hour.

t = The time interval.

A = The temperature acceleration factor that relates the T_2 failure rate to the failure rate at the desired T_1 temperature.

Signetics uses a reliability calculator (or reliability slide rule) to adjust the assessed failure rate to a 60% upper confidence level. The assessed failure rate at other confidence levels can be obtained by selecting the desired confidence level and inputting into the calculator the number of failures and the total number of device hours. Confidence levels are used to relate to the dispersion of failure rate values which would be expected to exist if the experiment were repeated many times under the same conditions. The confidence values are a measure of the total area under a % frequency vs. % failure rate dispersion plot. Signetics calculations (i.e., reliability calculators) are based on the assumption that this graph follows a chi squared distribution. The calculations also assume that the failure rate (λ) is constant with respect to time (i.e., Figure 13-1 Constant Hazard). The 60% upper confidence value in essence means that if the life tests were to be repeated, there is a 60% probability that the new failure rate will be equal to or less than the given assessed failure rate value.

Assessed failure rates can vary widely. The more important factors which can significantly affect assessed failure rates include:

The actual failure mechanisms present.

The definition of what constitutes a "failure" (for both catastrophic and degradational failures).

The comprehensiveness of the electrical test program used to detect a "failure." Various I.C. electrical test programs can

produce various failure rates. (This is especially true for MSI and LSI devices where the exact cause of a "failure" may not be identifiable).

The competence of the failure analyst in determining if the reported failures are in fact legitimate failures and in determining if a failure mechanism can be found for the mode of failure. (Mishandling/electrical overstress/retested good type failures should not be considered legitimate failures.)

The population distribution (i.e., fab runs, assembly weeks, etc.) as well as the quantity of devices has a bearing on how average a failure rate the assessed failure rate is.

The length of stress is important. If an I.C. manufacturer knew that he had a decreasing failure rate with time, it might be in his interest to use a smaller quantity and longer stress times to obtain a device-hour product related to fewer failures (i.e., a lower assessed failure rate).

The removal of degradational failures from the population before they have a chance to become catastrophic can affect the assessed catastrophic failure rate.

Failure rate of screened vs. unscreened devices (i.e., origin of population for a population with a non-constant failure rate).

The acceleration factor used to derate from a T_2 temperature to a T_1 temperature.

The quantity of device-hours and its effect on a device-hour limited failure rate (i.e., the failure rate may be large only because not enough device-hours have been accumulated).

The stress used. Temperature is widely recognized as having an accelerating affect on most failure mechanisms. For this reason failure rates are quoted at a specific temperature. Reverse biasing of junctions and biasing of MOS gates can produce an accelerating affect on die surface related failure mechanisms. Current accelerates bulk failure mechanisms as well as electro-migration. However, voltage or current acceleration factors have not as yet been identified for voltages or currents within the data sheet limits. Also worthy of note is the possibility that different vendors of a given product may have different associated failure mechanisms which in turn might dictate unique stresses to be used.

Considering all these variables, Signetics suggests that two unique assessed I.C. failure rates which differ by an order of magnitude or less can easily have equal legitimate failure mechanism failure rates if, in fact, the variables could be controlled.

Failure Rate Requirements vs. Demonstrating The Required Failure Rate

Table 13-1 lists some recently published estimates of I.C. failure rates required to meet specific system requirements. The failure rate ranges shown reflect the total range based on five sources of inputs per system repair difficulty category. Table 13-1 is not meant to be an endorsement of those failure rate levels but rather to show some exisiting typical I.C. failure rate rquirements. The system lifetime requirements, on the other hand, typically fall in the range of 2 to 30 years.

Table 13-2 is a demonstration of the minimum effort (cost related) that would be needed to determine whether an assumed failure rate-mean time between failure requirement can be met by a specific I.C. product at temperature T_1. This table dramatizes the importance of accelerated testing at a temperature $T_2 \gg T_1$ and the need for combining life test data of similar products/processes to obtain a large enough device hour product for meaningful generic failure rate assessments. Combining data and the use of accelerated testing does, of course, leave unanswered the question of whether or not the mean time between an I.C. failure at T_1 is in fact 114 years for a 0.1% per 1000 hour failure rate (i.e., instead of waiting 114 years for the answer, engineering approaches are used over relatively short time periods due to a lack of a realistic alternative).

Temperature Acceleration Factor

Signetics uses the temperature acceleration factor graph (1) of Figure 13-2 to relate

SYSTEM REPAIR DIFFICULTY	RANGE OF I.C. FAILURE RATES (%/1000 HRS.)
Standard	0.1 to 0.003
M.S. 883, Level C, Avionics Easy Repair	0.01 to 0.045
M.S. 883, Level B, Avionics Difficult Repair	0.003 to 0.008
M.S. 883, Level A, Space Repair "Impossible"	0.002 to 0.005

(1) Summary of Table IX, Peattie, et al, "Elements of Semiconductor-Device Reliability," Proceedings of the IEEE, Vol. 62, No. 2, February, 1974.

Table 13-1 ESTIMATES OF I.C. FAILURE RATE REQUIREMENTS(1)

ASSUMED REQUIREMENT		EFFORT NEEDED-QUANTITY DEVICES VS TIME*		
λ@ T_1 (%/1000 Hours)	MTBF@T_1	1 Year	10 Years	100 Years
0.1	10^6 Hours (114 Years)	114	12	2
0.01	10^7 Hours (1,140 Years)	1,140	114	12
0.001	10^8 Hours (11,400 Years)	11,400	1,140	114
0.0001	10^9 Hours (114,000 Years)	114,000	11,400	1,140

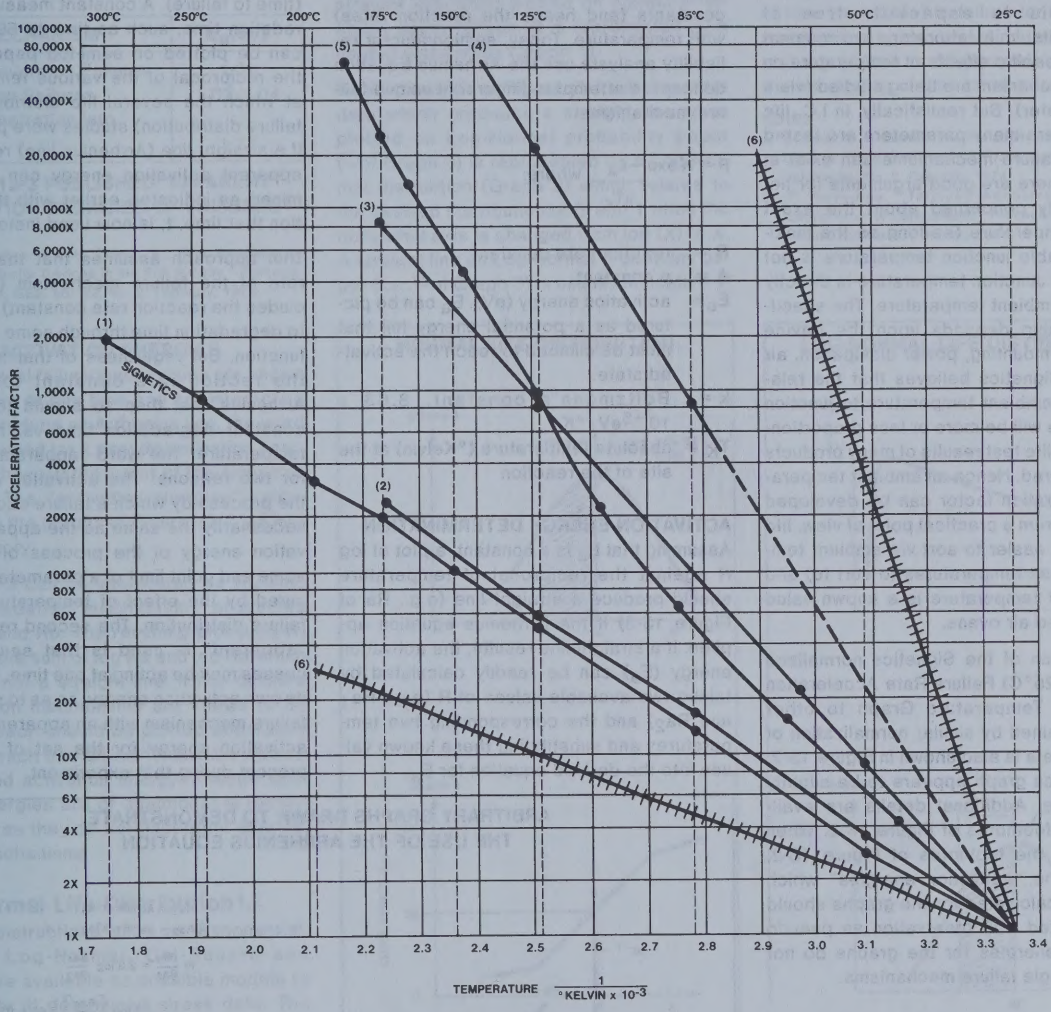
NOTE

1. MTBF = $1/\lambda$. MTBF ≠ MTTF.

Demonstration of the quantity of devices (assuming 0 failures) that would be needed to be placed on stress @ Temperature T_1 for the length of time (years) shown to demonstrate the ability to meet the MTBF/failure rate requirements at T_1.

Table 13-2 EFFORT NEEDED TO DEMONSTRATE REQUIRED FAILURE RATE

FAILURE RATE ACCELERATION FACTOR VS. TEMPERATURE GRAPHS — SIGNETICS AND OTHERS



NOTES

1. Calculated from the Signetics Failure Rate vs. Temperature Graph of Figure 3-2. Signetics uses acceleration factors of 15 (for +85° C), 100 (for +150° C), 200 (for +175° C 350 (for +20° C), 970 (for +250° C) and 2100 (for +300° C) to relate to +25° C ..ivalent ambient temperature. The +25° C to +125° C segment of the graph is based primarily on operating life data. The segment of the graph above +125°C is based on high temperature storage data. The graph equates to an "activation energy" E_a 0.41eV.
2. Calculated from MIL-HDBK-217B, 20 September, 1974, Table 2-1.5-4 for π T_1 vs T_J values. The graph equates to an "activation energy" E_a=0.41eV and is applicable to all bipolar digital (except ECL) in the normal mode of operations.
3. Calculated from MIL-HDBK-217B,20 September, 1974, Table 2.1.5-4 for π t vs T_J values. The graph equates to an "activation energy" E_a = 0.70eV and is applicable to all MOS, all linear, and bipolar ECL devices in the normal mode of operation.
4. Calculated from MIL-STD-883A, 15 November 1974. Figures 1005-4 and 1015-1 by extrapolating the time temperature regression graph from +78°C back to +25° C. The MIL-STD-883A graph is the Bell Telephone Laboratories graph (Specification AB-689143, 16 January 1974, etc.) and as such applies to storage and operating T_J values and primarily surface inversion failure mechanisms. The graph equates to an "activation energy" E_a = 1.02eV.
5. This curved graph is the result of plotting the "rule of thumb" that failure rates (hence acceleration factors) double for every +Δ10° C.
6. All competitor data (available to Signetics) produced graphs falling within these two boundaries. The two boundaries equate to "activation energies" E_a = 0.23eV (for lower graph) and E_a = 1.92eV (for the top graph).

Figure 13-2

life test data generated at a specific ambient temperature to the +25°C ambient temperature "equivalent."

Technically, an acceleration factor graph should be based on junction temperature (T_J) values instead of ambient temperatures. This is especially true of experiements in a laboratory environment when the specific effects of temperature on a failure mechanism are being studied (via a key parameter). But realistically, in I.C. life testing, where many parameters are tested and many failure mechanisms can exist at one time, there are good arguments for not being overly concerned about the exact junction temperature (as long as the maximum allowable junction temperature is not exceeded). Junction temperature is directly related to ambient temperature. The specific relationship depends upon the device packaging, mounting, power dissipation, air flow, etc. Signetics believes that the relationship of ambient temperature to junction temperature will be more or less proportional when the life test results of many products are considered. Hence an ambient temperature acceleration factor can be developed and used. From a practical point of view, life test data is easier to sort via ambient temperature (less temperatures to sort to) and the ambient temperature is a known value due to forced air ovens.

A comparison of the Signetics normalized (to T_A = +25°C) Failure Rate Acceleration Factor vs. Temperature Graph to other graphs obtained by similar normalization of published data is also shown in Figure 13-2. The Signetics graph appears to be slightly conservative. Additional details are available in the footnotes of Figure 13-2. When interpreting the footnotes of Figure 13-2, note that the "activation energies" which have been calculated for the graphs should be interpreted with reservation as pseudo activiation energies for the graphs do not relate to single failure mechanisms.

The Arrhenius Equation vs. Activation Energies

Some chemical reactions occur nearly instaneously, some are so slow that they are not perceptible at ordinary temperatures within human lifetimes, while others have measureable reaction rates (velocities of reaction) to which chemical kinetics and thermodynamics laws can be applied. The nature of the reacting substances, the temperature, and the concentrations of the reactants affect the reaction rates. The reactions can be classified as first order reactions, second order rections, etc. Regardless of the reaction rate or order of the reaction, a reaction rate constant is always present as part of the expression for the reaction rate.

In 1889 Arrhenius suggested the use of the equation (R) which now bears his name as a model to describe empirically derived data showing the variation of the reaction rate constants (and hence the reaction rates) with temperature. Today, semiconductor reliability analysts use the Arrhenius Equation concept to attempt to fingerprint unique failure mechanisms.

$$R = A \exp \frac{-E_a}{kT_K} \text{ where:}$$

- R = reaction rate constant
- A = a constant
- E_a = activation energy (eV). E_a can be pictured as a potential energy hill that must be climbed to reach the activated state.
- k = Boltzmann's constant, 8.63 x 10^{-5}eV/°K
- T_K = absolute temperature (°Kelvin) at the site of the reaction

ACTIVATION ENERGY DETERMINATION

Assuming that E_a is a constant, a plot of log R against the reciprocal of temperature should produce a straight line (e.g., Ra of Figure 13-3) if the Arrhenius equation applies. If a straight line results, the activation energy (E_a) can be readily calculated by taking two available values of R (e.g., Ra_1 and Ra_2) and the corresponding two temperatures and substituting these known values into the derived equation for E_a.

"APPARENT" ACTIVATION ENERGIES

If a singular failure mechanism is thought to exist (e.g., aluminum corrosion), a reliability analyst might try to determine the apparent activation energy of that mechanism by working with degradation or failure times (time to failure). A constant measure of degradation time, such as time to 50% failure, can be plotted on semi-log paper against the reciprocal of the various temperatures at which the several life distribution (i.e., failure distribution) studies were performed. If a straight line (Arrhenius line) results, the apparent activation energy can be determined as indicated earlier with the exception that time, t, is now used instead of R.

This approach assumes that the reaction rate of the failure mechanism (which includes the reaction rate constant) is related to degradation time through some undefined function. But regardless of that function, if the rection rate constant follows an Arrhenius line, then so should the plot of constant degradation time vs. reciprocal temperature. The word "apparent" is used for two reasons. The activation energy of the process by which a failure occurs is not necessarily the same as the apparent activation energy of the process of reaching some end point limit of a parameter as measured by the effect of temperature on the failure distribution. The second reason that "apparent" is used is that several processes may be acting at one time, each with its own activation energy, so as to produce a failure mechanism with an apparent singular activation energy for the set of variables present during that experiment.

ARBITRARY GRAPHS DRAWN TO DEMONSTRATE THE USE OF THE ARRHENIUS EQUATION

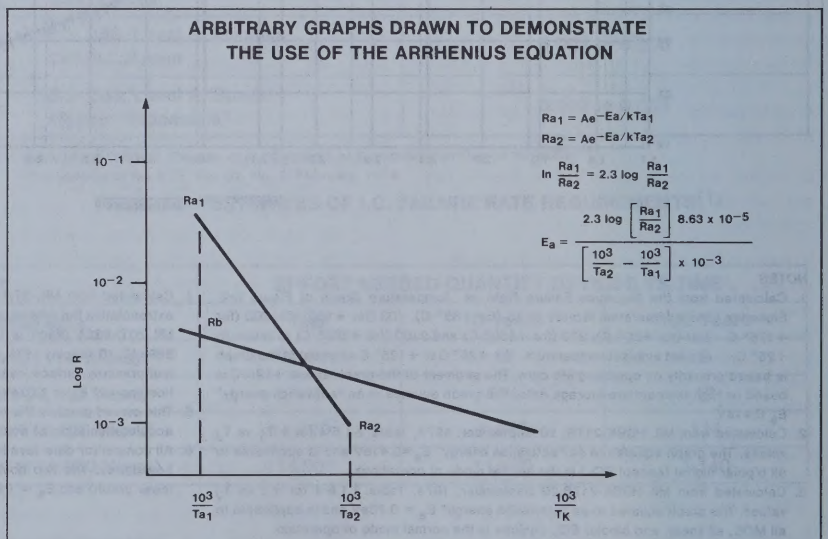


Figure 13-3

Table 13-3 lists a few of the published "apparent" activation energies of failures. Table 13-3 is not an endorsement of these activation energies, but rather an example of some typical values which one might expect.

MECHANISM	E_a(eV)
Surface-Inversion Failures	1.02
Au-Al Bond Failures	1.02-1.04
Metal Penetration Into Silicon	1.77

Table 13-3 PUBLISHED "APPARENT" ACTIVATION ENERGIES OF FAILURES[1]

NOTE

(1) D. S. Peck and C. H. Zierdt, Jr., "The Reliability of Semiconductor Devices in the Bell System," Proceedings of the IEEE, Vol. 62, No. 2, February, 1974.

PSEUDO ACTIVATION ENERGIES

When several failure mechanisms are known to be active at one time and are interacting so as to produce an Arrhenius line, the word pseudo is used for a pseudo activation energy that is beyond the intent of the Arrhenius equation. The "activation energies" calculated from the graphs of Figure 13-2 fall into this category.

Figure 13-3 can be interpreted as showing two degradation mechanisms producing plots Ra and Rb. The resulting plot (Log R) would be the sum of log Ra and log Rb which would be not a straight line. If two or more degradation mechanisms are known to be present, each should be plotted separately to see if each has an Arrhenius line with an associated activation energy. Pseudo activation energies are of questionable technical value as they do not fingerprint specific failure mechanisms.

Log Normal Life Distribution[1,2]

Several distrubtions such as Exponential, Normal, Log-Normal, Chi-Square and Weibull are available as possible models to empirically fit determined stress data. The Log-Normal Distrubtion has been found to be recognizable in life distributions when the population is large enough, when sufficient acceleration is present and when the test is continued long enough to show the complete distribution.[1] Signetics used Log-Normal graph paper in Section 5 for plotting the results of environmental studies of plastic products.

Figure 13-4 is a pictorial representation of how the normalized axis of normal probability paper came about. The variable "X" can be interpreted to mean the amount of time or the number of cycles. The f(X) can be interpreted as number of failures to a given criteria. Graph 1 is the easily recognizable normal distrubtion. Graph 2 shows what happens when the vertical axis is changed from f(X) to accumulative %f(X). Graph 3 shows how normal probability paper produces a straight line out of Graph 2 data. Therefore, that data which produces a straight line when plotted on normal probability paper (Graph 3) is represented by a normal distribution (Graph 1).

Similar analysis of Figure 13-5 will show that data which produces a straight line when plotted on Log-Normal probability paper (①of Graph 3) is represented by a Log-Normal distrubtion (Graph 2) which relates to the skewed distribution of Graph 1 when the horizontal axis is changed from log (X) to X. A straight line on Log-Normal probability paper (i.e., ①of Graph 3) is usually indicative of one failure mechanism. A second line ② is most likely representative of an infant mortality or freak failure mechanism. Failure analysis would need to be performed to identify the mechanisms.

The standard deviation (σ') of the logarithm of time (or cycles) to failure for the log-normal distribution can be estimated as the natural log of time to 50 percent failure minus the natural log of time to 16 percent failure.

NOTES

1. D. Peck, C. H. Zierdt, "The Reliability of Semiconductor Devices in the Bell System", Proceedings of the IEEE, Volume 62, No. 2, February 1974.
2. F. Reynolds, "Termally Accelerated Aging of Semiconductor Components", Proceedings of the IEEE, Volume 62, No. 2, February 1974.

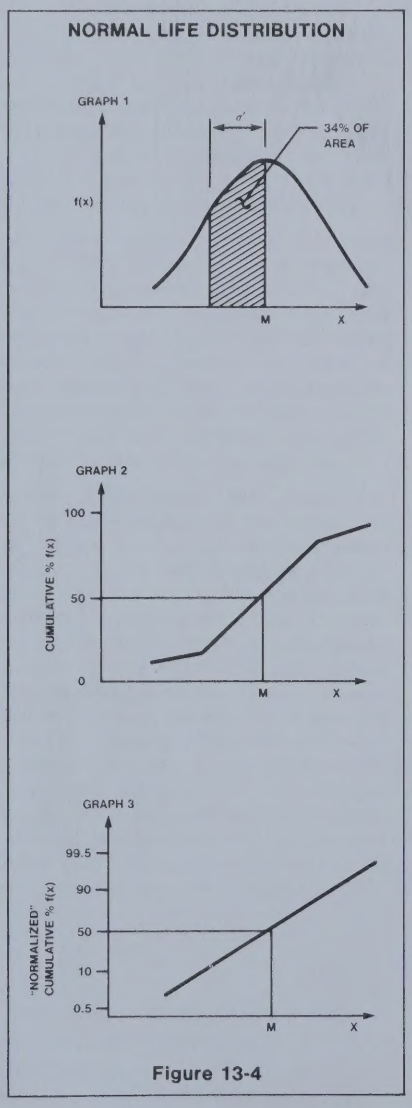


Figure 13-4

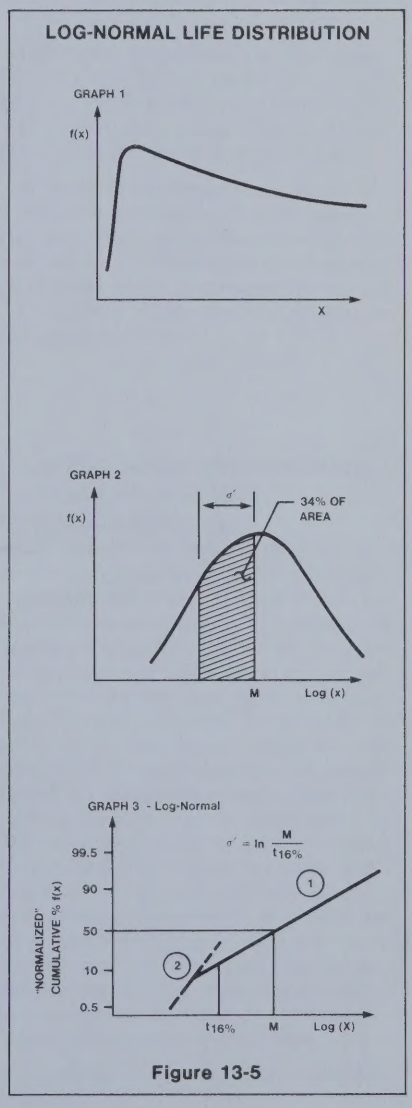
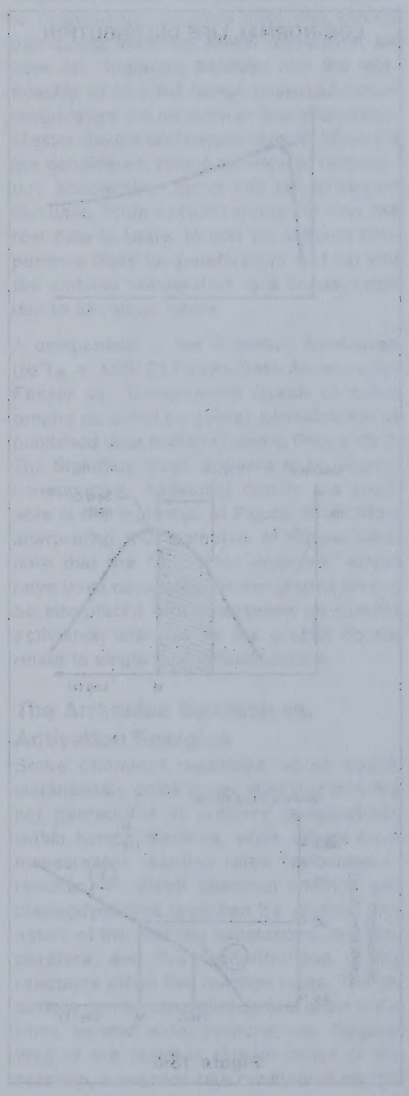
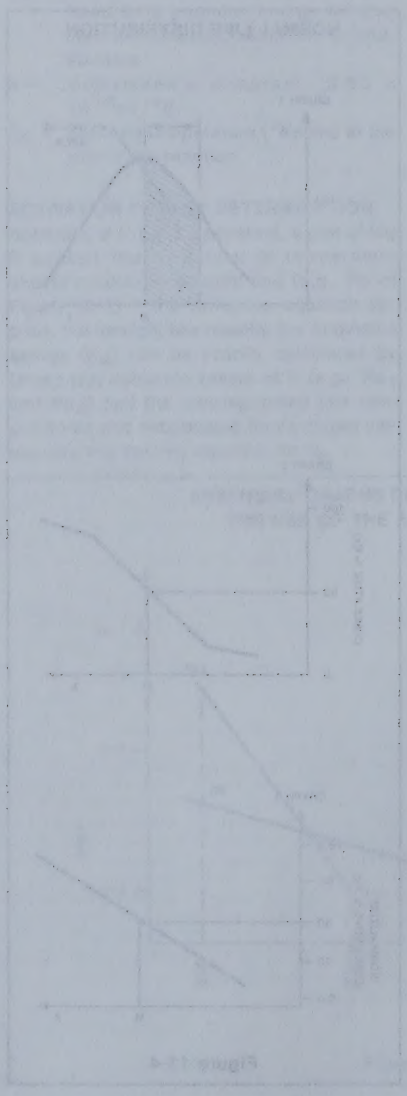


Figure 13-5





PLASTIC MOLDED ICs

PLASTIC ENCAPSULANT CONSIDERATIONS

Signetics has been a manufacturer of plastic integrated circuits for over ten years. During this time Signetics has refined the methods used to characterize potential encapsulants and has become acutely aware of the many variables that exist during integrated circuit manufacturing which can interact with the various encapsulant properties and impact product reliability. This knowledge is crucial, for to characterize an encapsulant by only a few properties, such as glass transition temperature (T_G) by itself, while ignoring the other properties and their interactions is almost a sure way of overlooking potential product reliability problems. Table 14-1 lists the major considerations involved in manufacturing reliable plastic integrated circuits.

Silicones and epoxies have been in common use by I.C. Manufacturers over the years. The considerations delineated in Table 14-1 apply (to varying degrees) to both silicones and epoxies. The general statements that can be made at this time concerning the suitability of silicone versus epoxy for plastic integrated circuit assembly are:

Epoxies can be made with a slightly smaller α_1 linear expansion coefficient. The slightly smaller linear expansion coefficient is more closely matched to the linear expansion coefficients of the leadframe, the bondwires, and the silicon die.

Epoxies out perform silicones during MIL-STD-883A salt atmosphere.

Silicones have slightly fewer "contaminants" than epoxies. Silicones therefore may be potentially better suited for surface state controlled devices (e.g., MOS).

Silicones have higher thermal stability than epoxies. Silicones therefore can withstand higher junction temperatures prior to emitting decomposition byproducts.

The primary constraints placed on plastic molded product applications are:

The junction temperature (T_J) should be limited to 150°C or below.

The formation of gold-aluminum intermetallic compounds, contributing to bond and metalization failures, are highly accelerated at T_J above 150°C.

Bond wire grain growth ("creep") is also accelerated at T_J above 150°C. The grain growth can cause bond wire failures.

14.1.6 Prolonged constant use at high temperature and high humidity conditions can cause parametric instability, aluminum corrosion, and external lead corrosion problems. These problems apply equally to the external surfaces of "hermetic" packaged and to the internal areas of non-plastic packages which lose their "Hermetic seal."

Scope Of Plastic Encapsulant Reliability Data Presented

All plastic encapsulant reliability data of Section 15 is based exclusively on Silicone (in production since 1966) or Epoxy Novolac I encapsulated devices and is labeled accordingly to provide clear interpretation. The Epoxy Novolac I encapsulant system also goes by the name of "Epoxy B." This new family of epoxy molding compounds was introduced in 1972 and offered significant and improved advantages over earlier epoxy systems thereby gaining rapid acceptance as demonstrated by successful qualification of Novolac I encapsulated products for use in all I.C. user appplications (EDP mainframe manufacturers, independent terminal and peripheral equipment manufacturers, mini-computer manufacturers, automotive manufacturers, consumer entertainment, and military applications).

Since the introduction of the Novolac I System in 1972, Signetics has evaluated over 50 additional commercially available or specially formulated encapsulants. None of the reliability data generated on these encapsulants is included in this report. All data obtained from reliability studies of the Novolac I System (Section 15) are being applied as part of the Signetics ongoing program to develop better encapsulants.

Section 15 was written in direct response to the interest expressed by several customers for data relating to the reliability performance of plastic encapsulated products during extended accelerated environmental stresses. The composite results of several key accelerated stresses are presented in Section 15. It is important to note that the data presented in Section 15 is for the most part engineering data which is beyond the scope of standard qualification programs. Signetics has, however, upgraded the SURE Program for 1975 (SURE II is discussed in Section 12) to include some extended environmental testing of plastic products. Most of the data that is presented in Section 15 was generated between 1972 and the start of 1975.

Comparison Of Signetics Plastic vs. "Hermetic" Package Life Test Data

To arrive at a meaningful comparison of plastic to hermetic package life test performance, it is essential that other variables (thermomechanical and humidity) be controlled so as to not have a deciding effect on the outcome. Such is the case in this study. All life test data (Tables 14-2 and 14-3) was generated under steady state temperature conditions and in a relatively dry environment.

Based on Table 14-2, no difference in life test performance between hermetic and plastic package products was observed for data covering all Signetics products from 1971 to 1975.

Based on Table 14-3, no difference in life test performance between hermetic and plastic packaged products was observed for data covering all Signetics products from 1962 to 1970.

Note that any differences that may appear to exist in the plastic to hermetic failure rate radios (0.6X to 2.3X) are considered to be well within the "noise" (scatter/non-repeatability) of generating failure rates.

The results of this comparison are not surprising when one recognizes that Signetics fully qualifies the encapsulant to the die process technology before going into production and that efforts are taken not to exceed T_J = 150°C while life testing plastic packaged products.

Extended Temperature-Humidity Performance of Plastic Encapsulated Products

When interpreting temperature humidity peformance of plastic packaged products, it is essential that one recognize that **accelerated stresses** be obtained for usage as an **engineering tool** in product improvement and process control efforts. To the product user, the data only has significance if, in fact, it relates to real life. (Failures can be obtained from **any** type of stress if a high enough stress level is used.) At the present time, many differences of opinion exist in the industry concerning the applicability of present stress levels to real life failure mechanisms. The problem at hand is the fact that no quick and valid test exists to evaluate the "hermeticity" of plastic devices. As a result, "tools" are used today which formerly were not used even for non-plastic products. The temperature-humidity stresses are used primarily to check for the following three failure mechanisms:

Die Surface related parametric instability problems.

General Corrosion without the presence of external bias. Such corrosion can be related to internal electromotive forces established by dissimilar metal couples or P-N junctions. As an example, the Au-Al couple produces approximately three volts self bias.

Cathodic or anodic oxidation (corrosion) which can occur with external bias applied. The amount of corrosion visible and the rate of corrosion increases with increasing external bias.

PLASTIC ENCAPSULANT CONSIDERATIONS (COMPOSITION, PROPERTIES, PROCESSING)	APPLICABLE RELIABILITY CONSIDERATIONS[1]	POSSIBLE MANUFACTURING INTERACTIONS[2]
I. Chemical Composition 1. Resin (type and hardener) 2. Catalyst 3. Mold release 4. Flame retardant system 5. Filler (type, amount and particle size distribution) II. Chemical-Physical Properties 1. Thermal stability 2. Impurities (ionic conductance and pH of water extract, total halogens, total metallic impurities). III. Thermomechanical Properties 1. Thermal expansion coefficients (α_1, α_2) 2. Glass transition temperature (T_G) IV. Thermal Conductivity V. Mechanical and Electrical Properties 1. Molded material 2. Post cured material VI. Process Conditions Affecting Package Properties 1. Preheating 2. Encapsulant flow characteristics 3. Molding (temperature, time and pressure) 4. Post molding curing (temperature and time) 5. Finish operations (Deflash, cutapart, lead bend, lead diping/plating).	1. Dry environment parametric stability (leakage current, threshold voltage, bond resistance, etc.) a. Evolution of contaminants during molding and cure (mobile ionic impurities, polar organic groups, etc.) b. Post cure thermal degradation of encapsulant 2. Humid environment parametric stability (measure of the encapsulant's ability to resist water absorption by the bulk material or moisture ingression along the leadframe/bond wire/encapsulant interfaces) a. Electrolytic metal (usually aluminum) corrosion b. Leach of contaminants producing "extended gate" affect, conductive glass, depletion/inversion or accumulation of silicon surface c. Decrease in encapsulant electrical resistance 3. Effect of thermomechanical stress of encapsulant on the bond/bond wire system (room, "window," and hot opens or shorts) a. Wire grain growth ("creep") b. Decrease in bond strength c. Wire to wire shorts ("wire sweep" related) d. Wire to die shorts 4. Flammability	1. Die process technology (sensitivity to contaminants and corrosion) a. Gold doped bipolar digital b. Non-gold doped bipolar digital c. Bipolar linear d. NMOS, PMOS, DMOS, CMOS 2. Glass integrity a. Porosity b. Phosphorous leach c. Gettering ability 3. Metal Integrity a. Retarding effect of oxidized metal on metal corrosion b. Grain size, etc. 4. Bond integrity factors of Table 1-2 paragraph II.C. 5. Lead frame a. Material b. Plating

NOTES

1. Typical Signetics reliability "tools" include:
   a. HTOL or HTRB (+85°C or +125°C) and HTSL (+150°C) to evaluate the electrical compatibility of the encapsulating material in a dry environment.
   b. Temperature humidity stresses (+85°C and 85% R.H., +121°C and 100% R.H., cyclic +25°C to +65°C with 80 to 98% R.H.) with or without electrical bias.
   c. Power cycle (P_D max and either a 5 minute or a 10 minute cycle), temperature cycle (0°C to +125°C, −55°C to +125°C, −65°C to +150°C), and thermal shock (0°C to +100°C, −55°C to +125°C, −65°C to +150°C).
2. Refer to Table 1-2 for a more comprehensive coverage of "manufacturing" factors.

Table 14-1 ENCAPSULANT vs. RELIABILITY vs. "MANUFACTURING" CONSIDERATIONS

Data Sort Routine	Life Test Data	SUMMARY of ACTUAL LIFE TEST DATA: 300°C High Temp. Storage Life — Device Hours	# Failures Cat	# Failures Deg	150°C High Temp. Storage Life — Device Hours	# Failures Cat	# Failures Deg	125°C Ambient High Temp. Operating Life — Device Hours	# Failures Cat	# Failures Deg	85°C Ambient High Temp. Operating Life — Device Hours	# Failures Cat	# Failures Deg	55°C to 25°C Ambient Operating Life — Device Hours	# Failures Cat	# Failures Deg	Total # of "Lots" Tested	Total # of Devices Tested	Combined (HTOL & HTSL) 25°C Equivalent (1) — Device Hours	# Failures Cat	# Failures Deg
Bipolar Technologies (DTL, ECL, TTL, Linear, PROMS, TTL Schottky, Low Pwr TTL-S)	"Hermetic"	95,500	2	0	5,336,500	3	2	5,890,000	8	8	-	-	-	-	-	-	192	8,641	1,028,700,000	13	10
	Plastic (Epoxy Novolac)	-	-	-	2,648,000	2	1	3,296,480	4	0	235,120	1	0	4,290,320	1	0	98	5,371	437,441,120	8	1
	Plastic (Silicone)	-	-	-	1,232,000	3	3	1,813,880	0	0	-	-	-	39,000	0	0	42	2,596	213,933,000	3	3
MOS Technologies (CMOS, DMOS, NMOS, PMOS)	"Hermetic"	-	-	-	613,000	1	1	754,000	0	0	624,000	2	2	97,000	1	0	30	1,488	108,457,000	4	3
	Plastic (Pre-Production)	-	-	-	172,000	0	0	61,000	0	3	146,000	0	0	37,000	0	1	10	366	22,477,000	0	4
	Plastic (Silicone)	-	-	-	841,728	4	0	255,000	2	1	1,023,358	5	3	33,000	0	0	36	1,643	112,306,170	11	4
	Total	95,500	2	0	10,843,228	13	7	12,070,360	14	12	2,028,478	8	5	4,496,320	2	1	408	20,105	1,923,314,290	39	25

Data Sort Routine	Life Test Data and Failure Rates	Combined (HTOL & HTSL) 25°C Equivalent (1) — Device Hours	# Failures Cat	# Failures Deg	Failure Rates in %/1000 Hours @ 60% Confidence — Catastrophic λ	Catastrophic (2)	Cat + Deg λ	Cat + Deg (2)
Bipolar Technologies (DTL, ECL, TTL, Linear, PROMS, TTL Schottky, Low Pwr TTL-S)	"Hermetic"	1,028,700,000	13	10	0.0014	1X	0.0024	1X
	Plastic (Epoxy Novolac)	437,441,120	8	1	0.0021	1.5X	0.0024	1X
	Plastic (Silicone)	213,933,000	3	3	0.00195	1.4X	0.0034	1.4X
MOS Technologies (CMOS, DMOS NMOS, PMOS)	"Hermetic"	109,457,000	4	3	0.0047	1X	0.0076	1X
	Plastic (Pre-Production)	22,477,000	0	4	0.0041	0.9X	0.023	3.0X
	Plastic (Silicone)	112,306,170	11	4	0.011	2.3X	0.015	2.0X
	Total	1,923,314,290	39	25				

NOTES:
1. The Signetics Failure Rate Acceleration Factor vs. Temperature Graph (Figure 13-2) was used for these calculations (1X used for 25°C and below).
2. λ arbitrrily normalized to the "hermetic" group of each technology for ease of comparison.

Table 14-2 COMPARISON of PLASTIC vs. "HERMETIC" PACKAGE LIFE TEST PERFORMANCE 1971 to 1975

STRESS		PACKAGE	"ACTUAL" DEVICE HOURS	CAT PLUS DEG FAILURES	λ @ 60% CONFIDENCE IN %/1000 HOURS	PLASTIC/ HERMETIC λ RATIO
HTSL	150°C	Plastic Hermetic	5.6M 8.3M	9 20	0.18 0.25	0.7X
HTOL	125°C	Plastic Hermetic	7.3M 29.2M	6 42	0.089 0.155	0.6X
HTOL	85°C	Plastic Hermetic	2.3M 3.4M	0 0	0.039 0.026	1.5X
HTOL (RTE)	25°C	Plastic Hermetic	136M 319M	1 2	0.00145 0.00098	1.5X

Table 14-3 COMPARISON of PLASTIC vs. "HERMETIC" PACKAGE LIFE TEST PERFORMANCE 1962 to 1970

Figure 14-1 shows the average cumulative percent failures versus time for biased temperature-humidity (BTH) stressing at 85°C and 85% R.H.

Considering the uncertainty in the data presented, the following general statements appear appropriate. (The reader is urged to study the data and form his own conclusions.)

Bipolar products encapsulated in Silicone or Epoxy Novolac I appear to have 0.6 to 1.7% average failures after 1,000 hours.

MOS products in Silicone appear to have 8 to 10% average failure after 1,000 hours. Surface sensitivity and higher stress voltages may have contributed to this failure level. Limited data exists.

Non-Hermetic Non-Plastic aproducts can be made to fail at similar percent failure levels after 1,000 hours. Cerdip (ceramic packages with glass seals at the lead frame) products with defective seals were used in this study.

Competitor MOS products (based on complementary MOS data) appear to have 44 to 55% average failures (prior to any failure analysis) after 1,000 hours when tested to the Signetics conditions. In addition, during 1975 Competitor B published that his CMOS products have 5% cumulative failures at 1,500 hours. Compleitor B also stated that his four CMOS competitors have from 20% to 70% cumulative failures at 1,000 hours. Competitor C stated that his CMOS products have 2.5% failures at 1,500 hours and CMOS Competitor D stated that his products have 50% cumulative failures at 2,000 hours. This information is presented so that a gauge exists by which to judge future MOS plastic product performance during biased 85°C/85% RH accelerated stressing and also to point out that "typical" cumulative pecent failure graphs may not be related to lot-to-lot variance during the BTH 85/85 test.

Several articles have been written describing acceleration factors between 85°C/85% RH stress levels and stress levels more closely in line with typical applications. One of the more recent articles (and apparently most technical approach) is one written by D. S. Peck and C. H. Zierdt, Jr., "The Reliability of Semiconductor Devices In The Bell System" which appeared in the Proceedings of the IEEE, Volume 62, No. 2, February 1974. In that article acceleration factors for the junction temperature (T_J) and the %RH at the die surface were determined for biased 85°C/85% RH stressing. The device life versus T_J relationship was found to be independent of relative humidity for %RH above 10% at the die surface. Likewise, the device life versus %RH at the die surface relationship was found to be independent of temperature for at least $50°C \leq T_J \leq 150°C$. Using the acceleration factor graphs of Figures 25, 26 and 27 of that article, an acceleration factor of greater than 1.4×10^5 exists between biased 85°C/85% RH and "real life" biased 25°C/50% RH conditions. For these calculations, a T_J = 40°C was assumed for the 25°C ambient condition which related to 10% RH at the die surface for the external 50% RH conditions. Using the calculated acceleration factor, 10% failures at 1,000 hours of biased 85°C/85% RH relates to 10% failures after 10^8 hours (i.e., 1.1×10^4 years) at biased 25°C/50% RH.

Figure 14-2 shows the average cumulative percent failures versus time for 30 PSIA (15 PSIG), 121°C, Pressure Cooker (Steam). The following general statements appear appropriate:

Bipolar products in Epoxy Novolac I appear to have 2.3% average failures after 96 hours. Not shown in Figure 14-2 is bipolar Silicone performance. There are indications that bipolar Silicone meets or exceeds Epoxy Novolac I performance during 96 hours. This statement is based on the test results of eight lots totalling 808 bipolar Silicone devices which completed 144 hours at 30 PSIA, 121°C with 1.3% functional test failures. Of the 1.3% rejects, 20% were due to corrosion of the aluminum. The Silicone data was reported in June 1975 (Status Report from the Plastic I.C. Assembly Plant) and has not as yet been formally analyzed and documented for reference purposes.

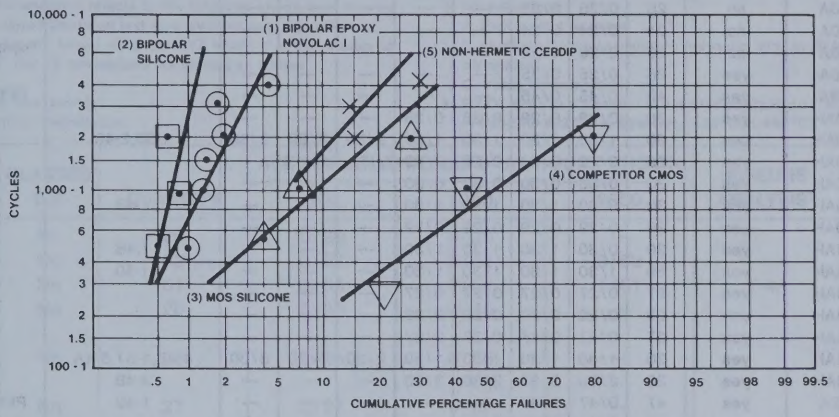
MOS in Silicone appears to have an average of 11% failures after 96 hours. However, none of the failures were failure analyzed to legitimatize the percent failures observed.

Competitor bipolar product appears to be at 35% average failures at 96 hours and competitor CMOS appears to be at 30% average failures at 96 hours based on data generated at Signetics from 1972 to 1974. This information was included to show that Signetics top competitors can also have significant failure levels during this test. This data is not intended to imply that all Signetics competitors are always experiencing these failure levels.

Signetics has not found a relationship between extended pressure cooker performance (i.e., test beyond 24 hours) and real life failures. Thus, the 96 hour results reported above are presented for information purposes only.

Pressure cooker tests of eight to 24 hours appear to be adequate for producing failures in those devices having body cracks and separations in the interface between encapsulant and lead frame. Table 14-12 shows that throughout 1974 no major problems were observed with encapsulant lead frame integrity during eight hours of pressure cooker and 52 consecutive weeks of monitoring Epoxy Novolac I assembly. The results of monitoring Silicone assembly in 1974 are not reported due to the fact that test equipment at the assembly plant did not allow for MOS functional testing (only bond continuity testing). However, an idea of MOS Silicone performance during eight hours of pressure cooker can be obtained from Table 14-10.

A COMPARISON OF AVERAGE CUMULATIVE % FAILURES VS. TIME FOR BIASED TEMPERATURE-HUMIDITY STRESS (85°C, 85% R.H.)


(1) BIPOLAR EPOXY NOVOLAC I
(2) BIPOLAR SILICONE
(3) MOS SILICONE
(4) COMPETITOR CMOS
(5) NON-HERMETIC CERDIP
CYCLES
10,000 - 1
1,000 - 1
100 - 1
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
CUMULATIVE PERCENTAGE FAILURES

NOTES

1. The graph for Signetics Bipolar Products in epoxy novolac is based on the data from Table 14-4. The graph to the 2000 hour timepoint is based on the samples progressing to 2000 hours. The 3000 and 4000 hour points represent a substantially reduced sample size.
2. The graph for Signetics Bipolar Products in silicone is based on the data from Tabe 14-5. The 2000 hour data point (reduced sample size) is depicted for reference only.
3. The graph for Signetics MOS Products in silicone is based on the data from Table 14-6. The 2000 hour data point is probably non-typical of average performance due to the limited amount of data available and lack of failure analysis.
4. The average performance of six Signetics CMOS competitors is based on the data of Table 14-7. The graph could be non-typical due to the lack of failure analysis.
5. This graph serves as a reminder that non-plastic devices (e.g. "hermetic" devices which may lose hermeticity during board insertion, etc.) can also be subject to aluminum corrosion during this stress. Parallel with test DT74113 of Table 14-4, a sample of 39 each 7400FH (CERDIP) devices were assembled on an engineering line to act as "controls". Approximately half of the parts were built to exhibit fine or gross leaks at 0 hours. Consequently, results of +85 C/85% R.H. stress showed electrical failures as follows

	Timepoint				
Cumulative Failures	0	1000	2000	3000	4000
	0/39	0/39	6/39*	7/39[8]	12/39

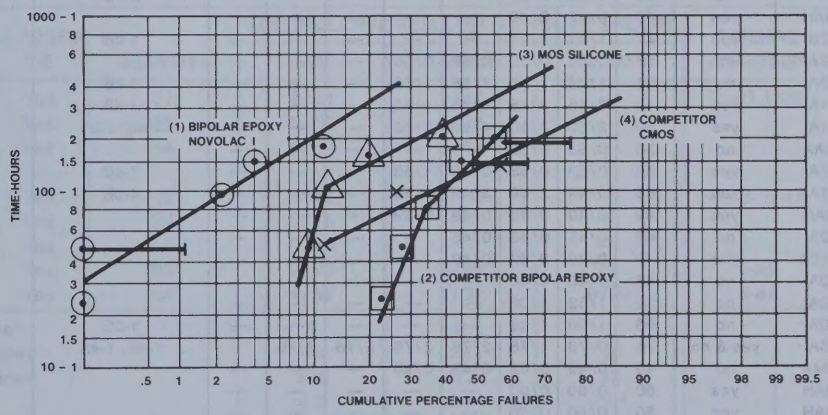
*At corrosion, failed dye penetrant

Additionally, at 4000 hours, the remaining 27 "good" devices exhibited 12 fine and zero gross leaks

6. A logarithm of time-to-failure versus a normal probability scale was chosen for these plots so that straight lines (when they develop) would represent a log-normal failure distribution. For log-normal distribution, median life corresponds to t(50%) and the standard to ln [t(50%)/t(16%)]

Figure 14-1

A COMPARISON OF AVERAGE CUMULATIVE % FAILURES VS. TIME FOR 30psia, 121°C, PRESSURE COOKER (STEAM).


(1) BIPOLAR EPOXY NOVOLAC I
(2) COMPETITOR BIPOLAR EPOXY
(3) MOS SILICONE
(4) COMPETITOR CMOS
TIME-HOURS
1000 - 1
100 - 1
10 - 1
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
CUMULATIVE PERCENTAGE FAILURES

NOTES

1. The graph for Signetics Bipolar Products in epoxy novolac is based on the data from 14-8 and includes only those samples which completed 192 hours.
2. The average performance of competitor bipolar products in epoxy is based on the data of Table 14-9 and a sample size of 203 through 192 hours
3. The graph for Signetics MOS Products in silicone is based on the data of Table 14-10. The graph could be non-typical of average performance due to the lack of failure analysis. Sample size of 106 used for all data points.
4. The average performance of six Signetics CMOS competitors is based on the data of Tables 14--11. The graph could be non typical of average performance due to the lack of failure analysis.
5. A logarithm of time to failure versus a normal probability scale was chosen for these plots so that straight lines (when they develop, median life corresponds to t(50%) and the standard deviation to ln (t[50%0/t16%)].

Figure 14-2

TEST NUMBER	DEVICE	GLASS'D DIE?	QTY	ACCUMULATIVE RESULT[2] AT HOURS SHOWN 500	1000	1500	2000	3000	4000	5000	FAILURE ANALYSIS[3]	COMMENTS
DT72092	7400AH	yes	41	0/41	0/41	—	—	—	—	—		
DT72095	7400A	no	25	0/25	0/25	—	—	—	—	—		PPIP, R338
DT72098	7400A	no	24	0/24	0/24	—	—	—	—	—		PPIP,R336
DT72098	7400A	no	26	0/26	0/26	—	—	—	—	—		PPIP,R336, *PER M.S. 883
DT72101	7400A	yes	25	0/25	0/25	—	—	—	—	—		PPIP, R336
DT72164	5748A	yes	45	0/45	0/45	—	—	—	—	—		PPIP, R336, PER M.S. 883
DT73011	7400AH	yes	28	0/28	0/28	0/28	0/28	—	—	—		R242
DT73012	7400AH	yes	30	1/30	1/30	1/30	1/30	2/30	3/30	3/30	1-30,2-48	R242
DT73013	7400AH	yes	29	0/29	0/29	0/29	0/29	—	—	—		R242
DT73014	7400AH	yes	30	0/30	0/30	0/30	0/30	—	—	—		R242
DT73015	7400AH	yes	30	0/30	1/30	1/30	1/30	—	—	—	1.48	R242
DT73016	7400AH	yes	29	0/29	0/29	0/29	0/29	—	—	—		R242
DT73017	7404AH	yes	30	0/30	1/30	1/30	1/30	—	—	—	1.4B	R242
DT73018	7404AH	yes	30	1/30	1/30	1/30	1/30	—	—	—	1-30	R242
DT73019	7404AH	yes	27	0/27	0/27	0/27	0/27	—	—	—		R242
DT73020	7404AH	yes	29	0/29	0/29	0/29	0/29	—	—	—		R242
DT73021	7404AH	yes	27	0/27	0/27	0/27	0/27	—	—	—		R242
DT73022	7404AH	yes	30	1/30	1/30	1/30	1/30	2/30	6/30	8/30	4-48,1-31,3-4A	R242
DT73023	7404AH	yes	30	2/30	3/30	3/30	3/30	—	—	—	3-4B	R242
DT73047	5748A	yes	47	0/47	1/47	—	—	—	—	—	1-4B	PPIP, R336, PER M.S. 883
DT73048	5748A	yes	45	0/45	0/45	0/45	—	—	—	—		PPIP, R336
DT73061	7400AH	yes	50	0/50	0/50	—	—	—	—	—		R101
DT73071	7404A	no	47	1/47	2/47	—	—	—	—	—	1-31, 1-4C	R067
DT73038	7408A	no	25	1/25	5/25	—	—	—	—	—	5-4B	R067
DT72178	7404AH	yes	45	0/45	0/45	—	—	—	—	—		R082, PER M.S. 883
DT72179	7404AH	yes	45	0/45	0/45	—	—	—	—	—		R082, PER M.S. 883
DT72197	7404AH	yes	19	1/19	1/19	—	—	—	—	—	1-4B	RO82
DT72198	7404AH	yes	19	0/19	0/19	—	—	—	—	—		RO82
DT73079	7404AH	yes	24	1/24	1/24	—	—	—	—	—	1-2A	R101
DT73089	7410AH	yes	23	0/23	0/23	—	—	—	—	—		R125
DT73093	7410AH	yes	24	0/24	0/24	—	—	—	—	—		R125
DT73096	7410AH	yes	23	0/23	0/23	—	—	—	—	—		R125
DT73099	7403AH	yes	23	0/23	0/23	—	—	—	—	—		R125
DT73100	7400AH	yes	25	0/25	3/25	—	—	—	—	—	3-4B	R125
DT73106	7400AH	yes	24	0/24	0/24	—	—	—	—	—		R125
DT73108	7403AH	yes	24	0/24	5/24	—	—	—	—	—	5-4B	R125
DT73104	7400A	yes	45	0/45	0/45	—	—	—	—	—		R338
DT73105	7400A	yes	49	0/49	0/49	—	—	—	—	—		R338
Customer A	7400A	yes	150	0/150	0/150	0/150	0/150	3/150	3/150	—		
Customer A	7400A	yes	148	0/148	0/148	0/148	0/148	0/148	—	—		85°C/60% R.H.
DT73111	7404A	no	85	1/85	2/85	—	—	—	—	—	2-4B	
DT73112	7404A	no	85	5/85	8/85	—	—	—	—	—	8-4B	
DT73116	7400AH	yes	40	0/40	0/40	—	—	—	—	—		
DT73118	7442B	yes	41	1/41	1/41	—	—	—	—	—	1-4B	
DT73127	7402A	no	56	0/56	0/56	0/56	0/56	—	—	—		R284, PEEP
DT73128	7402A	no	56	1/56	1/56	1/56	1/56	—	—	—	1-4B	R284, PEEP
DT73136	5741A	yes	45	2/45	2/45	4/45	4/45	—	—	—	4-48	R334, PEEP
DT73137	5741A	yes	50	2/50	3/50	4/50	5/50	—	—	—	4-48, 1-2E	R334, PEEP
DT73151	7402AA	no	33	0/33	0/33	—	—	—	—	—		R269
DT73152	5741A	yes	53	0/53	0/53	0/53	1/53	—	—	—	1-4B	R334
DT73162	5741A	yes	49	0/49	2/49	3/49	4/49	—	—	—	4-4B	
DT74001	7400AH	yes	49	0/49	0/49	0/49	0/49	—	—	—		
DT74007	7400A	no	45	0/45	0/45	0/45	—	—	—	—		R280
DT74048	10171BA	yes	49	0/49	0/49	0/49	—	—	—	—		
DT74063	7400A	no	48	0/48	0/48	—	—	—	—	—		R345, DEQP
Customer B	7400A	no	32	1/32	1/32	—	—	—	—	—		90°C, 85% R.H.
DT74071	7400A	no	96	1/96	1/96	—	—	—	—	—	1-2E	R311
DT74080	7406A	yes & no	76	0/76	1/76	2/76	2/76	2/76	2/76		1-4B, 1-4A	IN PROCESS
DT74094	74SO4A	no	49	0/49	0/49	0/49	0/49	—	—	—		R298
DT74036	7400AH	yes	50	0/50	0/50	—	—	—	—	—		R291
DT74037	7400AH	yes	50	0/50	0/50	—	—	—	—	—		R291
DT74113	7400A	yes	100	0/100	0/100	0/100	1/100	1/100	3/100	—	1-4B, 2-4A	IN PROCESS
DT75005	7400A	no	50	0/50	0/50	0/50	0/50					IN PROCESS
		Total = "Lots"		63	63	29	26	6	5	2		
		Total = Failures		23	48	22	26	10	17	11		
		Total = Devices		2776	2776	1449	1310	534	386	60		
(Notes on following page)		% Failures		08	17	15	20	19	4.4	18		

Table 14-4 EPOXY NOVOLAC I ENCAPSULATED BIPOLAR PRODUCTS VS. BIASED[1] TEMPERATURE HUMIDITY (1972 TO 1975)

Notes to Table 14-4

1. Unless otherwise noted in the comments column, all products were stressed at +85°C and 85% relative humidity. All digital products were based at 5 volts, all linear products at +15 volts
2. The results are listed as accumulative rejects to the timepoint shown over starting sample size. All devices received functional test as a minimum pass/fail criterion.
3. The results of failure analysis are shown via code X-YZ where X is the quantity of failures with mechanism YZ. The YZ mechanisms are defined as follows
   2. Die Problems
      A. Oxide Defects (shorts, pits, voids)
      E. Cause Unknown, Electrical Degradation.
   3. Assembly and Package Problems
      G. External Lead Broken
      I. Pitted Leads/Lead Corrosion
   4. Miscellaneous
      A. Failures Not Analyzed
      B. Aluminum Corrosion (moisture ingression, etc., could be die fab, package, or assembly related)
      C. Visual Contamination
4. RXXX refers to a Signetics Internal Reliability Report. M.S. 883 refers to Method 1004 of MIL-STD-883 (80 to 98% R.H., +25°C to +65°C).

TEST NUMBER	DEVICE	GLASSED DIE	QUANTITY	ACCUMULATIVE RESULTS[2] AT HOURS SHOWN			FAILURE ANALYSIS[3]	COMMENTS[4]
				500	1000	2000		
DT71077	8855A	No	20	0/20	0/20	—		R338
DT72068	7400A	No	52	0/52	0/52	0/52		R338, per M.S. 883
DT72069	7400A	No	51	0/51	1/51	1/51	1-4A	R338
DT72094	7400A	No	25	0/25	0/25	—		PPIP, R336, per M.S. 883
DT72096	7400A	No	25	0/25	0/25	—		PPIP, R336, per M.S. 883
DT72097	7400A	No	27	0/27	0/27	—		PPIP, R336, per M.S. 883
DT72097	7400A	No	25	0/25	0/25	—		PPIP, R336
DT72099	7400A	No	26	1/26	1/26	—	1-4B	PPIP, R336, per M.S. 883
DT72099	7400A	No	25	0/25	0/25	—		PPIP, R336
DT72100	7400A	Yes	24	0/24	0/24	—		PPIP, R336
DT72107	5723A	Yes	22	0/22	0/22	—		PPIP, R336
DT72108	5723A	Yes	22	2/22	2/22	—	1-4B, 1-2E	PPIP, R336
DT72163	5748A	Yes	44	0/44	0/44	—		PPIP, R336 per M.S. 883
DT72163	5748A	Yes	48	0/48	0/48	—		PPIP, R336
DT73153	5741A	Yes	52	0/52	0/52	0/52		PEEP, R334
	Total # "Lots"			15	15	3		
	Total # Failures			3	4	1		
	Total # Devices			488	488	155		
	% Failures			0.6	0.8	0.6		

Table 14-5 SILICONE ENCAPSULATED BIPOLAR PRODUCTS VS. BIASED[1] Temperature Humidity (1971 to 1973)

TEST NUMBER	DEVICE	GLASSED DIE	QUANTITY	ACCUMULATIVE RESULTS[2] AT HOURS SHOWN			FAILURE ANALYSIS[3]	COMMENTS[4]
				500	1000	2000		
DT72105	2518B	Yes	31	2/31	2/31	—	1-4D, 1-2E	PPIP,R074,R336
DT72106	2518B	Yes	25	0/25	0/25	—		PPIP, R074,R336
DT72149	2501A	Yes	44	0/44	0/44	—		PPIP, R336, per M.S. 883
DT73141	2518B	Yes	42	8/42	13/42	—	8-4B, 5-4A	PEEP, R335
DT72110	1103XA	Yes	25	0/25	—	—		R338
DT72111	1103XA	Yes	10	0/10	—	—		R338
DT74089	4002A	Yes	99	2/99	3/99	—	3-4B	R350
DT74104	4001A	Yes	32	1/32	4/32	9/32	9-4A	R356
	Total # "Lots"			8	6	1		
	Total # Failures			13	22	9		
	Total # Devices			308	273	32		
	%Failures			4.2	8.1	28.1		

NOTES:

1. Unless otherwise noted in the comments column, all devices were stressed at +85°C and 85% relative humidity. The bipolar digital products were biased at 5 volts, the linear at ± 15 volts, the CMOS at 15 volts and the PMOS at 17 volts
2. The results are listed as accumulative rejects to the timepoint shown over starting sample size. All devices received functional test as a niminum pass/fail criterion.
3. The results of failure analysis are shown via code X-YZ where X is the quantity of failures with mechanism YZ. The YZ mechanisms are defined as follows:
   2. Die Problems
      E. Cause Unknown, Electrical Degradation
   4. Miscellaneous
      A. Failures Not Analyzed
      B. Aluminum Corrosion (moisture ingression, etc., could be die fab, package, or assembly related)
      D. Destroyed during F/A. Cause unknown
4. RXXX refers to a Signetics internal reliability report. M.S. 883 refers to method 1004 of MIL-STD-833 (80 to 98% R.H., +25°C to +65°C).

Table 14-6 SILICONE ENCAPSULATED MOS PRODUCTS VS. BIASED 1 TEMPERATURE HUMIDITY (1974 TO 1974)

TEST NUMBER	DEVICE	GLASSED DIE	QUANTITY	ACCUMULATIVE RESULTS[2] AT HOURS SHOWN			FAILURE ANALYSIS[3]	COMMENTS[4]
				500	1000	2000		
DT74104	A	7411	31	6/31	15/31	31/31	31-4A	R356, epoxy novolac
DT74104	B	7402	32	12/32	25/32	30/32	30-4A	R356, epoxy novolac
DT74104	C	7415	32	1/32	5/32	17/32	17-4A	R356, epoxy novolac
DT74104	D	7413	30	5/30	14/30	24/30	24-4A	R356, epoxy novolac
DT74104	E	7333	29	10/29	15/29	27/29	27-4A	R356, epoxy novolac
DT74104	F	7349	28	3/28	6/25	16/22	16-4A	R356, Silicone
Total # "Lots"				6	6	6		
Total # Failures				37	80	145		
Total # Devices				182	182	182		
% Failures				20.3	44.0	79.7		

NOTES:
1. Unless otherwise noted in the comments column, all devices were stressed at +85°C and 85% relative humidity. The bipolar digital products were biased at 5 volts, the linear at ±15 volts, the CMOS at 15 volts and the PMOS at 17 volts
2. The results are listed as accumulative rejects to the timepoint shown over starting sample size. All devices received functional test as a niminum pass/fail criterion.
3. The results of failure analysis are shown via code X-YZ where X is the quantity of failures with mechanism YZ. The YZ mechanisms are defined as follows:
   2. Die Problems
   E. Cause Unknown, Electrical Degradation
4. Miscellaneous
   A. Failures Not Analyzed
   B. Aluminum Corrosion (moisture ingression, etc., could be die fab, package, or assembly related)
   D. Destroyed during F/A. Cause unknown
4. RXXX refers to a Signetics internal reliability report. M.S. 883 refers to method 1004 of MIL-STD-833 (80 to 98% R.H., +25°C to +65°C).

Table 14-7 SIX CMOS COMPETITORS (4001A EQUIVALENT PRODUCTS) VS. BIASED 1 Temperature Humidity

The exact significance of text results beyond 24 hours is somewhat dubious when related to the knowledge that:

(a) Plastics (silicones and epoxies) saturate with moisture within 24 to 200 hours (typically 100 hours) at 121°C and 30 PSIA as determined by weight gain studies.

(b) Plastics will dry out once removed from the hostile environment (i.e., in real life plastics will most likely not saturate as heat at the die tends to drive out moisture).

(c) Many factors associated with I.C. manufacturing can contribute to the non-repeatability and scatter of test results once absorbed moisture reaches the die surface.

(d) There does not appear to be a known relationship between extended pressure cooker performance and real life. As an example, test DT75004 (worst results experienced) of Table 14-8 had 40% failures by 96 hours and 100% failures by 192 hours. Samples from the same lot (Test DT75005 of Table 5-4) have reached 2,000 hours of biased 85°C/85% RH with zero rejects.

Extended Thermomechanical Performance of Plastic Encapsulated Product

Power Cycle, temperature cycle and thermal shock are the primary reliability stresses used to judge the thermomechanical integrity of the encapsulant to bond wire/die/lead frame system. In actuality, the primary reliability concern is open or intermittent bonds or wires. Other possible problem areas such as cracked die, cracked packages, die metallization microcracks, etc., occur so seldom that they are totally inconsequential in comparison to bond/bond wire problems occurring during extended cyclic thermal stresses. Unless otherwise noted, thermal scan continuity testing (each and every bond wire is tested for continuity over the temperature range of 25°C to ≥ 125°C) was used as a minimum reject criterion for all data pertaining to extended cyclic thermal stresses.

TEST NUMBER	DEVICE	QTY	ACCUMULATIVE RESULTS[1] AT HOURS SHOWN								FAILURE ANALYSIS[2]	COMMENTS[3]
			8	24	48	96	144	192	240	288		
DT72160	5748A	96	0/96	0/96	0/96	-	-	-	-	-	-	PPIP, R336
DT73048	5748A	50	0/50	0/50	0/50	-	-	-	-	-	-	PPIP, R336
DT74049	10171BA	50	-	0/50	0/50	0/50	-	-	-	-	-	R269
DT74062	7400A	49	-	-	0/49	0/49	2/49	7/49	8/49	17/49	≈17-48	DEQP, R345
DT74073	7404A	49	-	-	0/49	0/49	1/49	2/49	5/49	11/49	11-4B	R331
DT74114	7400A	140	-	-	1/140	2/140	5/140	6/140	7/140	14/140	1-4B, 13-4A	Glass Study
DT75004	7400A	50	-	-	-	20/50	-	50/50	-	-	10-4B, 40-4A	CEQP, R352
-	MIX	17,550	6/17,550	-	-	-	-	-	-	-	6-4B	1974 P.M., R329, (4)
Customer B	7400A	32	-	-	0/32	1/32	2/32	7/32	16/32	-	?	
-	MIX	4,116	-	-	-	-	574/4116	-	-	-	≈ALL-4B	1975 P.M., R357, (5)
-	MIX	200	0/200	0/200	0/200	7/200	10/200	23/200	-	66/200	≈ALL-4B	Pre-shipment (6)
-	MIX	600	0/600	0/600	0/600	0/600	6/600	9/600	-	32/600	≈ALL-4B	Glass Study (7)
-	MIX	578	-	-	1/578	10/578	36/578	131/578	-	-	≈ALL-4B	Deflash Study (8)
	Total=Failures		6	0	2	40	636	235	36	140		
	Total=Devices		19,496	996	1844	1748	5764	1698	270	1038		
	% Failures		0.30	0	0.11	2.3	11.0	13.8	13.3	13.5		

Table 14-8 EPOXY NOVALAC I ENCAPSULATED BIPOLAR PRODUCTS VS. 30PSIA, 121°C, PRESSURE COOKER (STEAM) 1972 to 1975

TEST NUMBER	COMPETITOR	DATE CODE	PRODUCT	QTY	ACCUMULATIVE RESULTS[1] AT HOURS SHOWN					FAILURE ANALYSIS[2]	COMMENTS[3]
					24	48	80	144	192		
DT73076	G	7215	7406A EQUIV.	22	15/22	-	-	-	-	15-4A	R206
DT73074	C	7239	7400A EQUIV.	20	0/20	0/20	3/20	-	-	3-4A	R206
DT73125	C	7247	5741A EQUIV.	23	3/23	12/23	18/23	-	-	6-4B, 8-4A	R206
DT73124	G	7319	5741A EQUIV.	22	22/22	-	-	-	-	3-4B, 19-4A	R206
DT73126	B	7318	5741A EQUIV.	21	8/21	8/21	9/21	-	-	8-2E, 1-4A	R206
DT74072	G	7414	7400A EQUIV.	48	-	0/48	1/48	23/48	47/48	47-4B	R331
DT74074	C	7415	7400A EQUIV.	47	-	0/47	0/47	1/47	1/47	1-4B	R331
			Total=Failures		48	20	31	24	48		
			Total=Devices		108	159	159	95	95		
			% Failures		44.4	12.6	19.5	25.3	50.5		

Table 14-9 COMPETITOR BIPOLAR PRODUCTS IN EPOXY VS. 30PSIA, 121°C, PRESSURE COOKER (STEAM)

TEST NUMBER	DEVICE	QTY	ACCUMULATIVE RESULTS[1] AT HOURS SHOWN					FAILURE ANALYSIS[2]	COMMENTS[3]
			8	48	96	144	192		
DT72139	2510A	99	0/99	0/99	-	-	-		R336
DT74103	4001A	31	0/31	0/31	0/31	1/31	5/31	5-4A	R356
DT74084A	4002A	200	2/200	12/200	14/200	16/200	30/200	30-4A	R350
DT74084B	4011A	500	7/500	31/500	37/500	37/500	41/500	41-4A	R350
DT74084C	4049B	550	4/500	53/500	59/500	107/550	308/550	308-4A	R350
DT74084D	4050B	325	1/325	53/325	73/325	148/325	236/325	236-4A	R350
	Total=Failures		14	149	183	309	620		
	Total=Devices		1705	1705	1606	1606	1606		
	% Failures		0.8	8.7	11.4	19.2	38.3		

Table 14-10 SILICONE ENCAPSULATED MOS PRODUCTS VS. 30PSIA, 121°C PRESSURE COOKER (STEAM)

NOTES:
1. The results are listed as cumulative rejects to the timepoint shown over starting sample size. All devices received functional test as a minimum pass/fail criterion.
2. The failure analysis results are shown via code X-YZ, where X is the quantity of failures with mechanism YZ. The YZ mechanisms are defined as follows
   2. Die Problems
      E. Cause Unknown, Electrical Degradation
   4. Miscellaneous
      A. Failures Not Analyzed
      B. Aluminum Corrosion (moisture ingression, etc.)
3. RXXX refers to a Signetics internal reliability report.
4. Data is from Table 14-12 and represents 195 "lots" tested during 1974 via the Product Monitor Program (Sigkor).
5. The Product Monitor Program (Sigkor) was changed (2x1) in 1975 from 8 hours to 144 hours pressure cooker. Data shown represents the first 14 weeks, contains 49 "lots" of which 31% had zero rejects and 61% had less than 4% rejects through 144 hours. Thermal scan and GFT were used at zero hours; GFT at 144 hours.
6. Results reported by package engineering 31 January 1975. Nine lots of 25 devices each (7400A, 7404A, 7402A, 7442B) were tested to 1000 hours as part of a pre-shipment study. Sitek functional testing used.
7. Results reported by package engineering 4 June 1975. Six lots of 100 each glassed vs. non-glassed 7400A and 7404A were tested to 2000 hours to establish a data base. Sitek 3200A functional testing was used.
8. Sigkor Deflash Approval Memo, 28 January 1975. Five lots of devices represented.

TEST NUMBER	COMPETITOR	DATE CODE	QTY	ACCUMULATIVE RESULTS[1] AT HOURS SHOWN				FAILURE ANALYSIS[2]	COMMENTS[3]
				48	96	144	192		
DT74103	A	7411	32	1/32	3/32	9/32	32/32	32-4A	R356
DT74103	B	7402	32	2/32	3/32	3/32	4/32	4-4A	R356
DT74103	C	7415	31	1/31	9/31	16/31	22/31	22-4A	R356
DT74103	D	7413	29	2/29	13/29	28/29	28/29	28-4A	R356
DT74103	E	7333	32	6/32	11/32	16/32	23/32	23-4A	R356
DT74103	F	7349	26	11/26	11/26	14/26	17/26	17-4A	R356
	Total=Failures			23	50	86	126		
	Total=Devices			182	182	182	182		
	% Failures			12.6	27.5	47.3	69.2		

NOTES:
1. The results are listed as cumulative rejects to the timepoint shown over starting sample size. All devices received functional test as a minimum pass/fail criterion.
2. The failure analysis results are shown via code X-YZ, where X is the quantity of failures with mechanism YZ. The YZ mechanisms are defined as follows
   2. Die Problems
      E. Cause Unknown, Electrical Degradation
   4. Miscellaneous
      A. Failures Not Analyzed
      B. Aluminum Corrosion (moisture ingression, etc.)
3. RXXX refers to a Signetics internal reliability report.
4. Data is from Table 14-12 and represents 195 "lots" tested during 1974 via the Product Monitor Program (Sigkor).
5. The Product Monitor Program (Sigkor) was changed (2x1) in 1975 from 8 hours to 144 hours pressure cooker. Data shown represents the first 14 weeks, contains 49 "lots" of which 31% had zero rejects and 61% had less than 4% rejects through 144 hours. Thermal scan and GFT were used at zero hours; GFT at 144 hours.
6. Results reported by package engineering 31 January 1975. Nine lots of 25 devices each (7400A, 7404A, 7402A, 7442B) were tested to 1000 hours as part of a pre-shipment study. Sitek functional testing used.
7. Results reported by package engineering 4 June 1975. Six lots of 100 each glassed vs. non-glassed 7400A and 7404A were tested to 2000 hours to establish a data base. Sitek 3200A functional testing was used.
8. Sigkor Deflash Approval Memo, 28 January 1975. Five lots of devices represented.

Table 14-11 SIX CMOS COMPETITORS (4001A) EQUIVALENT PRODUCTS) VS. 30PSIA, 121°C, PRESSURE COOKER (STEAM)

Figure 14-3 shows the cumulative percent failures versus cycles for Epoxy Novolac I and Silicone encapsulated products subjected to extended temperature cycles (air to air) and power cycle. The Silicone products (unless otherwise noted) represent product manufactured without an inner die coat/junction coating material. The following comments are appropriate:

Both Silicone and Novolac I encapsulated products are capable of passing 21,000 power cycles of $\Delta Pd \doteq 500$ mW ($\Delta T_J \doteq 80°C$) with approximately 0% rejects. The 21K cycles could be related to turning equipment on and off once per day for 57 years.

Both Silicone and Novolac I encapsulated products demonstrated $\leq 1\%$ failures during 3,000 cycles of accelerated 0 to 125°C temperature cycling.

At 7,000 cycles, silicone has less than 3% failures and Novolac I has 0.03% to 2.1% failures depending upon how one interprets the "error range" of the data Table 14-13.

Graphs 3, 4, and 5 of Figure 14-3 show the accelerating effect of increasing either the temperature range of the temperature upper limit (i.e., 0 to 125°C versus −55°C to 125°C versus 0 to 150°C) during temperature cycling.

Figure 14-4 shows the cumulative percent failures versus extended accelerated thermal shock (liquid to liquid) cycles for Novolac I encapsulated product. Signetics uses accelerated thermal shock testing as an engineering tool to obtain percent failure information in relatively short time periods (as compared to temperature cycling). Since the failure mode distributions for temperature cycle and thermal shock are approximately the same, a good argument exists for the use of thermal shock testing. The reader is cautioned to be aware of the fact that the high stress levels used during thermal shock testing are far beyond the environmental requirements of most applications. The following comments are appropriate:

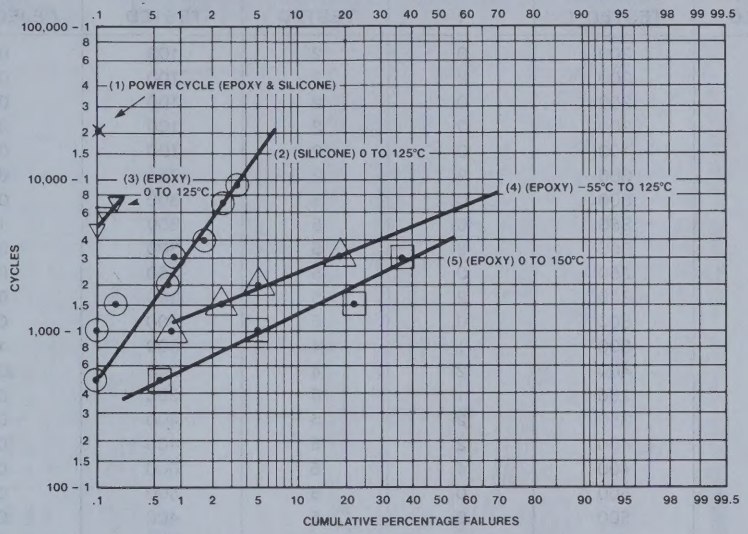
There appears to be an acceleration factor of 7X between −55°C to 125°C and −65°C to 150°C stress levels during 1,000 cycles of thermal shock.

A comparison of −55°C to 125°C thermal shock (Figure 14-4) to −55°C to 125°C temperature cycle (Figure 14-3) suggests that the effect of liquid to liquid and five minute cycles (for thermal shock) versus air to air and twenty minute cycles (for temperature cycle) is probably a second order effect at most. Based on the number of cycles to failure over the 1 to 30% cumulative failure range, temperature cycle appears to have a 2X acceleration factor over thermal shock for thermal excursions of −55°C to 125°C. However, the 2X acceleration factor could easily be related to the relatively small quantity of samples used for temperature cycle testing and the non-repeatability and scatter of thermal excursion data from lot to lot.

Table 14-12 shows that the "early bond off failure mechanism" has all but disappeared from current products. Part of this improvement is related to a better understanding of optimum bonding parameters and to the changes made to the bonding operation. Part of this improvement is related to the removal of die coating (inner encapsulant junction coating) from silicone packaged products. The die coating was originally placed on the die in 1966 with the intent of protecting the die surface from possible thermal expansion, shock, and contamination problems. These concerns proved to be unfounded.

Fifty-two consecutive weeks of product monitor testing of Epoxy Novolac I assembly has not shown an early bond failure problem during 100 cycles of −65°C to 150°C thermal shock. Of the 0.38% rejects obtained on this accelerated stress, only 0.09% were of a lifted ball bond failure mechanism. Not shown in Table 14-12 are the results of 100 cycles of −65°C to 150°C thermal shock testing of Silicone products. Internal report R329 (which was referenced for Table 14-12) shows that silicone products without die coating had 0.80% rejects (16 out of 1,999) when tested to 25°C and then 125°C LVC (low voltage continuity to detect bond problems) following the 100 cycles of accelerated stress. The failure mechanisms were not listed for the sixteen silicone rejects. Another study performed at the time that the die coating was removed showed 0% failures (sample size of 999) after 100 cycles of −65°C to 150°C thermal shock. That study used functional test at 25°C and 125°C as a failure criteria. All samples in that study received a pre-screen of D.C. parametric test, fifteen cycles of 0 to 100°C thermal shock and high temperature functional test.

CUMULATIVE % FAILURES vs. EXTENDED TEMPERATURE AND POWER CYCLES for EPOXY NOVOLAC I & SILICONE ENCAPSULATED DEVICES

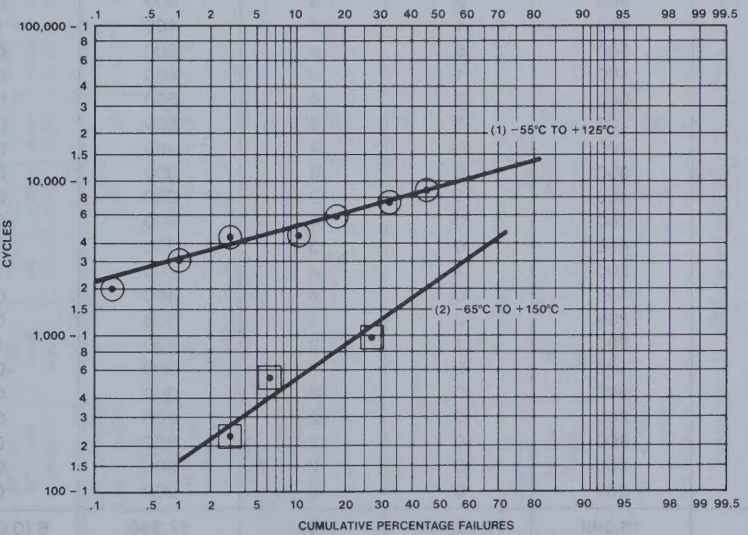

(1) POWER CYCLE (EPOXY & SILICONE)
(2) (SILICONE) 0 TO 125°C
(3) (EPOXY) 0 TO 125°C
(4) (EPOXY) −55°C TO 125°C
(5) (EPOXY) 0 TO 150°C
CYCLES
CUMULATIVE PERCENTAGE FAILURES

NOTES

1. The graph for both Silicone and Epoxy Novolac encapsulated devices vs. 25°C ambient power cycle ($\Delta Pd \doteq 500$ mW) is based on the data from Table 14-15 and Table 14-16.
2. The graph for Silicone encapsulated devices vs. 0 to 125°C temperature cycle is based on the data from Table 14-14.
3. The graph for Epoxy Novolac encapsulated devices vs. 0 to 125°C temperature cycle is based on the data from Table 5-13 through 7000 cycles.
4. The graph for Epoxy Novolac encapsulated devices vs. −55°C to 125°C temperature cycle is based on the data from Table 14-13.
5. The graph for Epoxy Novolac encapsulated devices vs. 0°C to 150°C temperature cycle is based on the data from Table 5-13 (Customer A data).
6. Engineering judgment was used in constructing the graphs based on the tabulated data. Straight lines which result from plotting data on logarithm of cycles to failure versus normal probability scale graph paper represent log-normal failure distributions. For such distributions, median life corresponds to t @ 50% and the standard deviation to ln [t @ 50%/t @ 16%].

Figure 14-3

CUMULATIVE % FAILURES vs. EXTENDED THERMAL SHOCK CYCLES FOR EPOXY NOVOLAC I ENCAPSULATED DEVICES



NOTES

1. The graph for Epoxy Novolac encapsulated devices vs. −55°C to +125°C thermal shock is based on the data from Table 14-17 using the 8000 cycle sample size of 498.
2. The graph for Epoxy Novolac encapsulated devices vs. −65°C to +150°C thermal shock is based on the data from Table 14-17 using the 1000 cycle sample size of 4,433.
3. Engineering judgment was used in constructing the graphs based on the tabulated data. Straight lines which result from plotting data on logarithm of cycles to failure versus normal probability scale graph paper represent log-normal failure distributions. For such distributions, median life corresponds to t @ 50% and the standard deviation to ln [t @ 50%/t @ 16%].

Figure 14-4

	THERMAL SHOCK (LIQUID TO LIQUID) 100 CYCLES, −65 TO 150°C			PRESSURE COOKER (IN STEAM) 8 HOURS, 30 PSIA, 121°C			
WEEK	#LOTS TESTED	QUANTITY TESTED 1	REJECTS 1	#LOTS TESTED	QUANTITY TESTED	VALID REJECTS 2	TOTAL REJECTS 2
7401	2	200	0	2	100	0	1
7402	2	200	2	2	100	0	0
7403	2	200	0	2	100	0	0
7404	2	200	0	2	100	0	0
7405	1	100	0	2	100	0	0
7406	5	300	9	2	250	0	0
7407	5	500	12	5	300	0	2
7408	5	350	6	5	300	1	6
7409	5	350	2	5	300	0	3
7410	5	250	0	5	350	0	0
7411	5	350	2	5	300	0	2
7412	5	500	0	5	500	0	4
7413	4	300	1	4	300	1	2
7414	5	400	2	4	300	0	1
7415	5	250	1	5	350	0	0
7416	5	350	2	5	400	0	0
7417	5	400	2	5	400	0	2
7418	5	400	4	5	500	0	0
7419	5	500	0	5	500	0	4
7420	5	500	0	5	400	0	0
7421	4	300	0	4	300	0	1
7422	5	400	0	5	400	0	0
7423	5	400	1	5	400	0	0
7424	5	500	0	5	500	0	0
7425	5	400	0	5	400	0	0
7426	5	400	2	5	500	0	1
7427	4	400	0	4	400	1	12
7428	4	400	2	4	400	0	2
7429	4	400	0	4	400	0	0
7430	4	500	0	4	400	0	2
7431	4	400	1	4	500	0	6
7432	4	500	0	4	500	0	2
7433	4	400	1	4	400	1	1
7434	4	500	5	4	500	0	5
7435	4	400	1	4	400	0	1
7436	4	500	3	4	500	0	2
7437	4	500	3	4	500	0	1
7438	4	400	3	4	400	0	2
7439	3	300	0	3	300	0	1
7440	4	400	1	3	300	0	0
7441	4	400	0	4	400	0	5
7442	4	400	0	3	300	0	2
7443	3	300	1	3	300	1	1
7444	4	400	0	4	400	0	2
7445	3	299	0	2	200	0	0
7446	2	200	1	2	200	1	1
7447	3	300	0	3	300	0	1
7448	3	300	0	3	300	0	1
7449	2	200	0	2	200	0	0
7450	2	200	0	2	200	0	0
7451	2	200	0	2	200	0	0
7452	2	200	0	2	200	0	0
Totals	201	18,399	70 (0.3%)	195	17,550	6 (0.034%)	79 (0.45%)

NOTES

1. Samples came from final test parametric rejects (to reduce costs) that passed subsequent +25°C general functional test (GFT) and thermal scan (bond continuity test from +25°C to +125°C). Thermal scan was used for the post stress reject criteria. Of the 70 rejects shown, 16 were for lifted ball bonds.
2. Samples came from final test parametric rejects (to reduce costs) that passed subsequent +25°C GFT. Post stress reject criteria was to +25°C GFT. Failures related to mechanical problems that might have been removed had a zero hour thermal scan been performed were discounted from the valid rejects.
3. The data for Table 14-12 is reported in Signetics Internal Reliability Report R329.

Table 14-12 1974 PRODUCT MONITOR DATA FOR EPOXY NOVOLAC I ENCAPSULATED BIPOLAR PRODUCTS

TEMP. CYCLE RANGE[1]	TEST NUMBER	DEVICE	QTY	ACCUMULATIVE REJECTS[1] OVER STARTING AT THE NUMBER OF CYCLES SHOWN												FAILURE ANALYSIS[2]	COMMENTS[1]
				100	500	1,000	1,500	2,000	3,000	4,000	5,000	6,000	7,000	8,000	9,000		
0°C to 125°C	DT73094A	7400A	404	0/404	0/404	0/404	0/404	0/404	0/404	0/404	0/404	0/404	—		—		R266
0°C to 125°C	DT73094B	7400A	477	0/477	0/477	0/477	0/477	0/477	0/477	0/477	0/477	0/477	—	28/1300	—	27-1C, 1-4E	R266
0°C to 125°C	DT73094C	7400A	419	0/419	0/419	0/419	0/419	0/419	0/419	0/419	0/419	0/419	—		—		R266
0°C to 125°C	DT73102A	7400A	190	0/190	0/190	0/190	0/190	0/190	0/190	0/190	0/190	—	—	—	12/190	12-1C	R266
0°C to 125°C	DT73102B	7400A	97	0/97	0/97	0/97	0/97	0/97	0/97	0/97	0/97	—	—	—	32/97	31-1C, 1-4A	R266
0°C to 125°C	DT73120A	7442B	694	0/694	0/694	0/694	0/694	0/694	0/694	—	—	—	1/694	—	—	1-1C	R266
0°C to 125°C	DT73120B	7442B	116	0/116	0/116	0/116	0/116	0/116	0/116	0/116	0/116	0/116	0/116	—	—		R266
0°C to 125°C	DT73121A	7400A	783	0/783	0/783	0/783	0/783	0/783	0/783	0/783	0/783	0/783	0/783	—	—		R266
0°C to 125°C	DT73121B	7400A	282	0/282	0/282	0/282	0/282	0/282	0/282	0/282	0/282	0/282	0/282	—	—		R266
0°C to 125°C	Customer A	7400A	150	0/150	0/150	0/150	0/150	0/150	0/150	0/150	0/150	5/150	—	—	—	5-1C	R266, P.E. @70°C
	Total = Failures			0	0	0	0	0	0	0	1	5	1	28	44		
	Total = Devices			3612	3612	3612	3612	3612	3612	2918	2918	2631	1875	1300	287		
	% Failures			0	0	0	0	0	0	0	0.03	0.20	0.05	2.2	15.3		
0° C to 135° C	DT74014A	7400A	500	0/500	0/500	0/500	0/500	0/500	0/500	—	—	—	—	—	—		R266
0°C to 135°C	DT74014B	7400A	500	0/500	0/500	0/500	0/500	0/500	0/500	—	—	—	—	—	—		R266
0°C to 135°C	DT74020A	7400A	83	0/83	0/83	0/83	0/83	0/83	—	—	—	—	—	—	—		R266
0°C to 135°C	DT74029	(TH.DIE) BA	34	0/34	0/34	0/34	0/34	0/34	—	—	—	—	—	—	—		R269
0°C to 135°C	DT74050	10171BA	174	0/174	0/174	0/174	0/174	0/174	—	—	—	—	—	—	—		R269
	Total = Failures			0	0	0	0	0	0								
	Total = Devices			1291	1291	1291	1291	1291	1000								
	% Failures			0	0	0	0	0	0								
0°C to 140°C	Customer A	7400A	48	0/48	0/48	0/48	0/48	4/48	7/48	14/48	20/48	—	—	—	—	≈ 4-1C, 16-4A	R266, P.E. @70°C
	% Failures			0	0	0	0	8.3	14.6	29.2	41.7						
0°C to 150°C	Customer A	7400A	150	0/150	1/150	8/150	31/150	—	55/150	—	—	—	—	—	—	≈ 55-1C	R266, P.E. @70°C
0°C to 150°C	Glass Study	Mix	197	0/297	0/297	7/297	—	—	—	—	—	—	—	—	—	7-4A	(3)
	% Failures			0	0.2	3.4	20.7	—	36.7								
−55°C to 125°C	Pre-Ship	Mix	100	0/100	0/100	0/100	0/100	0/100	0/100	0/100	0/100	4/100	4/100	—	—		(4)
−55°C to 125°C	DT74060	7400A	100	0/100	0/100	2/100	6/100	13/100	31/100	—	—	—	—	(85/100)	—	2-1B, 11-1C, 18-4A	R345, DEQP (5)
−55°C to 125°C	DT75001	7400A	50	0/50	0/50	0/50	0/50	0/50	18/50	29/50	—	—	—	—	—	29-1C	R352, CEQP
	Total = Failures			0	0	2	6	13	49	29	0	4	4	85			
	Total = Devices			250	250	250	250	250	250	150	100	100	100	100			
	% Failures			0	0	0.8	2.4	5.2	19.6	19.3	0	4	4	85			

Table 14-13 EPOXY NOVOLAC I ENCAPSULATED DEVICES vs. EXTENDED TEMPERATURE CYCLE (AIR to AIR) 1973 to 1975

TEMP. CYCLE RANGE[1]	TEST NUMBER	DEVICE	QTY	ACCUMULATIVE REJECTS[1] OVER STARTING AT THE NUMBER OF CYCLES SHOWN											FAILURE ANALYSIS[2]	COMMENTS[1]
				100	500	1,000	1,500	2,000	3,000	4,000	5,000	6,000	7,000	8,000	9,000	
0°C to 125°C	DT73087	5070B	975	1/975	2/975	2/975	3/975	9/975	11/975	13/975	—	—	31/975	—	41/975	11-4A, 5-4E, 12-1B, 13-1C,	R266
0°C to 125°C	DT73088	5070B	995	0/995	0/995	0/995	1/995	6/995	8/995	19/995	—	—	23/995	—	26/995	6-4A, 1-4E, 12-1B, 5-1C, 2-3D	R266
Total = Failures				1	2	2	4	15	19	32	—	—	54	—	67		
Total = Devices				1970	1970	1970	1970	1970	1970	1970	—	—	1970	—	1970		
% Failures				0.05	0.10	0.10	0.20	0.76	0.96	1.6	—	—	2.7	—	3.4		

Table 14-14 SILICONE ENCAPSULATED DEVICES vs. EXTENDED TEMPERATURE CYCLE (AIR TO AIR AT 3CYCLE/HOURS) - 1973

POWER CYCLE T_A = 25°	TEST NUMBER	DEVICE	QTY	ACCUMULATIVE REJECTS[1] AT CYCLES				FAILURE ANALYSIS	COMMENTS[1]
				2,016	8,064	14,400	21,000		
5 min./cycle	DT72170	5723A	39	0/39	0/39	0/39	—	—	Rejection Criterion was to go-no-go parametic test at 25°C. R279, R336
5 min./cycle	DT72158	2510A	37	0/37	0/37	0/37	—	—	Rejection Criterion was to go-no-go parametic test at 25°C. R279, R336
5 min./cycle	DT72113B	7400A	125	0/125	0/125	0/125	0/125	—	R279, R336
5 min./cycle	DT721130	7402AH	85	0/85	0/85	0/85	0/85	—	R279
5 min./cycle	DT73062	7400AH	71	0/71	0/71	0/71	—	—	R279
5 min./cycle	DT74119	7400AH	98	0/98	0/98	0/98	—	—	R279
Total = Failures				0	0	0	0		
Total = Devices				455	455	455	210		
% Failures				0	0	0	0		

Table 14-15 EPOXY NOVOLAC 1 ENCAPSULATED DEVICES vs. POWER CYCLE AT 25°C AMBIENT (Δ PD ≐ 0.5W) 1972 to 1974

POWER CYCLE T_A = 25°	TEST NUMBER	DEVICE	QTY	ACCUMULATIVE REJECTS[1] AT CYCLES				FAILURE ANALYSIS[2]	COMMENTS[1]
				2,016	8,064	14,400	21,000		
5 min./cycle	DT72113	7400A	158	0/158	0/158	0/158	1/158	1-1B	Devices had old silicone die coat material; removed from assembly in 1972. R279
5 min./cycle	DT72113	7400A	157	0/157	0/157	0/157	0/157		R279, R336
5 min./cycle	DT72157	2501A	33	0/33	0/33	0/33	—		R279, R336. Reject criterion was to go-no-go parametic test at 25°C.
5 min./cycle	DT72169	5723A	40	0/40	0/40	0/40	—		R279, R336. Reject criterion was to go-no-go on parametic test at 25°C.
Total = Failures				0	0	0	1		
Total = Devices				388	388	388	315		
% Failures				0	0	0	0.3		

Table 14-16 SILICONE ENCAPSULATED DEVICES vs. POWER CYCLE AT 25°C AMBIENT (Δ Pd ≐ 0.5W) — 1972

NOTES

1. Thermal scan (+25°C to > +125°C) was used as a reject criterion unless otherwise noted in the Comments column. RXXX refers to Signetics internal reliability report.
2. The results of failure analysis are shown via code X-YZ where X is the quantity of failures with mechanism YZ. The YZ mechanism are defined as follows:
   1. Bond Problems
      B. Poor Bond Adherence (substandard bonds)
      C. Broken Bond Wires (at the die package)
   3. Assembly and Package Problems
      D. Wire breakage (in the span)
   4. Miscellaneous
      A. Failures Not Analyzed
      E. Not Verified. No F/A performed.

THERMAL SHOCK RANGE	TEST NUMBER	DEVICE	QTY	ACCUMULATIVE REJECTS (1) OVER STARTING QUANTITY AT THE NUMBER OF CYCLES SHOWN													FAILURE ANALYSIS [2]	COMMENTS [1]
				100	250	500	1000	1500	2000	3000	4000	5000	6000	7000	8000	9000		
−55°C to 125°C	DT74029	(Th. Die)BA	32	0/32	0/32	—	—	—	—	—	—	—	—	—	—	—	—	R269
−55°C to 125°C	DT74050	10171BA	174	0/174	0/174	—	—	—	—	—	—	—	—	—	—	—	—	R269
−55°C to 125°C	DT74061	7400A	100	0/100	0/100	0/100	1/100	3/100	3/100	—	—	—	—	—	—	—	2-1B, 1-1C	R345, DEQP
−55°C to 125°C	DT74122	4001A	100	0/100	0/100	0/100	0/100	0/100	0/100	—	—	—	—	—	—	—	—	R356
−55°C to 125°C	SIGKOR '74	C2225A	100	0/100	0/100	0/100	0/100	0/100	0/100	0/100	2/100	10/100	17/100	26/100	45/100	—	≈75%-1C	R328. (3)
−55°C to 125°C	SIGKOR '74	C2238A	98	0/98	0/98	0/98	0/98	0/98	0/98	0/98	0/98	2/98	4/98	15/98	27/98	—	≈75%-1C	R328, (3)
−55°C to 125°C	SIGKOR '74	C2163A	100	0/100	0/100	0/100	0/100	0/100	0/100	0/100	3/100	12/100	24/100	46/100	60/100	—	≈75%-1C	R328, (3)
−55°C to 125°C	SIGKOR '74	D2088A	100	0/100	0/100	0/100	0/100	0/100	0/100	0/100	1/100	8/100	17/100	33/100	47/100	—	≈75%-1C	R328, (3)
−55°C to 125°C	VTS '74	7420A	50	0/50	0/50	0/50	0/50	0/50	1/50	5/50	9/50	22/50	25/50	33/50	43/50	—	43-4A	(3)
−55°C to 125°C	11S	7440	25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	2/25	2-4A	(3)
−55°C to 125°C	33S	7440A	25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	2/25	2/25	2/25	3-4A	3-4A	(3)
		Total ≠ Failures		0	0	0	1	3	4	5	15	54	89	155	224	5		
		Total ≠ Devices		904	904	698	698	698	698	498	498	498	498	498	498	50		
		% Failures		0	0	0	0.1	0.4	0.6	1.0	3.0	10.8	17.9	31.1	45	10		
−65°C to 150°C	DT74106	4001A	24	—	—	5/24	18/24	24/24	—	—	—	—	—	—	—	—	7-1C, 17-4A	R356
−65°C to 150°C	DT75003	7400A	50	—	—	47/50	50/50	—	—	—	—	—	—	—	—	—	30-1C, 20-4A	R352, CEQP
−65°C to 150°C	DT73176	(MIX) A	136	1/136	1/136	—	—	—	—	—	—	—	—	—	—	—	1-1C	R280
−65°C to 150°C	SIGKOR '74	Pd3-N	200	—	7/200	49/200	152/200	—	—	—	—	—	—	—	—	—	85%-1C, 12%-3D	R328, (4)
−65°C to 150°C	SIGKOR '74	Pd4-N	400	—	1/400	37/400	149/400	—	—	—	—	—	—	—	—	—	68%-1C, 30%-3D	R328, (4)
−65°C to 150°C	SIGKOR '74	Pd5/6-N	700	—	0/700	7/700	83/700	—	—	—	—	—	—	—	—	—	76%-1C, 15%+3D	R328, (4)
−65°C to 150°C	SIGKOR '74	Pd7-H	300	—	2/300	2/300	6/300	—	—	—	—	—	—	—	—	—	5-1C, 1-3D	R328, (4)
−65°C to 150°C	SIGKOR '74	Pd8-H	300	—	2/300	2/300	3/300	—	—	—	—	—	—	—	—	—	1-1C, 2-3D	R328, (4)
−65°C to 150°C	SIGKOR '74	H-Pd3	200	—	3/200	26/20	170/200	—	—	—	—	—	—	—	—	—	79%-1C, 19%-3D	R328, (4)
−65°C to 150°C	SIGKOR '74	H-Pd4	400	—	6/400	33/400	148/400	—	—	—	—	—	—	—	—	—	68%-1C. 26%-3D	R328, (4)
−65°C to 150°C	SIGKOR '74	H-Pd5/6	700	—	2/700	7/700	77/700	—	—	—	—	—	—	—	—	—	81%-1C, 11%-3D	R328. (4)
−65°C to 150°C	SIGKOR '74	N-Pd7	300	—	0/300	0/300	1/300	—	—	—	—	—	—	—	—	—	1-1B	R328, (4)
−65°C to 150°C	SIGKOR '74	N-Pd8	300	—	2/300	2/300	4/300	—	—	—	—	—	—	—	—	—	3-1B, 1-3D	R328, (4)
−65°C to 150°C	SIGKOR '74	C2225A	99	—	—	6/99	34/99	77/99	—	—	—	—	—	—	—	—	≈75%-1C	R328, (3)
−65°C to 150°C	SIGKOR '74	C2238A	100	—	—	1/100	18/100	51/100	—	—	—	—	—	—	—	—	≈75%-1C	R328, (3)
−65°C to 150°C	SIGKOR '74	C2163A	99	—	—	7/99	50/99	83/99	—	—	—	—	—	—	—	—	≈75%-1C	R328, (3)
−65°C to 150°C	SIGKOR '74	C2088A	100	—	—	2/100	37/100	64/100	—	—	—	—	—	—	—	—	60-4A	(3)
−65°C to 150°C	VTS '74	7420A	63	—	—	19/63	54/63	60/63	—	—	—	—	—	—	—	—	2-4A	(3)
−65°C to 150°C	11S	7440A	49	1/49	1/49	1/49	2/49	—	—	—	—	—	—	—	—	—	4-4A	(3)
−65°C to 150°C	33S	7440A	49	0/49	0/49	0/49	4/49	—	—	—	—	—	—	—	—	—	40%-1B, 27%-1C	R329, (4)
−65°C to 150°C	Table 5-12	MIX	18,399	70/18,399	—	—	—	—	—	—	—	—	—	—	—	—		R269
−65°C to 150°C	DT73151	7402AA	33	0/33	—	—	—	—	—	—	—	—	—	—	—	—		R269
−65°C to 150°C	DT74029	(T. Die)BA	32	0.31	0.31	—	—	—	—	—	—	—	—	—	—	—		R269
−65°C to 150°C	DT74050	10171BA	174	0/174	0/174	—	—	—	—	—	—	—	—	—	—	—		
		Total ≠ Failures		72	27	253	1,060	359										
		Total ≠ Devices		18,871	4,239	4,433	4,433	461										
		% Failures		0.38	0.6	5.7	23.9	77.9										

NOTES

1. Thermal Scan (25°C to 125°C) to monitor bond continuity was used as the reject criterion. RXXX under comments refers to a Signetics Internal Reliability Report.
2. The results of failure analysis are shown via code X, YZ where X is the quantity of failures with mechanism YZ. The YZ mechanisms are defined as follows:
   1. Bond Problems
      B. Poor Bond Adherence (Substandard Bonds)
      c. Broken Bond Wires (At the Die or Package)
   3. Assembly and Package Problems
      D. Wire Breakage (In the Span)
   4. Miscellaneous
      A. Failures Not Analyzed.
3. The Signetics Package Development Group performed these tests.
4. Sigkor performed these tests.

Table 14-17 EPOXY NOVOLAC 1 ENCAPSULATED DEVICES vs. EXTENDED THERMAL SHOCK (LIQUID TO LIQUID) — 1974

Plastic Encapsulated Product Performance Compared to Hermetic Package Product Performance

The March 1975 SURE II Bulletin 5005 describes the Signetics program to periodically qualify die process families, hermetic package families, and plastic package families to stresses equal to or exceeding the requirements of MIL-STD-883A, Method 5005.2.

Signetics frequently performs initial qualification of a new package using stress levels beyond the requirement of the SURE program (new lead frame materials may be tested for hundreds of hours of salt atmosphere, new hermetic packages are routinely tested for hermetic seal integrity after 200 cycles of −65°C to 150°C thermal shock, new cavity materials are routinely tested for a bond pull and die pry performance, etc.) After intitial qualification, new packages are incorporated into the ongoing SURE qualification program. Table 14-18 is an example of initial qualification studies performed during the qualification of the new U (TO-220) and S (TO-92) plastic packages.

Plastic packages do not have a hermetic cavity and hence cannot be tested for hermetic seal. Plastic packages are also unique in that the molding compound surrounds the bond wires and die causing concern about parametic stability and the thermomechanical properties of the materials used. As a result, stresses beyond the scope of MIL-STD-883 testing were implemented to determine the susceptibility of the plastic encapsulated product to moisture (hermetic products need only retain their hermetic seal) and thermomechanical stresses. Section 14, therefore, covered these considerations and those test procedures which apply primarily to plastic encapsulated integrated circuits.

Plastic packages, due to their construction, are inherently more rugged than cavity type packages. Thus, stresses such as acceleration, vibration, and mechanical shock have less impact when applied to plastic packages since bond wires and lid/caps cannot be made to fly off and die cannot be made to come loose from their die attach pads.

Frequently a customer requires help in determining which package (plastic or hermetic) is better suited for his application. Table 14-19, which for simplicity compares the Cerdip package family to the Epoxy Dip package family, was constructed to help in deciding whether a plastic package is better suited for a specific application.

STRESS	TEST CONDITION	TIME POINTS	TO-220 CUM. REJ./START QTY		TO-92 CUM. REJ./START QTY	
			SIGNETICS 1,2	COMPETITOR A 1,2	SIGNETICS 1,3	COMPETITOR A 1,3
HTOL T_A=85°C	For TO-220, V_{CC}=8 Volts, P_D=300mW	240 Hour	0/45	17/48	0/50	1/50
	For TO-92, V_{CC}=15 Volts, P_D=270mW	1,000 Hour	0/45	17/48 (7-2E, 10-4A)	0/50	2/50
	Recorded Data	2,000 Hour	0/45	—	0/50	3/50 (3-2E)
HTSL 150°C		240 Hour	0/45	10/28	0/50	—
		1,000 Hour	0/45	10/28 (3-2E, 7-4A)	0/50	—
	Recorded Data	2,000 Hour	1/45 (1-2E a DEG)	—	0/50	—
Power Cycle T_A=25°C	For TO-220, V_{CC}=9 Volts, ΔP_D=4.2W.	2,880 cycles	0/45	3/24	0/25	1/25
	5 min./cycle, Recorded Data	6,000 cycles	—	—	0/25	2/25
	For T0-92, V_{CC}=10 Volta, ΔP_D=350mW	12,000 cycles	0/45	4/24 (2-2E, 2-4A)	0/25	2/25 (2-1B)
	10 min./cycle, Thermal Scan[4]	24,000 cycles	0/45	—	—	—
Temperature Cycle	M.S. 883A, Meth. 1010.1, Cond. B	500 cycles	0/52	0/25	—	—
	(−55°C to 125°C)	1,000 cycles	0/52	2/25	0/50	26/48 (20-1B)
	Thermal Scan[4]	2,000 cycles	0/52	15/25 (8-1C, 7-4A)	0/50	40/48 (20-4A)
Thermal Shock	M.S. 883A, Meth. 1011.1, Cond. B	200 cycles	0/52	0/23	0/50	34/48 (17-1B)
	(−55°C to 125°C) for TO-220, Cond. C (−65°C to 150°C) for To-92. Thermal Scan[4]	1,000 cycles	—	—	0/50	48/48 (31-4A)
Temperature Humidity	For T0-220, M.S. 883A, Meth. 1004.1	240 Hours	0/52	—	0/49	1/50 (1-4B)
	Moisture Resistance. For T0-92, 85°C/	1,000 Hours	—	—	0/49	1/50
	85% R.H./5 volt. Both had Recorded Data	2,000 Hours	—	—	1/49 (1-4B)	2/50 (1-4A)
Pressure Cooker 2-1B)	30 PSIA (15 PSIG), 121°C	24 Hours	0/52	—	0/40	8/50
		48 Hours	0/52	—	0/40	15/50 (12-4B,
		72 Hours	—	—	1/40 (1-4B)	21/50 (7-4A)
	Recorded Data	96 Hours	2/52 (2-4B)	10/29 (10-4B)	—	—

NOTES

1. The results of failure analysis are shown via code X-YZ (in parentheses) where X is the quantity of failures with mechanisms YZ. The YZ mechanisms are defined as follows:
   1. Bond Problems
      B. Poor Bond Adherence (substandard bond)
      C. Broken Bond wires (at the die or package)
   2. Die Problems
      E. Cause Unknown, Electircal Degradation.
   4. Miscellaneous
      A. Failures Not Analyzed
      B. Aluminum Corrosion
2. Internal reports R337, R340 and R394 and test control numbers DT74903/96, DT75008/12 apply to this study. All dice were 7805 voltage regulators. Signetics products were encapsulated in DC480 silicone.
3. Internal reports R351, R361 and R402 and test control numbers DT75017/18/19 apply to this study. All dice were 78LXXX voltage regulators. 78LO5 dice were used for HTOL, HTSL and Temperature Humidity. 78LO6 dice were used for power cycle and pressure cooker. 78L12 dice were used for temperature cycle and thermal shock. Signetics products were encapsulated in Epoxy Novolac 1.
4. Thermal Scan (continuous electrical monitor during +25°C to > +125°C) for bond continuity was used as a reject criteria.

Table 14-18 INITIAL 1975 QUALIFICATION DATA FOR THE U PACKAGE (TO-220) AND THE S PACKAGE (TO-92)

APPLICATION OR PERFORMANCE CONSIDERATION	GENERAL COMPARISON 1		COMMENTS
	EPOXY DIP	CERDIP	
Cost	Lower	Higher	
Failure Rate for Steady State non-Humid Environment	Same (0.0024%/1000 Hour)	Same (0.0024%/1000 Hour)	Refer to Section 14.3 and Table 14.2 for details
Thermal Resistance (Effect on T_J During Operation)	Usually Higher	Standard	Medium Power Plastic Packages with a θ_{JA} comparable to CERDIP are available
Storage Temperature (Maximum Rating)	150°C	200°C	E-DIP Limited by Au-Al bonding system and epoxy thermal stability. Ref. Sec. 5.1
Temperature Limit for Reverse Bias Stresses	$\leq$125°C	150°C	E-DIP $\leq$125°C to keep $T_J \leq$150°C for extended stress times.
Resistance to Mechanical Abuse	High Strength Encapsulant	Package Strength is related to the seal area	CERDIPs could lose their hermetic seal with abnormal handling, board insertion, etc.
Mechanical Shock Mechanical Vibration Constant Acceleration	Solid Package	Cavity Package	BOTH packages easily meet SURE subgroup C2 requirements of Table 4-2*. (Refer to Section 14.6 also)
Salt Atmosphere (For Lead Corrosion)	Same	Same	BOTH packages have Alloy 42 leadframes, CERDIP has tin plated, E-DIP has solder dipped leads. See Subgroup C-3 of Table 4-2*.
Thermal Shock, 15~, −65 to 150°C Temperature Cycle, 10~, −65 to 150°C, Moisture Resistance, 10 days	Excellent	Good	See Subgroup C-1 of Table 4-2. The possibility of CERDIP losing hermetic seal increases slightly with larger seal areas.
Extended Power Cycle, 5 min./cycle ΔT_J=80°C	No Bond Problems at 20,000 cycles	No Bond Problems expected at 10,000 cycles	Refer to Figure 14-3 for E-DIP. See note 2 for CERDIP.
Extended Temperature Cycle (Expected Safe Performance Levels)	4000 cyc, 0 to 125°C 1000 cyc, −55 to 125°C 500 cyc, 0 to 150°C	200 cyc, −55 to 125°C	For E-DIP, concern is bond integrity, Refer to Figure 14-3 for E-DIP, For CERDIP, concern is of hermetic seal 3.
Extended Thermal Shock (Expected Safe Performance Levels)	2000 Shocks, 0 to 100°C 1000 Scks, −55 to 125°C 250 Scks, −65 to 150°C	200 Shocks, 0 to 100°C	For E-DIP, concern is bond integrity. Refer to Figure 14-4 for E-DIP. For CERDIP concern is hermetic seal loss 3.
Extended Temperature (85°C) Humidity (85% R.H.) with 5V Bias. (Expected Performance)	2000 Hour, 2% Rejects (4)	Hermetic	For E-DIP, refer to Figure 14-1. CERDIP will also fail if hermetic seal is lost.
Pressure Cooker, 30 PSIA (15 PSIG), 121°C (Expected Performance)	24 hour, 0% Rejects 96 hour, 2% Rejects (4)	Hermetic	For E-DIP, refer to Figure 14-2. CERDIP will also fail if hermetic seal is lost.

NOTES

1. Refer to Table 14-1 for an overview of manufacturing factors and encapsulant considerations vs. potential impact on I.C. Reliability. CERDIP packages have a glass seal at the leadframe and use ultrasonic aluminum wire bonding. The Epoxy DIP packages use Novolac I encapsulant and thermo-compression gold wire bonding.
2. A November 30, 1970 NASA (MSFC) Report, TMX-64566, showed that 2N2222A transistors (vendor unknown) with 1 mil alumninum ultrasonic bonded wire can develop 5.8% cumulative bond failures (at the heel of the bond) after 10,000 cycles (0% at 8,000 cycles) of 6 minute power cycles of ΔPd = 500mW. ΔIc = 50mA. The aluminum wire in air can be expected to see a higher temperature than the gold wire which is surrounded by epoxy. Aluminum wire lead movement caused by Joulian heating (1 R) and die power dissipation can result in fatigue if excessive microcrack/tool marks exist.
3. Signetics packages were tested to and passed 200 cycles of −65°C to +150°C thermal shock. However, a report by W.T. Fitch, "The Degredation of Bonding Wires and Sealing Glasses with Extended Thermal Cycling," appearing in the April 1975 13th Annual Proceedings Reliability Physics, states that 0°C to +100°C thermal shock tests performed on CERDIP packages from 6 vendors showed one vendor having a 50% hermetic seal failure problem after 110 shocks. Seal integrity is related to the amount of an extended thermal shock testing.
4. Refer to Section 14-4 for an interpretation of these reject levels.

*This information supplied upon request.

Table 14-19 A GENERAL COMPARISON OF EPOXY DIP TO CERDIP APPLICATION CONSIDERATIONS

TABLE OF PRODUCTS AND ORDERING INFORMATION

TABLE OF PRODUCTS AND ORDERING INFORMATION

OPERATIONAL AMPLIFIERS

LF155/155A	High Performance JFET Input Op Amp (Low Supply Current)
LF156/156A	High Performance JFET Input Op Amp (Wide Band)
LF157/157A	High Performance JFET Input Op Amp (Wide Band)
LF255	High Performance JFET Input Op Amp (Low Supply Current)
LF256	High Performance JFET Input Op Amp (Wide Band)
LF257	High Performance JFET Input Op Amp (Wide Band)
LF355/355A	High Performance JFET Input Op Amp (Low Supply Current)
LF356/356A	High Performance JFET Input Op Amp (Wide Band)
LF357/357A	High Performance JFET Input Op Amp (Wide Band)
LH2101A	High Performance Amplifier
LH2201A	High Performance Amplifier
LH2301A	High Performance Amplifier
LH2108/2108A	Precision Operational Amplifier
LH2208/2208A	Precision Operational Amplifier
LH2308/2308A	Precision Operational Amplifier
LM101/101A	High Performance Amplifier
LM201/201A	High Performance Amplifier
LM301A	High Performance Amplifier
LM107	General Purpose Operational Amplifier
LM207	General Purpose Operational Amplifier
LM307	General Purpose Operational Amplifier
LM108/108A	Precision Operational Amplifier
LM208/208A	Precision Operational Amplifier
LM308/308A	Precision Operational Amplifier
LM124/124A	General Purpose Single Supply Operational Amplifier
LM158/158A	General Purpose Single Supply Operational Amplifier
LM224/224A	General Purpose Single Supply Operational Amplifier
LM258/258A	General Purpose Single Supply Operational Amplifier
LM324/324A	General Purpose Single Supply Operational Amplifier
LM358/358A	General Purpose Single Supply Operational Amplifier
SA534	General Purpose Single Supply Operational Amplifier
MC1456	High Performance Operational Amplifier
MC1556	High Performance Operational Amplifier
MC1458	General Purpose Operational Amplifier
MC1558	General Purpose Operational Amplifier
SA1458	General Purpose Operational Amplifier
NE/SE515	Differential Amplifier
SE/NE530	Single High Slew Rate Operational Amplifier
SE/NE5530	Dual High Slew Rate Operational Amplifier
NE/SE531	High Slew Rate Operational Amplifier
NE/SE532/532A	Dual Operational Amplifier Single or Dual Power Supply Operation
SA532	Dual Operational Amplifier Single or Dual Power Supply Operation
NE/SE535	Single High Slew Rate Operational Amplifier
NE/SE5535	Dual High Slew Rate Operational Amplifier
NE/SU536	FET Input Operational Amplifier
NE/SE538	Single High Slew Rate Operational Amplifier
NE/SE5538	Dual High Slew Rate Operational Amplifier

NE/SE5534/5534A	Low Noise Operation Amplifier
SE/NE5533/5533A	Dual Low Noise Operational Amplifier
NE5532/5532A	Dual Low Noise Operational Amplifier, Fully Compensated
NE5539	Ultra High Frequency Operational Amplifier
μA709	Operational Amplifier
μA709A	Operational Amplifier
μA709C	Operational Amplifier
SA709C	Operational Amplifier
μA740C	FET Input Operational Amplifier
μA741/741C	General Purpose Operational Amplifier
SA741C	General Purpose Operational Amplifier
μA747/747C	Dual Operational Amplifier
SA747C	Dual Operational Amplifier
μA748/748C	General Purpose Operational Amplifier
SA748C	General Purpose Operational Amplifier
VIDEO AMPLIFIERS	
SE/NE5537	Sample and Hold
LF198/298/398	Sample and Hold
NE/SE592	Video Amplifier
μA733/733C	Differential Video Amplifier
VOLTAGE REGULATORS	
NE/SE5551	Dual Polarity Regulator
NE/SE5552	Dual Polarity Regulator
NE/SE5553	Dual Polarity Regulator
NE/SE5554	Dual Polarity Regulator
NE/SE5555	Dual Polarity Regulator
NE/SE550	Precision Adjustable Regulator
μA723/723C	Precision Voltage Regulator
SA723C	Precision Voltage Regulator
μA78L02AC	Three Terminal Positive Voltage Regulator
μA78L02C	Three Terminal Positive Voltage Regulator
μA78L05AC	Three Terminal Positive Voltage Regulator
μA78L05C	Three Terminal Positive Voltage Regulator
μA78L06AC	Three Terminal Positive Voltage Regulator
μA78L06C	Three Terminal Positive Voltage Regulator
μA78L08AC	Three Terminal Positive Voltage Regulator
μA78L08C	Three Terminal Positive Voltage Regulator
μA78L12AC	Three Terminal Positive Voltage Regulator
μA78L12C	Three Terminal Positive Voltage Regulator
μA78L15AC	Three Terminal Positive Voltage Regulator
μA78L15C	Three Terminal Positive Voltage Regulator
μA78HV05	Three Terminal Positive Voltage Regulator
μA78HV05C	Three Terminal Positive Voltage Regulator
μA78HV06	Three Terminal Positive Voltage Regulator
μA78HV06C	Three Terminal Positive Voltage Regulator
μA78HV08	Three Terminal Positive Voltage Regulator
μA78HV08C	Three Terminal Positive Voltage Regulator
μA78HV12	Three Terminal Positive Voltage Regulator
μA78HV12C	Three Terminal Positive Voltage Regulator
μA78HV14	Three Terminal Positive Voltage Regulator
μA78HV14C	Three Terminal Positive Voltage Regulator
μA78HV15	Three Terminal Positive Voltage Regulator
μA78HV15C	Three Terminal Positive Voltage Regulator
μA78HV18	Three Terminal Positive Voltage Regulator
μA78HV18C	Three Terminal Positive Voltage Regulator
μA78HV24	Three Terminal Positive Voltage Regulator
μA78HV24C	Three Terminal Positive Voltage Regulator

μA78MHV05	Three Terminal Positive Voltage Regulator
μA78MHV05C	Three Terminal Positive Voltage Regulator
μA78MHV06	Three Terminal Positive Voltage Regulator
μA78MHV06C	Three Terminal Positive Voltage Regulator
μA78MHV08	Three Terminal Positive Voltage Regulator
μA78MHV08C	Three Terminal Positive Voltage Regulator
μA78MHV12	Three Terminal Positive Voltage Regulator
μA78MHV12C	Three Terminal Positive Voltage Regulator
μA78MHV15	Three Terminal Positive Voltage Regulator
μA78MHV15C	Three Terminal Positive Voltage Regulator
μA78MHV20	Three Terminal Positive Voltage Regulator
μA78MHV20C	Three Terminal Positive Voltage Regulator
μA78MHV24	Three Terminal Positive Voltage Regulator
μA78MHV24C	Three Terminal Positive Voltage Regulator
78HVMGU1	Four Terminal High Voltage Programmable Positive Regulator
NE5560	Switched Mode Power Supply Controller Circuit
SG1524/2524/3524	Switched Mode Power Supply Controller Circuit
TL-430	Programmable Three Terminal Shunt Regulator

TIMERS

NE/SE555	Timer
SE555C	Timer
SA555	Timer
NE/SE556	Dual Timer
SA556C	Dual Timer
NE/SE556-1	Dual Timer
SE556-1C	Dual Timer
SA556-1	Dual Timer
NE/SE/SA558	Quad Timer
NE/SE/SA559	Quad Timer

COMPARATORS

LH2111	Voltage Comparator
LH2211	Voltage Comparator
LH2311	Voltage Comparator
LM111	Voltage Comparator
LM211	Voltage Comparator
LM311	Voltage Comparator
LM119	Dual Voltage Comparator
LM219	Dual Voltage Comparator
LM319	Dual Voltage Comparator
LM139/139A	Quad Voltage Comparator
LM239/239A	Quad Voltage Comparator
LM339/339A	Quad Voltage Comparator
MC3302	Quad Voltage Comparator
LM2901	Quad Voltage Comparator
LM193/193A	Low Power Dual Voltage Comparator
LM293/293A	Low Power Dual Voltage Comparator
LM393/393A	Low Power Dual Voltage Comparator
LM2903	Low Power Dual Voltage Comparator
NE521	High Speed Dual Differential Comparator/Sense Amp
NE522	High Speed Dual Differential Comparator/Sense Amp
NE/SE527	Voltage Comparator
NE/SE529	Voltage Comparator
μA710	Differential Voltage Comparator
μA711	Dual Voltage Comparator

MEMORY INTERFACE

55/75325	Memory Driver
75S207	High Speed Dual Sense Amplifier for MOS Memories

75S208	High Speed Dual Sense Amplifier for MOS Memories
7520	Dual Core Memory Sense Amplifier
7522	Dual Core Memory Sense Amplifier
7524	Dual Core Memory Sense Amplifier
7528	Dual Core Memory Sense Amplifier
75232	Dual Core Memory Sense Amplifier
75234	Dual Core Memory Sense Amplifier
75324	Memory Driver with Decode Inputs
INTERFACE	
DS3611	High Voltage Peripheral Driver
DS3612	High Voltage Peripheral Driver
DS3613	High Voltage Peripheral Driver
DS3614	High Voltage Peripheral Driver
DS7820	Dual Line Receiver
DS8820	Dual Line Receiver
DS7820A	Dual Line Receiver
DS8820A	Dual Line Receiver
DS7830	Dual Differential Line Driver
DS8830	Dual Differential Line Driver
MC1488	Quad Line Driver
MC1489/A	Quad Line Receiver
UDN5711	Dual High Voltage Peripheral Driver (AND)
UDN5712	Dual High Voltage Peripheral Driver (NAND)
UDN5713	Dual High Voltage Peripheral Driver (OR)
UDN5714	Dual High Voltage Peripheral Driver (NOR)
75S107	High Speed Dual Line Receiver
75S108	High Speed Dual Line Receiver
55/75450B	Dual Peripheral Positive Driver
55/75451B	Dual Peripheral Positive Driver
55/75452B	Dual Peripheral Positive Driver
55/75453B	Dual Peripheral Positive Driver
55/75454B	Dual Peripheral Positive Driver
TRANSISTOR ARRAYS	
NE/SE510	Dual Differential Amplifier
NE/SE511	Dual Differential Amplifier
NE5501	High Voltage/High Current Darlington Array
NE5502	High Voltage/High Current Darlington Array
NE5503	High Voltage/High Current Darlington Array
NE5504	High Voltage/High Current Darlington Array
ULN2001	High Voltage/High Current Darlington Transistor Array
ULN2002	High Voltage/High Current Darlington Transistor Array
ULN2003	High Voltage/High Current Darlington Transistor Array
ULN2004	High Voltage/High Current Darlington Transistor Array
CA3081	Seven Transistor Array
CA3082	Seven Transistor Array
CA3183	Seven Transistor Array
PHILIPS INDUSTRIAL	
SAA1027	Stepper Motor Driver Circuit
TAA960	Triple Active Filter Amplifier
TCA210	Audio Amplifier and Preamplifier
TCA580	Integrated Gyrator
TCA980	Microphone Amplifier
TDA1024	Zero Carrying On-Off Triac Control
DISPLAY DRIVERS	
DS8880/8880-1	High Voltage 7-Segment Decoder/Driver
NE580	Bar-Graph Logic Circuit

NE582	Hex Universal Driver
NE586	Bus Compatible, Fixed Current, Seven Segment LED Driver, Sinking
NE587	Bus Compatible, Programmable Current, Seven Segment LED Driver, Sinking
NE590	Addressable Peripheral Drivers, Current Sink
NE591	Addressable Peripheral Drivers, Current Source
NE594	Seven Segment Vacuum Flourescent Display Driver
D/A—A/D CONVERTERS	
MC1408-7	8-Bit Multiplying D/A Converter
MC1408-8	8-Bit Multiplying D/A Converter
MC1508-8	8-Bit Multiplying D/A Converter
NE5007	8-Bit Speed Multiplying D/A Converter
NE/SE5008	8-Bit Speed Multiplying D/A Converter
NE/SE5009	8-Bit Speed Multiplying D/A Converter
NE/SE5018	8-Bit μP-Compatible D/A Converter, Voltage Output
NE/SE5118	8-Bit μP-Compatible D/A Converter, Current Output
NE/SE5019	8-Bit μP-Compatible D/A Converter, Voltage Output, 9 Bit Accuracy
NE/SE5119	8-Bit μP-Compatible D/A Converter, Current Output, 9 Bit Accuracy
NE5034	8-Bit μP-Compatible, Analog-Digital Converter, SAR
AUDIO CIRCUITS	
LM381/381A	Dual Low-Noise Preamp
LM382	Dual Low-Noise Preamp
LM387	Dual Low-Noise Preamp
NE/SE540	Power Driver
NE541	High Voltage Power Driver
NE542	Dual Low-Noise Preamp
NE570	Compandor
NE571	Compandor
RADIO CIRCUITS	
CA3089	FM IF System
CA3089D2	FM IF System
MC1496	Balanced Modulator-Demodulator
MC1596	Balanced Modulator-Demodulator
N5596	Balanced Moldulator-Demodulator
NE546	AM Radio Receiver Subsystem
TCA440	AM Receiver Circuit
μA758	FM Stereo Multiplex Decoder, Phase Locked Loop
TV CIRCUITS	
LM1880	Sync. Processor
MC1327	Chroma Demodulator
TBA120S	8-Stage Amplifier with Balanced Demodulator
TBA120T	FM IF Amplifier and Demodulator
TBA120U	FM IF Amplifier and Demodulator
TBA395	Chrominance Combination Monolithic Silicon Integrated Circuit
TBA396	Luminance and Chrominance Control Combination
TBA1440	TV Video Amplifier-Demodulator
TBA1440G/1441	TV Video Amplifier with Demodulator
TDA2541	Video IF System
ULN2211	2-Watt TV/FM Sound Channel
ULN2212	1-Watt TV/FM Sound Channel
GENERAL CONSUMER	
NE543	Servo Amplifier
NE544	Servo Amplifier
NE644	Servo Amplifier

NE5044	RC Encoder (7 Channel)
NE5045	RC Decoder (7 Channel)
NE5046	RC Decoder (2 Channel)

PHASE LOCKED LOOPS

NE560	Phase Locked Loop
NE561	Phase Locked Loop
NE562	Phase Locked Loop
NE564	Phase Locked Loop
NE/SE565	Phase Locked Loop
NE/SE566	Function Generator
NE/SE567	Tone Decode/Phase Locked Loop

ORDERING INFORMATION

Signetics' Analog integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located on the back cover of this manual.

Minimum Factory Order:

Commercial Product:
- $1000 per order
- $50 per line item per order

Military Product:
- $250 per line item per order

Table 1 provides part number information concerning for both Signetics originated products and industry standard products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Table 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted however, that devices with a SE prefix (-55° C to +125° C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any analog product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

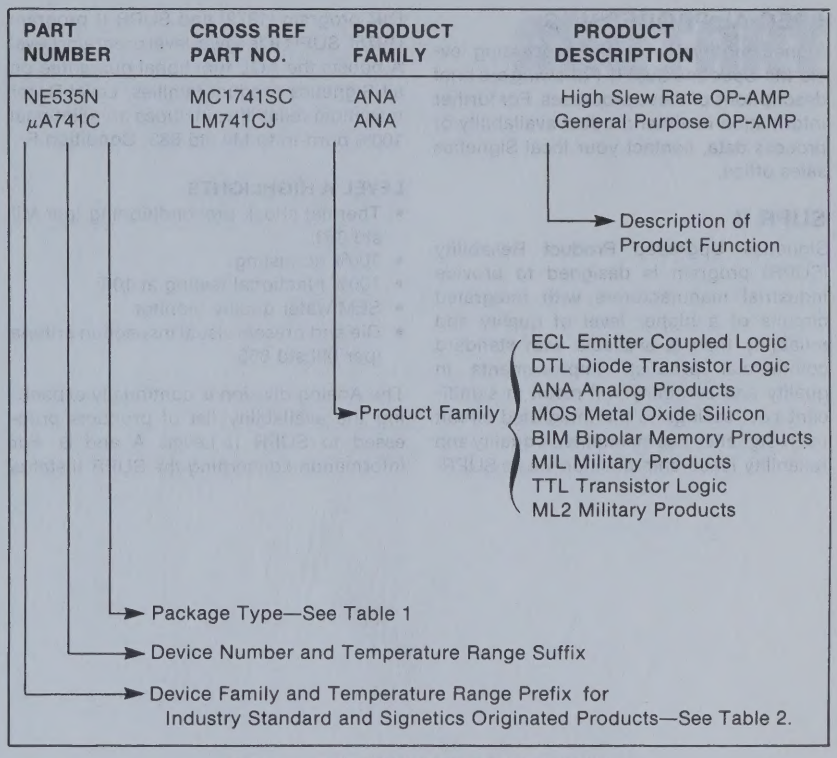


Table 1 PART NUMBER DESCRIPTION

SUFFIX		PACKAGE DESCRIPTION[2]
Old	New	
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
DA	DA	2-lead TO-3
DB	DB	3-lead TO-5
DC	DC	4-lead TO-46
DE	DE	4-lead TO-72
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	K	10-lead TO-100
L	L	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
PN	PHA	12 + 1 GND pin DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
S	S	3-lead TO-92 plastic
SK	SK	Microprocessor kit
T,TA	T	8-lead TO-99
U	U	Plastic power TO-220
V	N	8-lead plastic DIL
W,WJ	W	10, 14, 16 and 24-lead ceramic (Cerpac) flat
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 2 PACKAGE DESCRIPTIONS

PREFIX	DEVICE TEMPERATURE RANGE
N-	0° to +70°C
S-	-55° to +125°C
NE-	0° to +70°C
SE-	-55° to +125°C
SA	-40° to +85°C
SU	-25° to +85°C

Table 3 DEVICE TEMPERATURE

PREFIX	DEVICE FAMILY
CA	Linear Industry Standard
DM	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LH	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
PA	Linear Industry Standard
SD	Linear DMOS
SP	DTL Series
UA	Linear Industry Standard
ULN	Linear Industry Standard

Table 4 FAMILY PREFIX

SPECIAL PROCESSING

Signetics offers two major processing levels: Mil-Spec and Supr II. Following are brief descriptions of these processes. For further information in either product availability or process data, contact your local Signetics sales office.

SUPR II

Signetics Upgraded Product Reliability (SUPR) program is designed to provide industrial manufacturers with integrated circuits of a higher level of quality and reliability than is available with standard commercial product. Improvements in quality and reliability will result in significant cost savings to the integrated circuit user. Signetics has maintained a quality and reliability leadership position via its SUPR-DIP program (1972) and SUPR II program (1975). SUPR II is a two-level program. Level A boosts the AQL functional guarantee on all Signetics product families. Level B, for maximum reliability, includes an additional 100% burn-in to Mil std 883. Condition F.

LEVEL A HIGHLIGHTS

- Thermal shock preconditioning (per Mil std 883)
- 100% dc testing
- 100% functional testing at 100°
- SEM wafer quality monitor
- Die and preseal visual inspection criteria (per Mil std 883)

The Analog division is continually expanding the availability list of products processed to SUPR II Levels A and B. For information concerning the SUPR II status of products contact your local Signetics sales office.

MILITARY

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics MIL 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Fully compliant 883 flows on all products.
- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customer to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2, 3, 4 and 5.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES				
			DUAL-IN-LINE		
	8-PIN	10-PIN	14-PIN	16-PIN	24-PIN
CB	—	—	F	—	—
EB	—	—	—	F	—
JB	—	—	—	—	F
DB	—	—	W	—	—
FB	—	—	—	W	—
ZC	—	—	—	—	Q
GC	T	—	—	—	—
IC	—	K	—	—	—

All products listed are also available in Die form.

Table 1 MILITARY PACKAGE AVAILABILITY

	JB	RB	RC
	Jan Qualified	883B	883C
54/54H	X	X	X
54LS	X	X	X
54S	X	X	X
82/8T	X	X	X
93XX	X	X	X
96XX	—	X	X
Linear	Planned	X	X
Bipolar Memory	Planned	X	X
Microprocessor	—	X	X

Table 2 MILITARY SUMMARY

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 Method 5004, and is 100% electrically tested to industry data sheets. Devices are selectively available as custom processed parts with electricals screened to the JAN Slash Sheets.

MIL-STD-883, LEVEL C

If you need a Military temp, range device, but do not require burn in screening performed, our 883C product is ideal. 883C parts are the standard full Mil-Temperature range product to the Signetics data sheet parameters and screened to MIL-STD-883, Class C.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity or running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 4.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

PROCESS LEVEL AND MARKETING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @25°C	DC/AC @TEMP	QPL	OFFSHORE
JB JM38510XXXXX	2010, Cond. B	Yes	100%	100%	100%	Yes	No
RB SXXXX883B	2010, Cond.B	Yes	100%	100%	100%	No	Yes
RC SXXXX883C	2010, Cond. B	No	100%	100% dc Sample ac	Sample dc only	No	Yes

Table 3 MILITARY PRODUCTS PROCESSING MATRIX

QUALIFIED SUB-GROUPS	QUALIFIES	OPTION 1	OPTION 2
A*	Electrical Test		
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied.	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE*

Group A is performed on each lot or sublot of Signetics devices.

Table 4 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHDS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
General Mil-M-38510	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A
1. Pre-Certification						
A. Product Assurance Program Plan						
B. Manufacturer's Certification						
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A
Screening Per Method 5004 of Mil-Std-883						
6. Internal Visual (Precap)	2010, Cond. A or B	100%	XA	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C)	100%	X	X	X	X
8. Temperature Cycling*	1010, Cond. C; (10 cycles, −65°C to +150°C)	100%	X	X	X	X
*For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, 0° to +100°C)						
9. Constant Acceleration	2001, Cond. E; (30kg in YI Plane)	100%	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X
11. Seal (Hermeticity)	1014					
A. Fine	Cond. A or B (5.0 X 10^{-8}CC/Sec)	100%	X	X	X	X
B. Gross	Cond. C2 Min.	100%	X	X	X	X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100% Optional	100% Read & Record	Slash Sheet	Data Sheet	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100% 240 hrs.	X		N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1		X	X	X	X
B. Static Tests @ +125°C	Sub Group 2		X	X	X	N/A
C. Static Tests @ −55°C	Sub Group 3		X	X	X	N/A

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
D. Dynamic Test @25°C	Sub Group 4 (for Linear Product Mainly)		X	X	X	X
E. Functional Test @25°C	Sub Group 7		X	X	X	X
F. Switching Test @25°C	Sub Group 9		X	X	X	N/A
15. Percent Defective allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @ 25°C (A-1). This is controlled by the slash sheets for JB & JBX products. For RBX & RB 10% is standard	10%	5%	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	As Req'd	JM38510/XXXX Slash Sheet #	S X X X X 883B	SXXXX 883C
17. X-Ray	2012		100%	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std 883						
19. Group A	Electrical Tests-Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every 6 week per microcircuit group	X	X	Generic Data Available	
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constand acceleration.	Every 3 months per package type	X	X	Generic Data Available	
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available	

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD CLASS B PRODUCTS (Cont'd)

LINEAR PRODUCTS

DEVICE	DESCRIPTION	PACKAGE	
	COMPARATORS		
SE521	Dual Comparator	F	
SE522	Dual Comparator	F	
SE526	Analog Voltage Comparator	F	K
SE527	Analog Voltage Comparator	F	K
SE529	Analog Voltage Comparator	F	K
LH2111	Dual Comparator	F	
LM111	Comparator	F	T
LM119	Dual Comparator	F	K
LM139	Quad Comparator	F	
LM193/ 193A	Dual Comparator		T
μA710	Differential Voltage Comparator	F	T
μA711	Comparator	F	K
	DIFFERENTIAL AMPLIFIERS		
SE510	Dual Differential Amplifier	F	
SE511	Dual Differential Amplifier	F	
SE515	Differential Amplifier	F	K
μA733	Video Amplifier	F	K
	OPERATIONAL AMPLIFIERS		
LF155/ 156/157	FET Operational Amplifier	T	
LH2101A	Dual Operational Amplifier	F	
LH2108A	Dual Operational Amplifier	F	
LM101	High Performance Operational Amp	F	T
LM101A	High Performance Operational Amp	F	T
LM107	General Purpose Operational Amp	F	F
LM108	Precision Operational Amp	F	T
LM108A	Precision Operational Amp	F	T
LM124	Quad Operational Amplifier	F	
LM158	Dual Operational Amplifier		T
MC1556	Operational Amplifier	F	T
MC1558	Dual Operational Amplifier	F	T
SE532	Dual Operational Amplifier		T
SE535	Hi Slew Rate Operational Amp	T	
SE538	Hi Slew Rate Operational Amp	T	
μA709	Operational Amplifier	F	T
μA709A	Operational Amplifier	F	T
μA741	General Purpose Operational Amp	F	T
μA747	Dual Operational Amplifier	F	K
μA748	General Purpose Amp	F	T
SE530	Hi Slew Op Amp	F	T
SE5530	Dual Hi Slew Op Amp	F	K
SE5534	Lo Noise Op Amp	T	
SE5535	Dual Hi Slew Op Amp	F	K
SE5538	Dual Hi Slew Op Amp	F	K
SE5537	Sample & Hold	F	K
SE5539	Hi Speed Op Amp	F	K

DEVICE	DESCRIPTION	PACKAGE	
	PHASE LOCKED LOOPS		
SE567	Tone Decoder PLL	F	T
SE564	Phase Locked Loop	F	T
	INTERFACE		
55325	Memory Driver	F	
	LINE RECEIVERS		
DM7820	Dual Differential Line Receiver	F	
DM7830	Dual Differential Line Receiver	F	
	AUDIO CIRCUITS		
SE570	Compandor	F	
	TIMERS		
SE555	Timer	F	T
SE556	Dual Timer	F	T
SE558/559	Quad Timer	F	
	VOLTAGE REGULATORS		
LM109	5 Volt Regulator	DA	
SE5551	Dual Track Reg	F	
SE5552	Dual Track Reg	F	
SE5553	Dual Track Reg	F	
SE5554	Dual Track Reg	F	
78XX(7)	Positive Reg	DA	
79XX(7)	Negative Reg	DA	
79MXX(7)	Med Power Reg	DB	
μA723	Precision Voltage Regulator	F	L
†78HV00(7)	Hi Voltage Regulator	DA	
	DRIVERS		
DS1611-1614	Peripheral Drivers		T

*NOTE
F = Cerdip
K/T/L = Metal Can
DA/DB = TO-3 can
Flat pack available—special request

JAN-M-38510				
DEVICE	SLASH SHEET	PACKAGE		QUAL. STATUS
†JB555	10901	F	T	Part II
†JB556	10902	F		Part II
†JB2101A	10105	F		Part II
JB101	10103	F	T	June 1978-Part I
JB741	10101	F	T	June 1978-Part I
JB747	10102	F	K	June 1978-Part I

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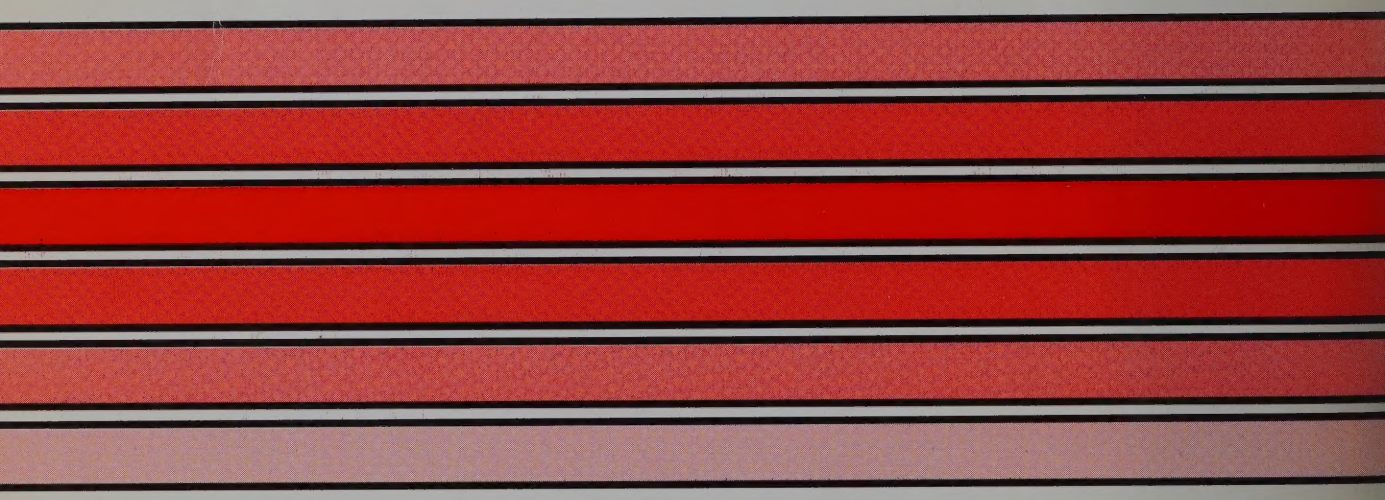

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